## N- and P-Channel 30-V (D-S) MOSFET

### GENERAL DESCRIPTION

The ME4542D is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

### FEATURES

- $R_{DS(ON)} \leqq 25.5m\Omega @ V_{GS}=10V$ (N-Ch)
- $R_{DS(ON)} \leqq 40m\Omega @ V_{GS}=4.5V$ (N-Ch)
- $R_{DS(ON)} \leqq 33m\Omega @ V_{GS}=-10V$ (P-Ch)
- $R_{DS(ON)} \leqq 43m\Omega @ V_{GS}=-4.5V$ (P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

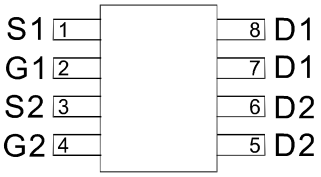
### APPLICATIONS

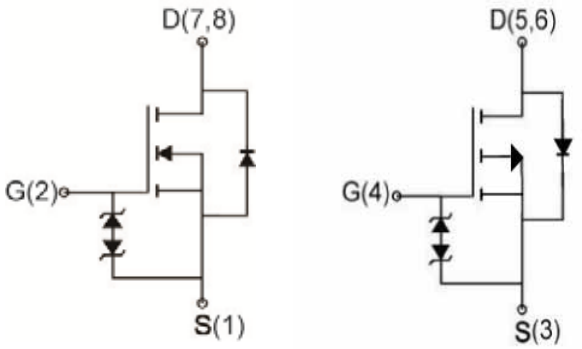
- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- LCD Display inverter

### PIN CONFIGURATION

(SOP-8)

Top View




**Ordering Information**: ME4542D (Pb-free)

ME4542D-G (Green product-Halogen free)

### Absolute Maximum Ratings ($T_A$=25℃ Unless Otherwise Noted)

| Parameter | | Symbol | N-Channel | P-Channel | Unit |
|---|---|---|---|---|---|
| | | | Steady State | Steady State | |
| Drain-Source Voltage | | $V_{DSS}$ | 30 | -30 | V |
| Gate-Source Voltage | | $V_{GSS}$ | ±20 | ±16 | |
| Continuous Drain Current(Tj=150℃) | $T_A$=25℃ | $I_D$ | 6.8 | 6.2 | A |
| | $T_A$=70℃ | | 5.4 | 4.9 | |
| Pulsed Drain Current | | $I_{DM}$ | 30 | -30 | |
| Avalanche Energy with Single Pulse(L=0.1mH) | | Eas | 4.4 | 20 | mJ |
| Maximum Power Dissipation | $T_A$=25℃ | $P_D$ | 2 | 2 | W |
| | $T_A$=70℃ | | 1.28 | 1.28 | |
| Operating Junction Temperature | | $T_J$ | -55 to 150 | | ℃ |
| Thermal Resistance-Junction to Ambient * | | $R_{\theta JA}$ | 62.5 | 62.5 | ℃/W |

*The device mounted on 1in2 FR4 board with 2 oz copper

## N- and P-Channel 30-V (D-S) MOSFET

**Electrical Characteristics** ($T_A$=25°C Unless Otherwise Specified)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **STATIC** | | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=250μA<br>$V_{GS}$=0V, $I_D$=-250μA | N-Ch<br>P-Ch | 30<br>-30 | | | V |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250μA<br>$V_{DS}$=$V_{GS}$, $I_D$=-250μA | N-Ch<br>P-Ch | 1.0<br>-1.0 | 1.6<br>-1.5 | 3.0<br>-3.0 | V |
| $I_{GSS}$ | Gate Leakage Current | $V_{DS}$=0V, $V_{GS}$=±16V<br>$V_{DS}$=0V, $V_{GS}$=±12V | N-Ch<br>P-Ch | | | ±10<br>±10 | μA |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=30V, $V_{GS}$=0V<br>$V_{DS}$=-30V, $V_{GS}$=0V | N-Ch<br>P-Ch | | | 1<br>-1 | μA |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance[a] | $V_{GS}$=10V, $I_D$= 6.7A<br>$V_{GS}$=-10V, $I_D$= -6.1A | N-Ch<br>P-Ch | | 21<br>25 | 25.5<br>33 | mΩ |
| | | $V_{GS}$=4.5V, $I_D$= 5.0A<br>$V_{GS}$=-4.5V, $I_D$= -5.0A | N-Ch<br>P-Ch | | 33<br>32 | 40<br>43 | |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=1.7A, $V_{GS}$=0V<br>$I_S$=-1.7A, $V_{GS}$=0V | N-Ch<br>P-Ch | | 0.78<br>0.77 | 1.2 | V |
| **DYNAMIC** | | | | | | | |
| Qg | Total Gate Charge | N-Channel<br>$V_{DS}$=15V, $V_{GS}$=10V, $I_D$=6.7A<br>P-Channel<br>$V_{DS}$=-15V, $V_{GS}$=-10V, $I_D$=-6.1A | N-Ch<br>P-Ch | | 11<br>23 | | nC |
| Qgs | Gate-Source Charge | | N-Ch<br>P-Ch | | 3<br>4 | | |
| Qgd | Gate-Drain Charge | | N-Ch<br>P-Ch | | 2<br>3.7 | | |
| Ciss | Input Capacitance | N-Channel<br>$V_{DS}$=15V, $V_{GS}$=0V, f=1MHz<br>P-Channel<br>$V_{DS}$=15V, $V_{GS}$=0V, f=1MHz | N-Ch<br>P-Ch | | 360<br>880 | | pF |
| Coss | Output Capacitance | | N-Ch<br>P-Ch | | 67<br>130 | | |
| Crss | Reverse Transfer Capacitance | | N-Ch<br>P-Ch | | 20<br>40 | | |
| Rg | Gate Resistance | $V_{DS}$=0V, $V_{GS}$=0V, f=1MHz | N-Ch<br>P-Ch | | 2.2<br>4.2 | | Ω |
| $t_{d(on)}$ | Turn-On Delay Time | N-Channel<br>$V_{DD}$=15V, $R_L$=15Ω<br>$I_D$=1A, $V_{GEN}$=10V, $R_G$=6Ω<br>P-Channel<br>$V_{DD}$=-15V, $R_L$=15Ω<br>$I_D$=-1A, $V_{GEN}$=-10V,$R_G$=6Ω | N-Ch<br>P-Ch | | 10<br>38 | | ns |
| $t_r$ | Turn-On Rise Time | | N-Ch<br>P-Ch | | 13<br>19 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | N-Ch<br>P-Ch | | 31<br>58 | | |
| $t_f$ | Turn-Off Fall Time | | N-Ch<br>P-Ch | | 4<br>9 | | |

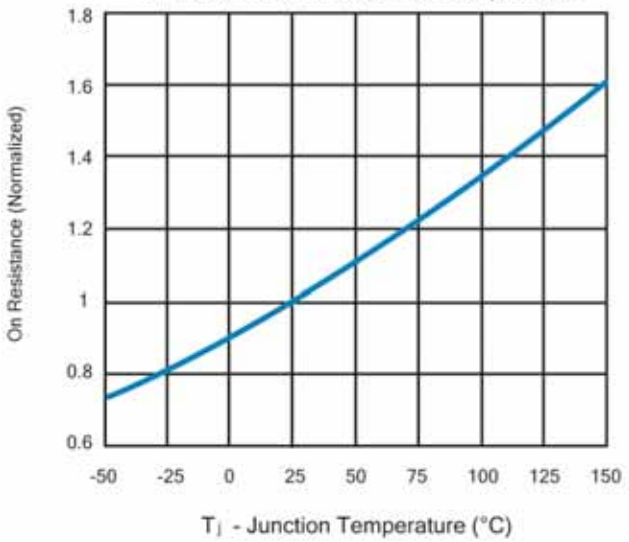
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

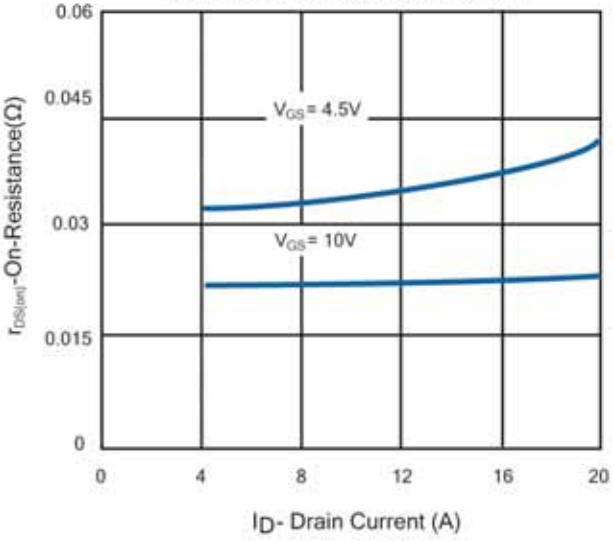
## N- and P-Channel 30-V (D-S) MOSFET

### Typical Characteristics ($T_J$ =25°C Noted) N-CHANNEL

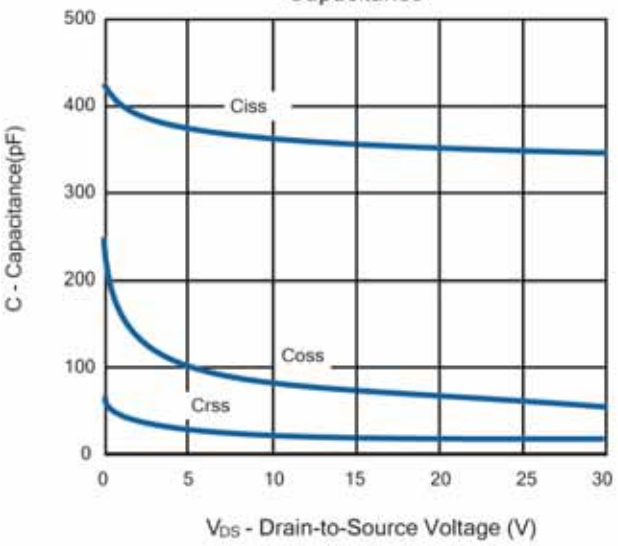
On Resistance vs. Junction Temperature



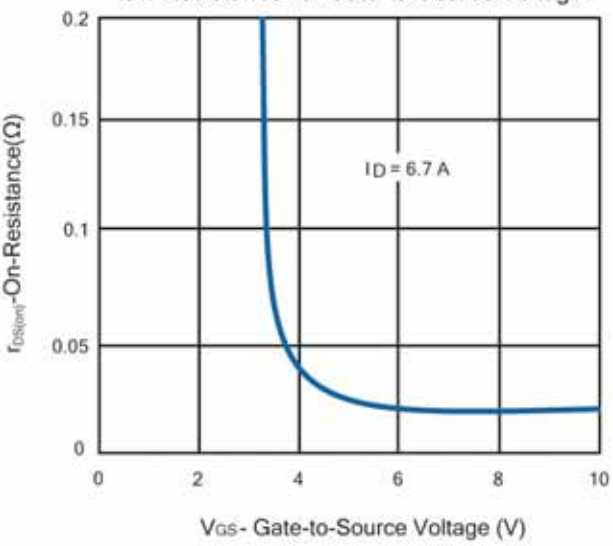

On-Resistance vs. Drain Current



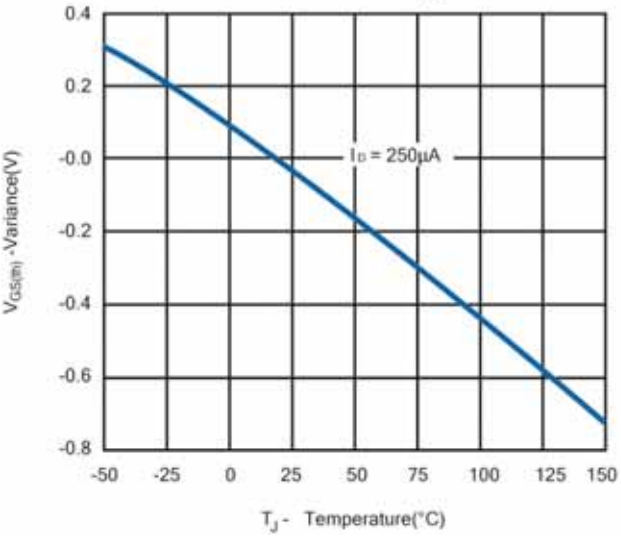

Capacitance



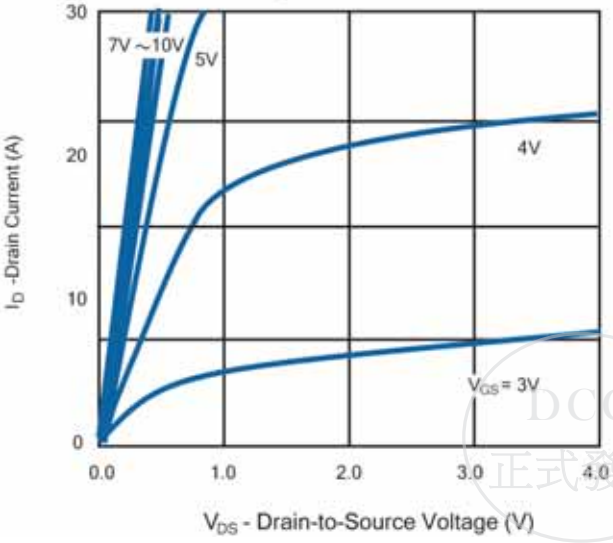

On-Resistance vs. Gate-to-Source Voltage




Threshold Voltage



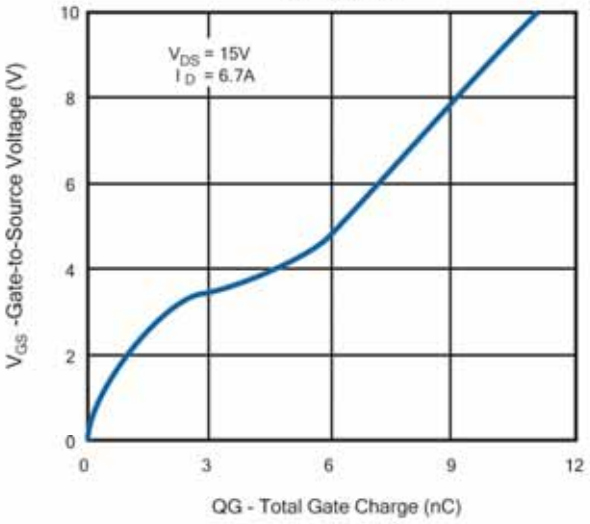

On-Region Characteristics



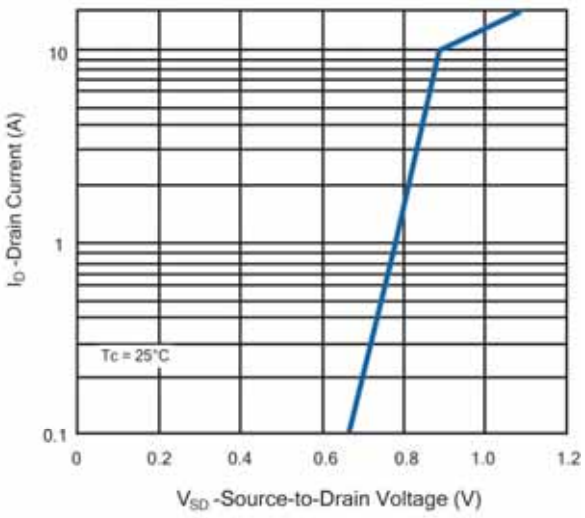
## N- and P-Channel 30-V (D-S) MOSFET

### Typical Characteristics ($T_J$ =25℃ Noted) N-CHANNEL

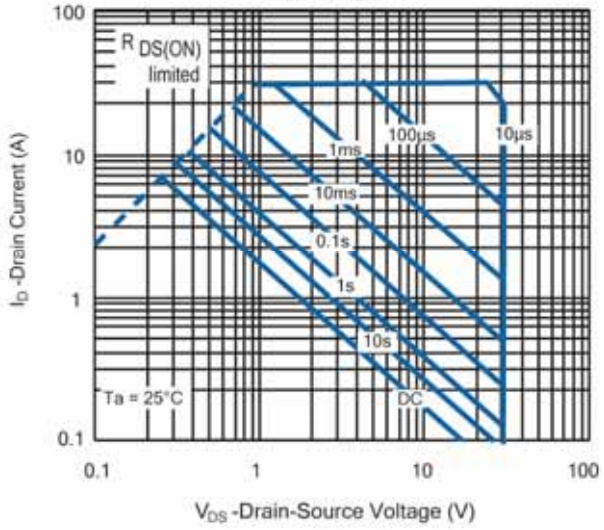
Gate Charge



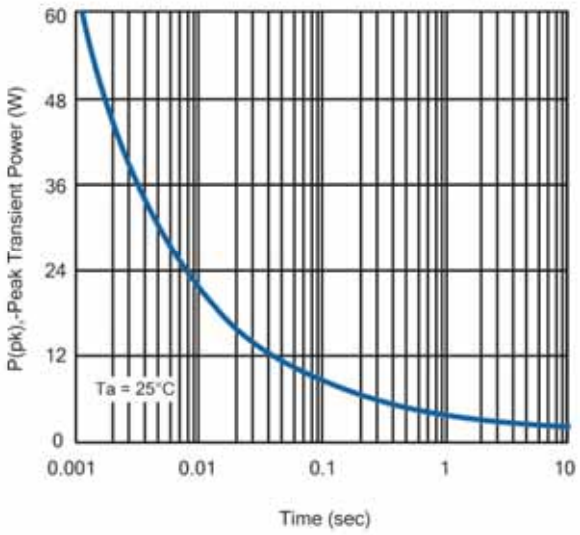

On-Resistance vs. Drain Current



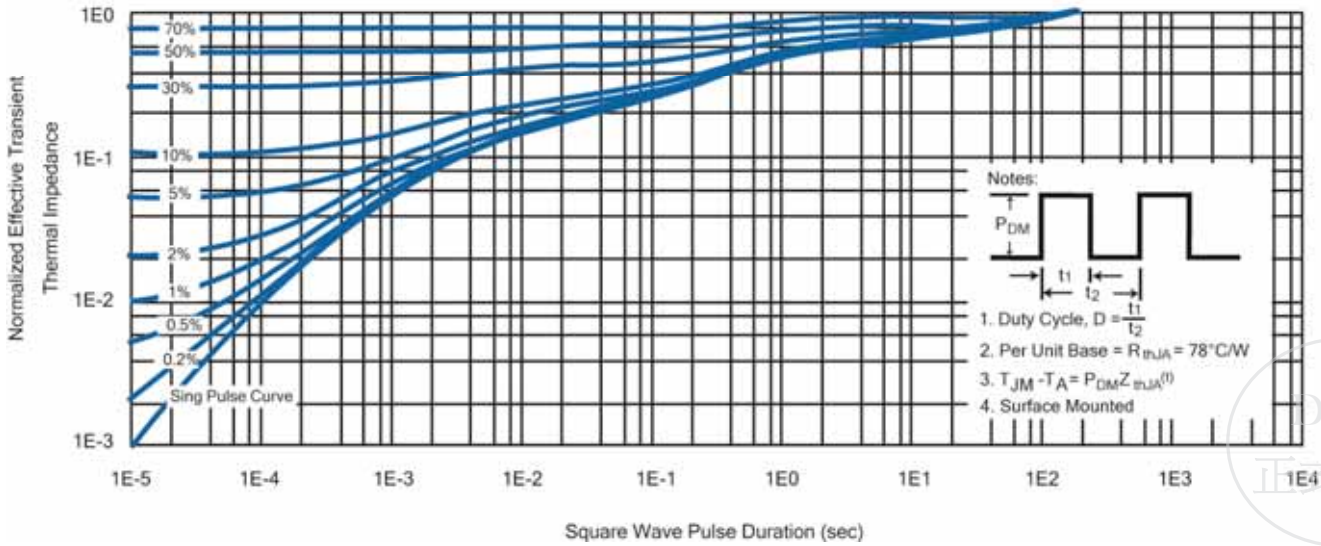

Maximum Forward Biased Safe Operating Area




Single Pulse Maximum Power Dissipation




Normalized Thermal Transient Impedance, Junction-to-Ambient

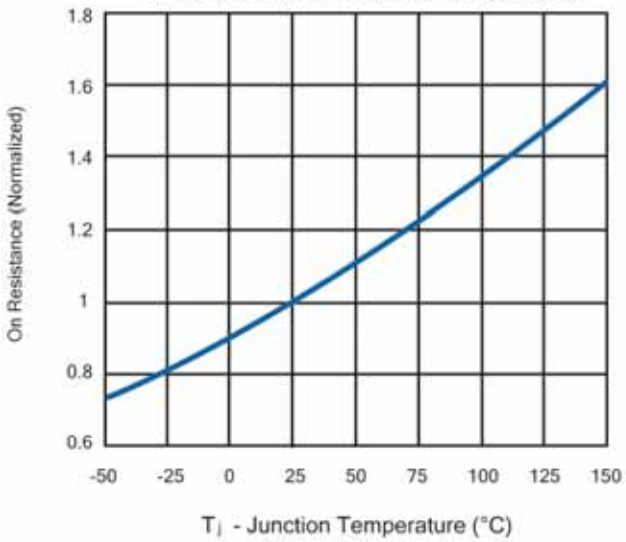


## N- and P-Channel 30-V (D-S) MOSFET

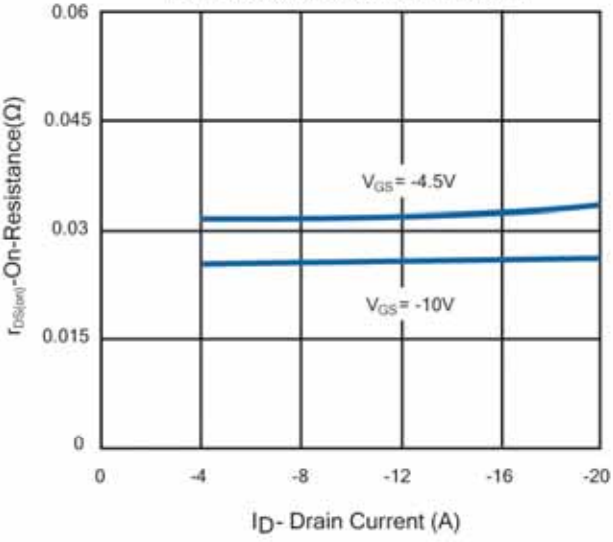
### Typical Characteristics ($T_J$ =25°C Noted)

### P-CHANNEL

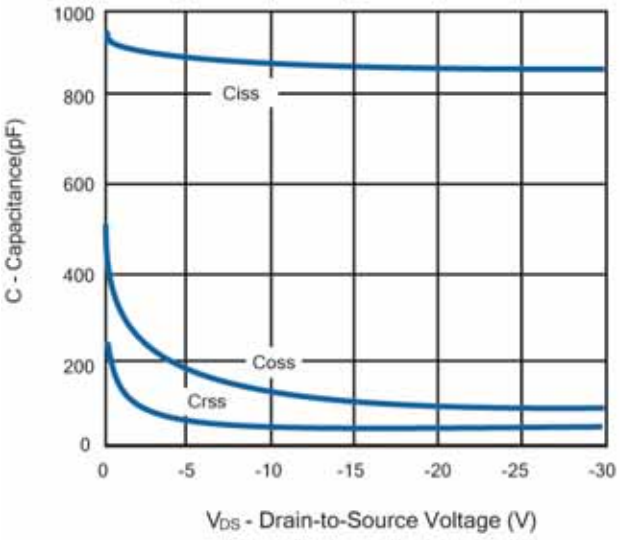
On Resistance vs. Junction Temperature



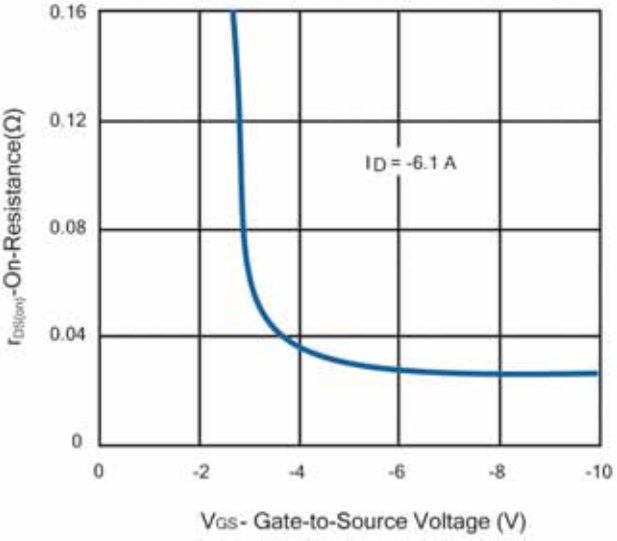

On-Resistance vs. Drain Current



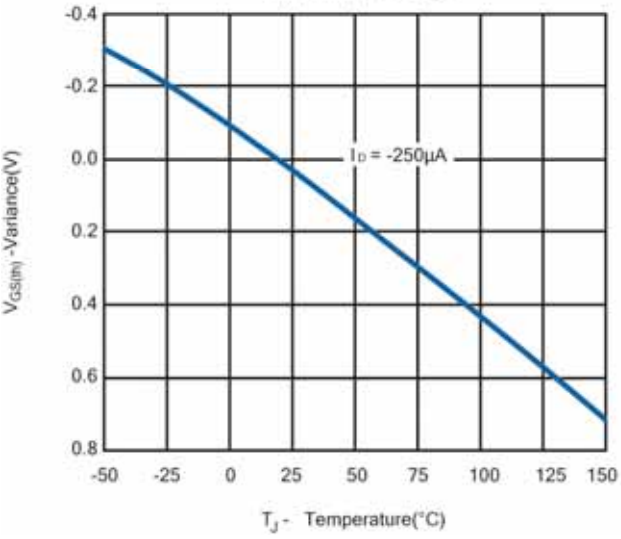

Capacitance



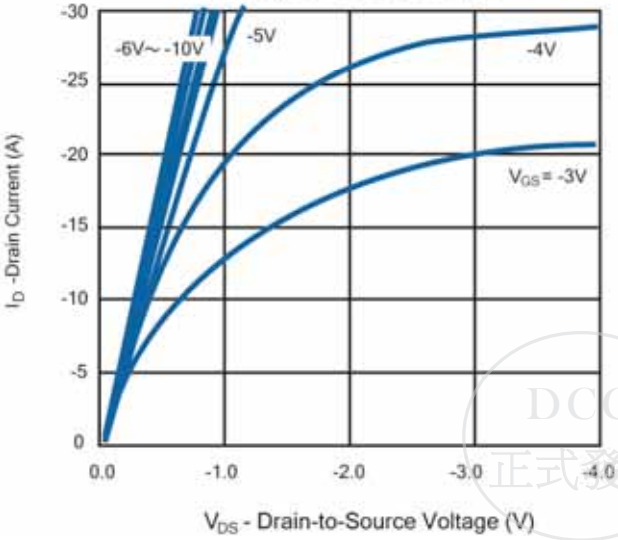

On-Resistance vs. Gate-to-Source Voltage




Threshold Voltage



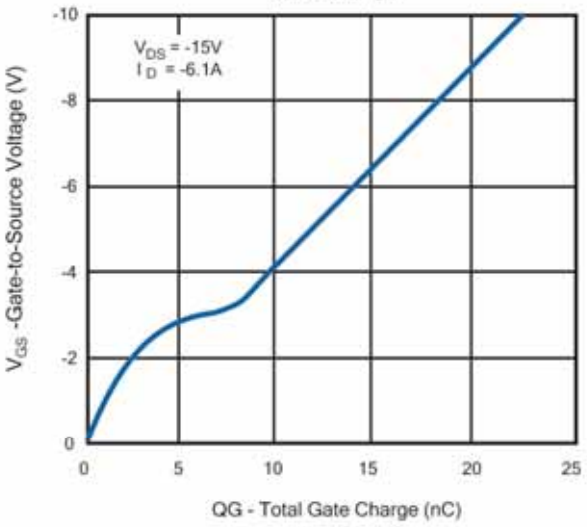

On-Region Characteristics



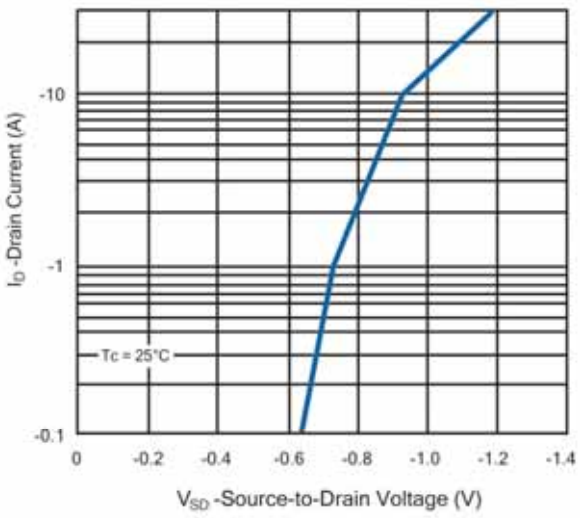
## N- and P-Channel 30-V (D-S) MOSFET

### Typical Characteristics ($T_J$ =25℃ Noted) P-CHANNEL

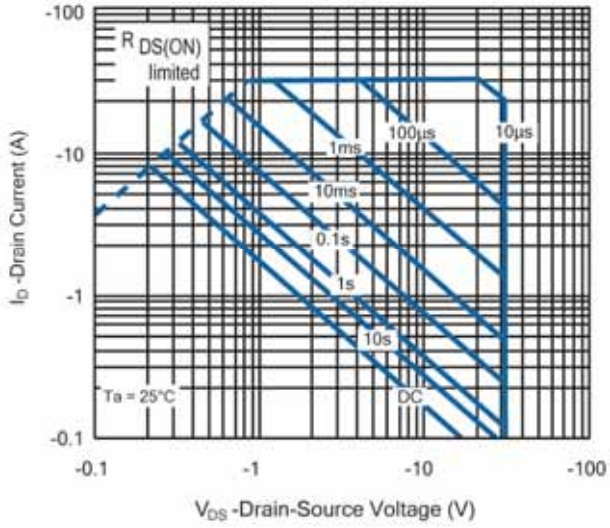
Gate Charge



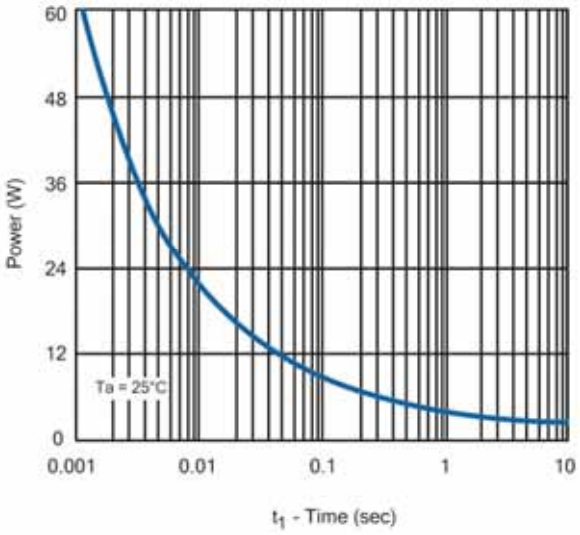

On-Resistance vs. Drain Current



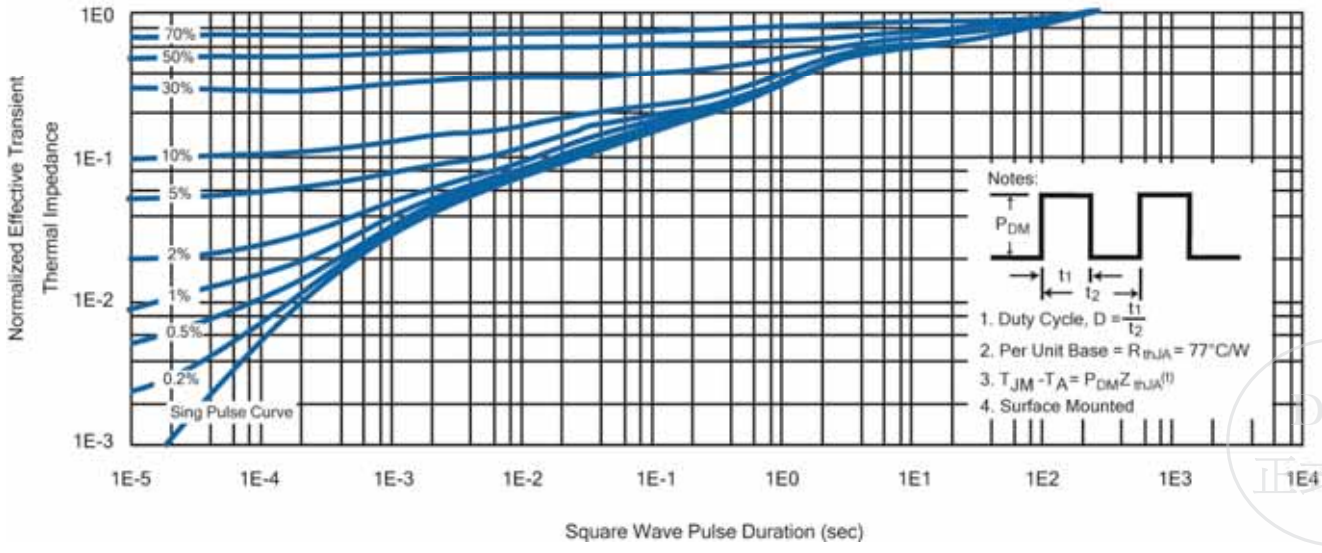

Maximum Forward Biased Safe Operating Area



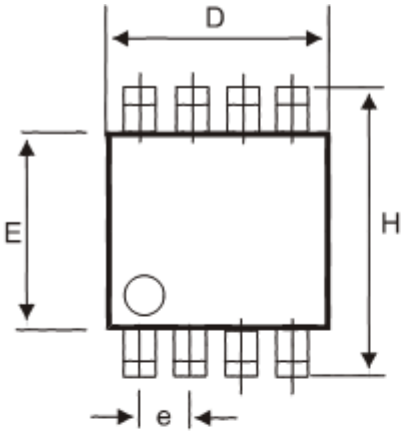

Single Pulse Maximum Power Dissipation

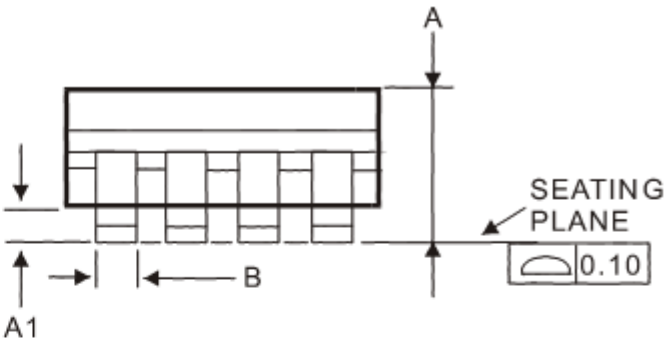


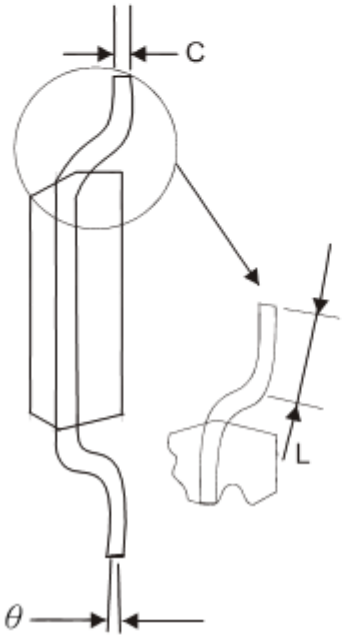

Normalized Thermal Transient Impedance, Junction-to-Ambient



# SOP-8 Package Outline




| DIM | MILLIMETERS (mm) | |
|---|---|---|
| | MIN | MAX |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.18 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| L | 0.40 | 1.25 |
| θ | 0° | 7° |

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.