N- and P-Channel 30-V (D-S) MOSFET , ESD Protection

GENERAL DESCRIPTION

The ME4544D is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 27m\Omega @ V_{GS}=10V$ (N-Ch)
- $R_{DS(ON)} \leqq 42m\Omega @ V_{GS}=4.5V$ (N-Ch)
- $R_{DS(ON)} \leqq 62m\Omega @ V_{GS}=-10V$ (P-Ch)
- $R_{DS(ON)} \leqq 83m\Omega @ V_{GS}=-4.5V$ (P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

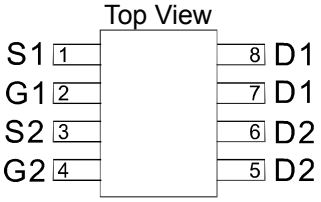
APPLICATIONS

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- LCD Display inverter

PIN CONFIGURATION

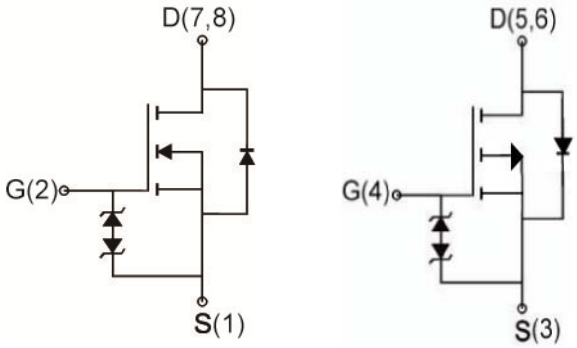
(SOP-8)

Top View



Ordering Information: ME4544D (Pb-free)

ME4544D-G (Green product-Halogen free)



Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DSS}	30	-30	V
Gate-Source Voltage		V_{GSS}	±20	±16	
Continuous Drain Current	T_A=25℃	I_D	6.8	-4.5	A
	T_A=70℃		5.4	-3.6	
Pulsed Drain Current		I_{DM}	27	-18	
Maximum Power Dissipation	T_A=25℃	P_D	2	2	W
	T_A=70℃		1.28	1.28	
Operating Junction and Storage Temperature Range		TJ, Tstg	-55 to 150		℃
Thermal Resistance-Junction to Ambient *		$R_{\theta JA}$	62.5	62.5	℃/W

*The device mounted on 1in2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
STATIC							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA V_{GS}=0V, I_D=-250μA	N-Ch P-Ch	30 -30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA V_{DS}=V_{GS}, I_D=-250μA	N-Ch P-Ch	1.0 -1.0		3.0 -3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±16V V_{DS}=0V, V_{GS}=±12V	N-Ch P-Ch			±10 ±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V V_{DS}=-30V, V_{GS}=0V	N-Ch P-Ch			1 -1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D= 6.9A V_{GS}=-10V, I_D= -6.1A	N-Ch P-Ch		21 48	27 62	mΩ
		V_{GS}=4.5V, I_D= 5.8A V_{GS}=-4.5V, I_D= -5.1A	N-Ch P-Ch		34 65	42 83	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V I_S=-1.7A, V_{GS}=0V	N-Ch P-Ch		0.78 0.8	1.2	V
DYNAMIC							
Qg	Total Gate Charge	N-Channel V_{DS}=15V, V_{GS}=10V, I_D=6.9A P-Channel V_{DS}=-15V, V_{GS}=-10V, I_D=-6.1A	N-Ch P-Ch		11 11.7		nC
Qgs	Gate-Source Charge		N-Ch P-Ch		3.1 3.3		
Qgd	Gate-Drain Charge		N-Ch P-Ch		2.2 2		
Ciss	Input Capacitance	N-Channel V_{DS}=15V, V_{GS}=0V, f=1MHz P-Channel V_{DS}=15V, V_{GS}=0V, f=1MHz	N-Ch P-Ch		335 432		pF
Coss	Output Capacitance		N-Ch P-Ch		74 79		
Crss	Reverse Transfer Capacitance		N-Ch P-Ch		47 51		
$t_{d(on)}$	Turn-On Delay Time	N-Channel V_{DD}=15V, R_L =15Ω I_D=1A, V_{GEN}=10V, R_G=6Ω P-Channel V_{DD}=-15V, R_L =15Ω I_D=-1A, V_{GEN}=-10V,R_G=6Ω	N-Ch P-Ch		9 34.6		ns
tr	Turn-On Rise Time		N-Ch P-Ch		17.6 18.9		
$t_{d(off)}$	Turn-Off Delay Time		N-Ch P-Ch		22.9 40.9		
tf	Turn-Off Fall Time		N-Ch P-Ch		3.3 5.5		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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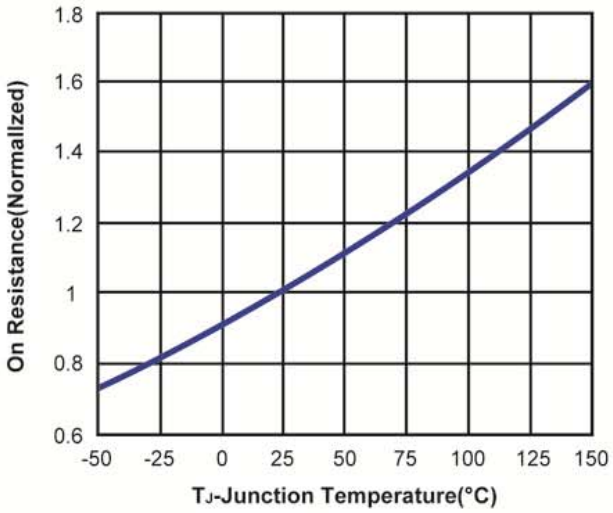
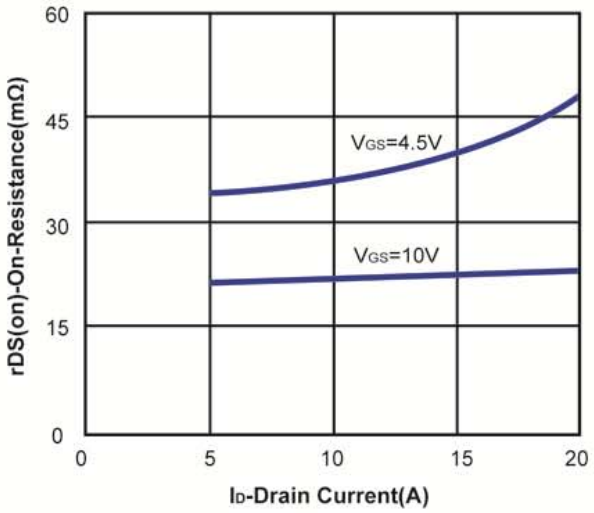
Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

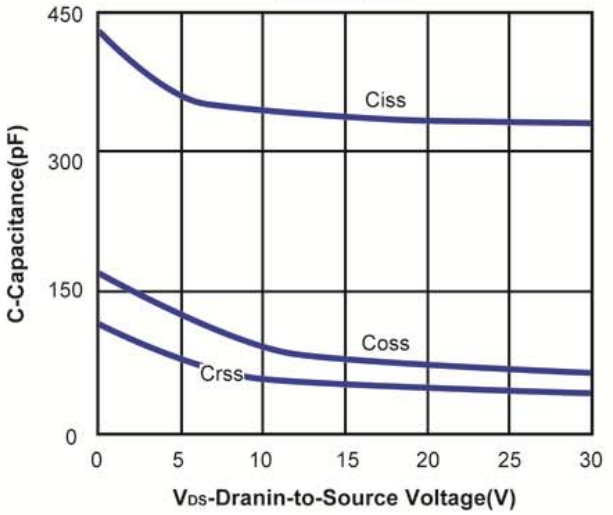
On Resistance vs. Junction Temperature



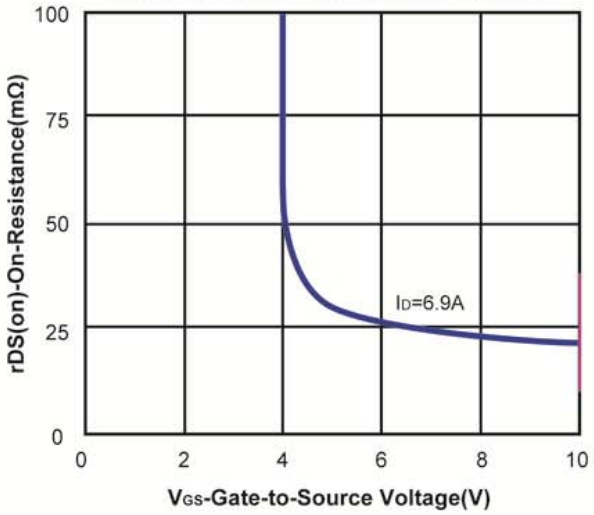
On Resistance vs. Drain Current



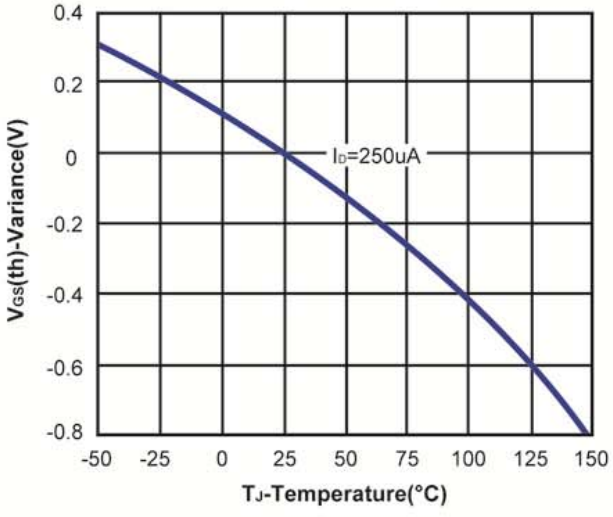
Capacitance



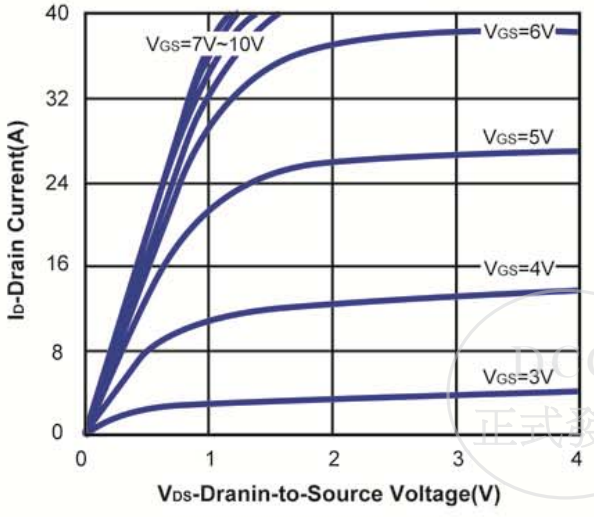
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



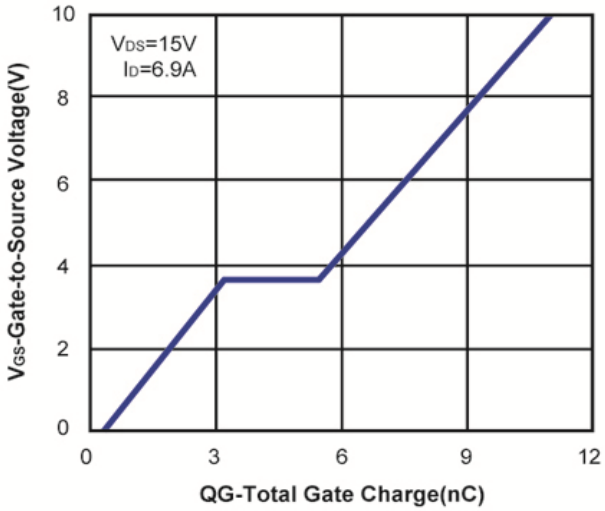
On-Region Characteristics



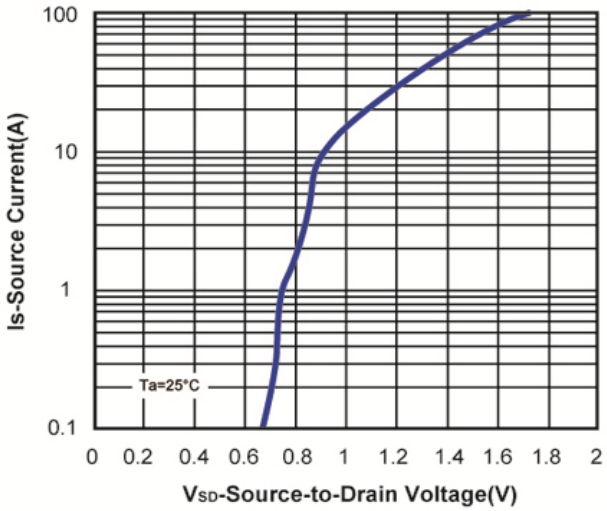
N- and P-Channel 30-V (D-S) MOSFET , ESD Protection

Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

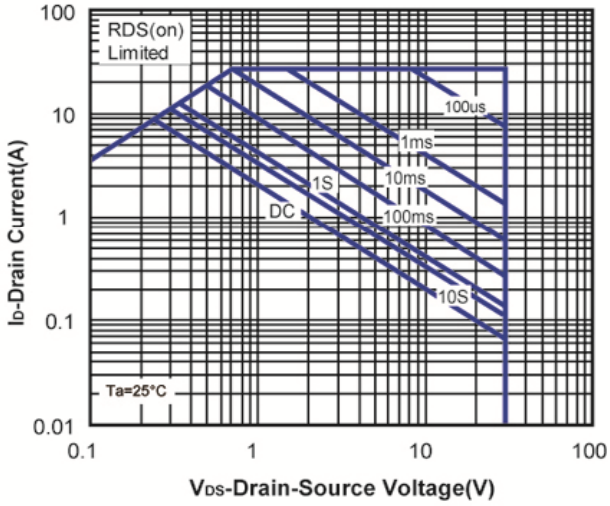
Gate Charge



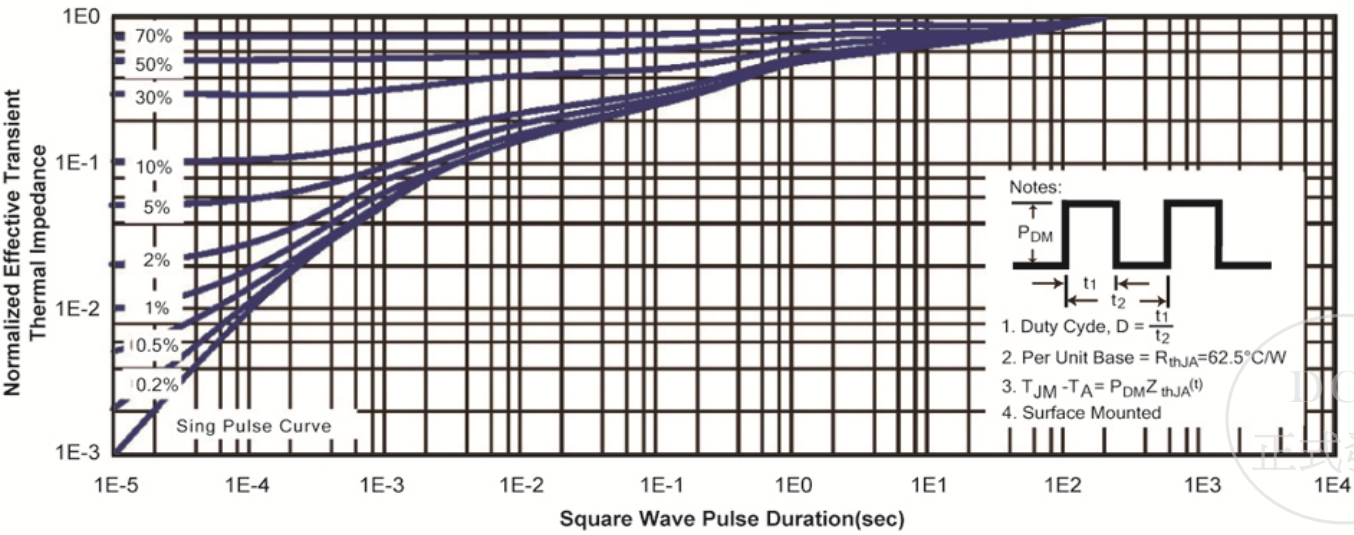
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



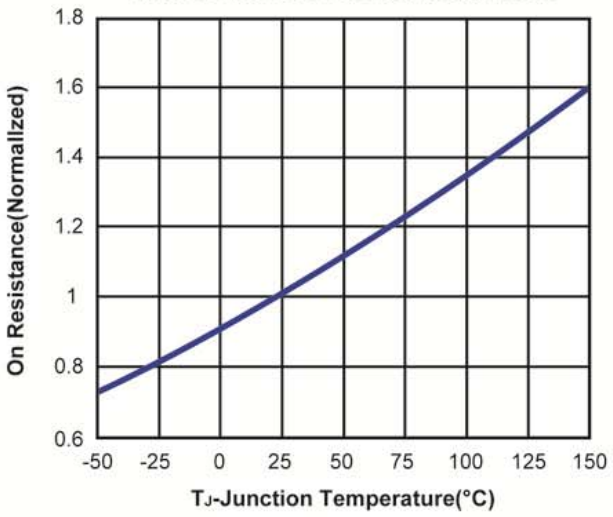
Normalized Thermal Transient Impedance, Junction-to-Ambient



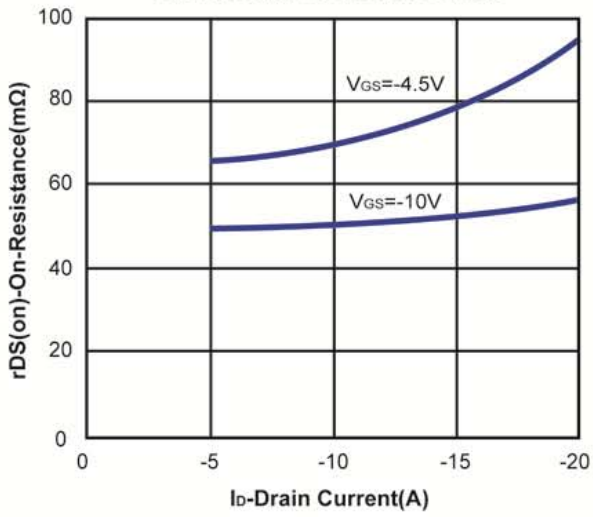
N- and P-Channel 30-V (D-S) MOSFET , ESD Protection

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

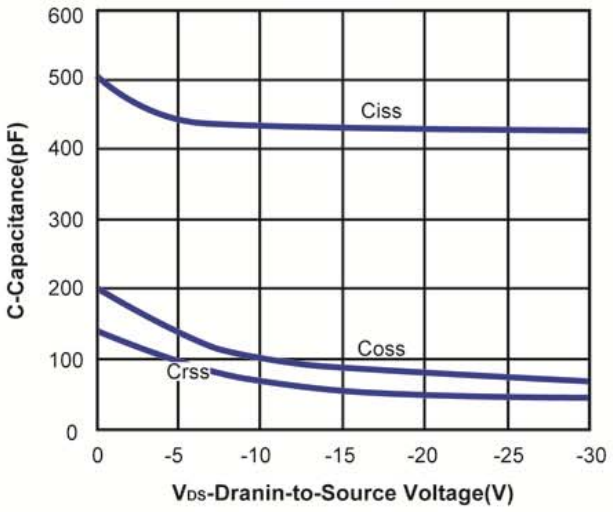
On Resistance vs. Junction Temperature



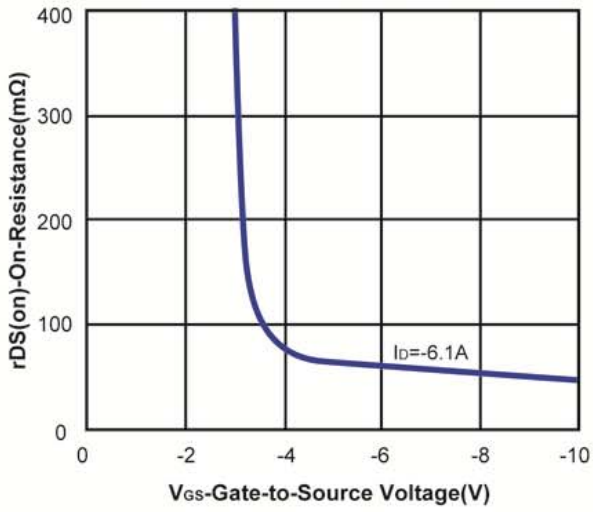
On Resistance vs. Drain Current



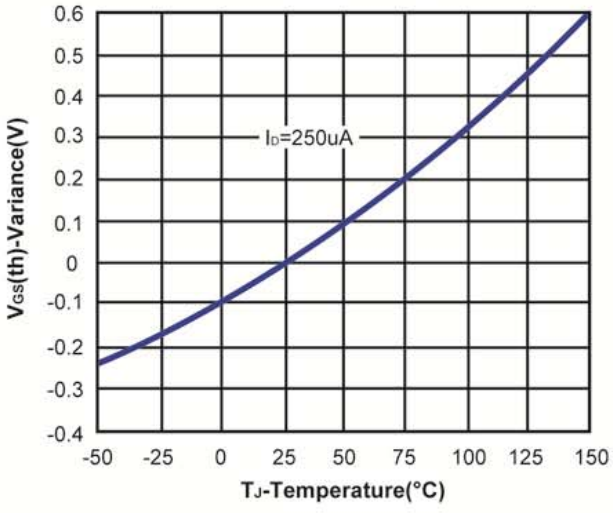
Capacitance



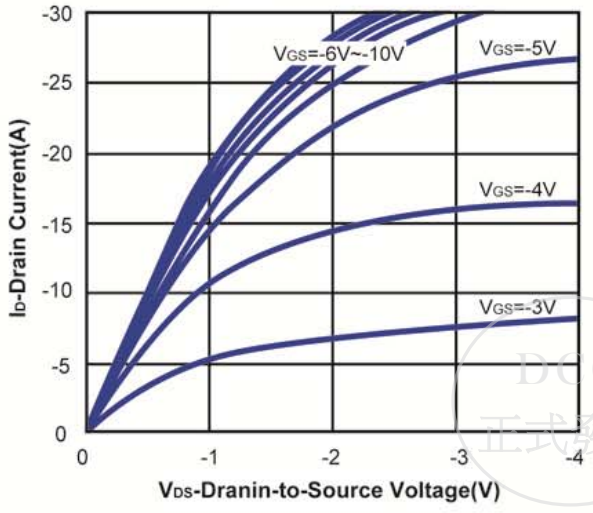
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



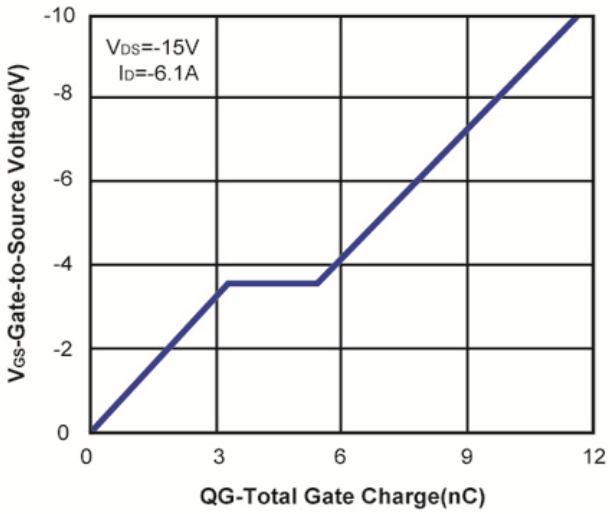
On-Region Characteristics



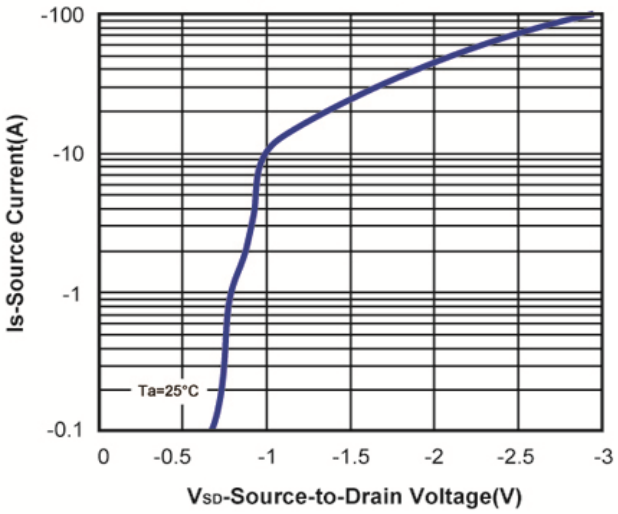
N- and P-Channel 30-V (D-S) MOSFET , ESD Protection

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

Gate Charge



Body-diode characteristics



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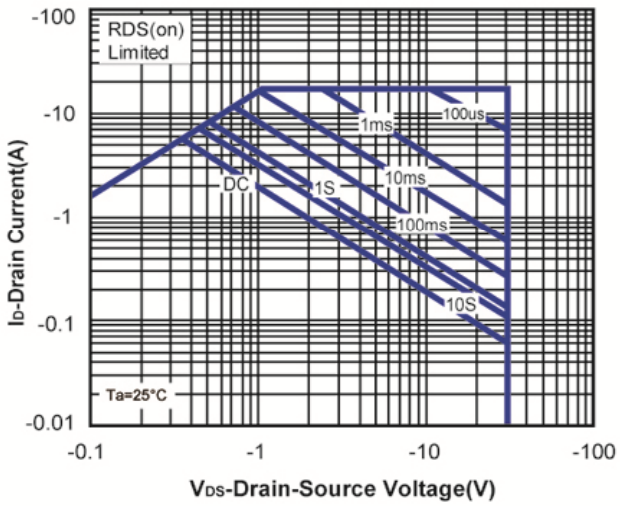
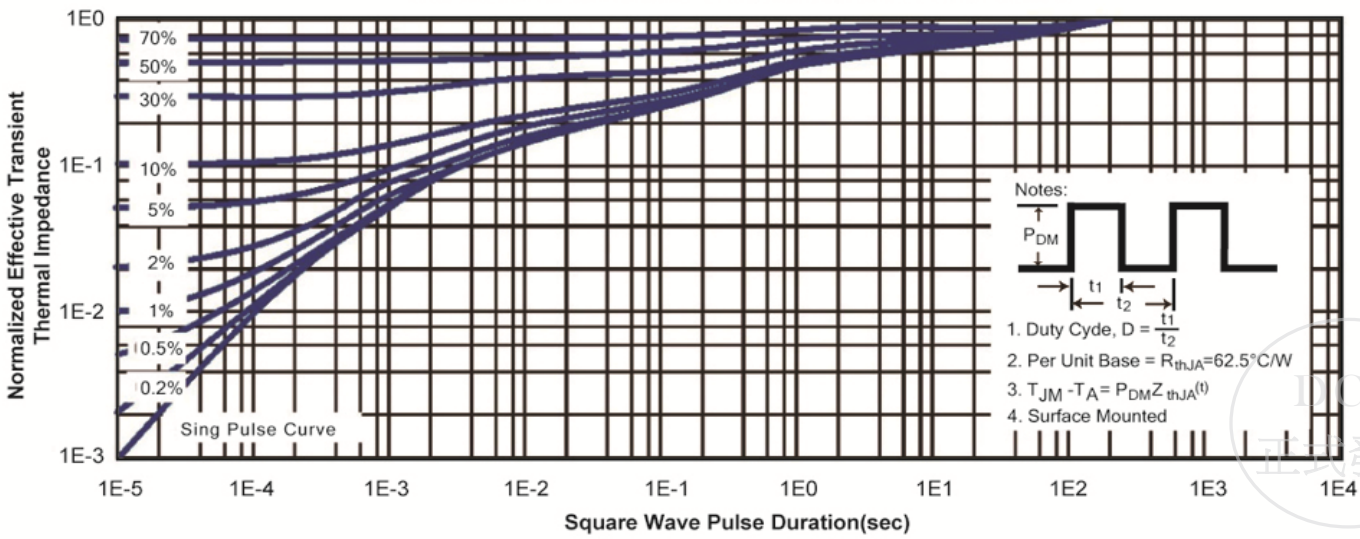
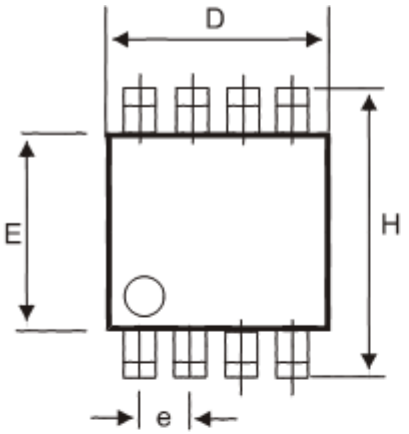
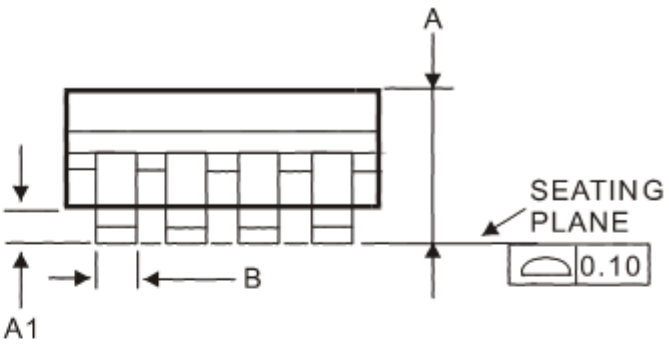


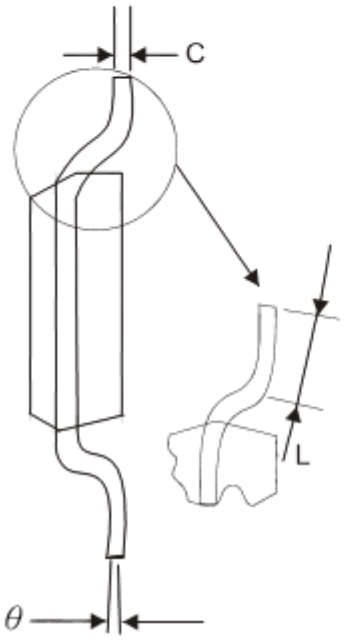
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.