Dual N- and P-Channel 30-V (D-S)

GENERAL DESCRIPTION

The ME4548 is the dual N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦18 mΩ@V_{GS}=10V (N-Ch)
- $R_{DS(ON)}$ ≦29 mΩ@V_{GS}=4.5V(N-Ch)
- $R_{DS(ON)}$ ≦20mΩ@V_{GS}=-10V(P-Ch)
- $R_{DS(ON)}$ ≦29 mΩ@V_{GS}=-4.5V(P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

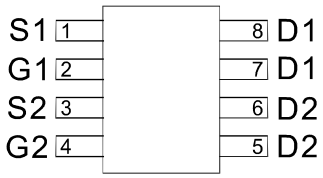
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switching
- LCD Display inverter

PIN CONFIGURATION

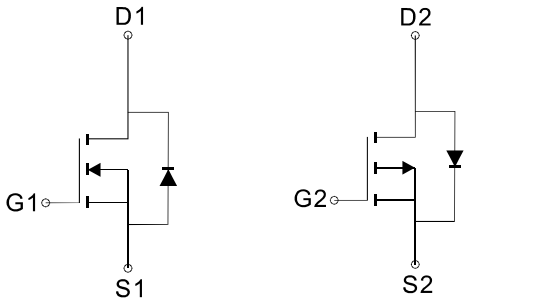
(SOP-8)

Top View



Ordering Information: ME4548 (Pb-free)

ME4548-G (Green product-Halogen free)



N-Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	N-Channel Maximum Ratings	P-Channel Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current*	T_A=25℃	I_D	8.3	-7.3	A
	T_A=70℃		6.6	-5.8	
Pulsed Drain Current		I_{DM}	33	-29	A
Maximum Power Dissipation*	T_A=25℃	P_D	2	2	W
	T_A=70℃		1.28	1.28	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	62.5		℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

Dual N- and P-Channel 30-V (D-S)

Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit		Min	Typ	Max	Unit
STATIC							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA V_{GS}=0V, I_D=-250μA	N-Ch P-Ch	30 -30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA V_{DS}=V_{GS}, I_D=-250μA	N-Ch P-Ch	1.0 -1.0		2.5 -2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V V_{DS}=0V, V_{GS}=±20V	N-Ch P-Ch			±100 ±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V V_{DS}=-24V, V_{GS}=0V	N-Ch P-Ch			1 -1	μA
$R_{DS(ON)}$	Drain-Source on-State Resistance[a]	V_{GS}=10V, I_D=8.1A V_{GS}=-10V, I_D= -7.1A	N-Ch P-Ch		15 17	18 20	mΩ
		VGS=4.5V, ID=6A VGS=-4.5V, ID=-5.6A	N-Ch P-Ch		21 21	29 29	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V I_S=-1A, V_{GS}=0V	N-Ch P-Ch		0.75 -0.7	1 -1	V
DYNAMIC							
Qg	Total Gate Charge	N-Channel V_{DS}=15V,V_{GS}=10V,I_D=8.1A P-Channel V_{DS}=-15V,V_{GS}=-10V,I_D=-7.1A	N-Ch P-Ch		16.6 31.7		nC
Qgs	Gate-Source Charge		N-Ch P-Ch		3.8 5.6		
Qgd	Gate-Drain Charge		N-Ch P-Ch		3.4 6.3		
Ciss	Input Capacitance	N-Channel V_{DS}=15V, V_{GS}=0V, f=1MHz P-Channel VDS=-15V,VGS=0V, f=1MHz	N-Ch P-Ch		502 892		pF
Coss	Output Capacitance		N-Ch P-Ch		81 188		
Crss	Reverse Transfer Capacitance		N-Ch P-Ch		59 133		
$t_{d(on)}$	Turn-On Delay Time	N-Channel VDD=25V, RL =25Ω ID=1A, VGS=10V, RG=6Ω P-Channel VDD=-15V, RL =15Ω ID=-1A, VGS=-10V, RG=6Ω	N-Ch P-Ch		11.1 43.4		ns
t_r	Turn-On Rise Time		N-Ch P-Ch		9.8 21.1		
$t_{d(off)}$	Turn-Off Delay Time		N-Ch P-Ch		32.9 92.6		
t_f	Turn-Off Fall Time		N-Ch P-Ch		4.5 20		

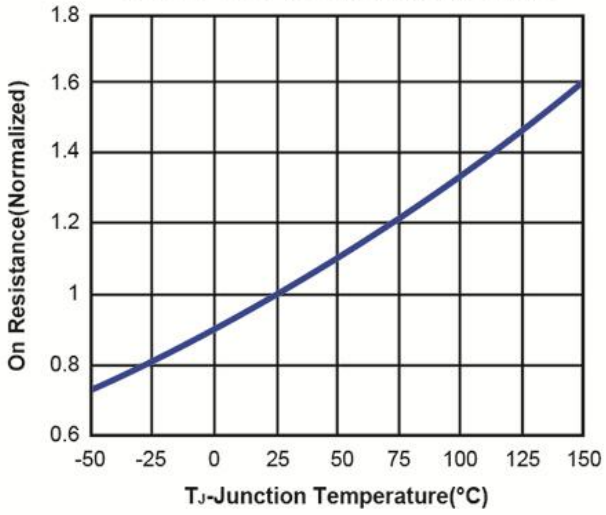
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

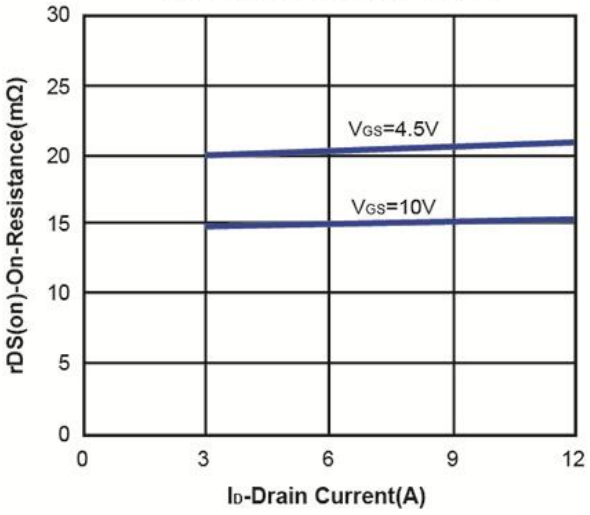
Dual N- and P-Channel 30-V (D-S)

Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

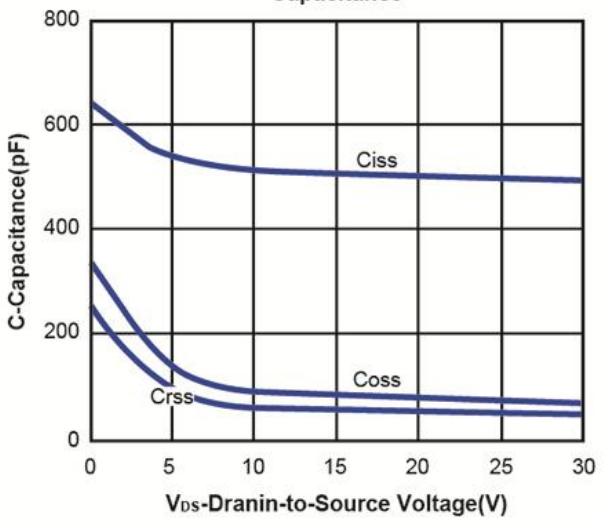
On Resistance vs. Junction Temperature



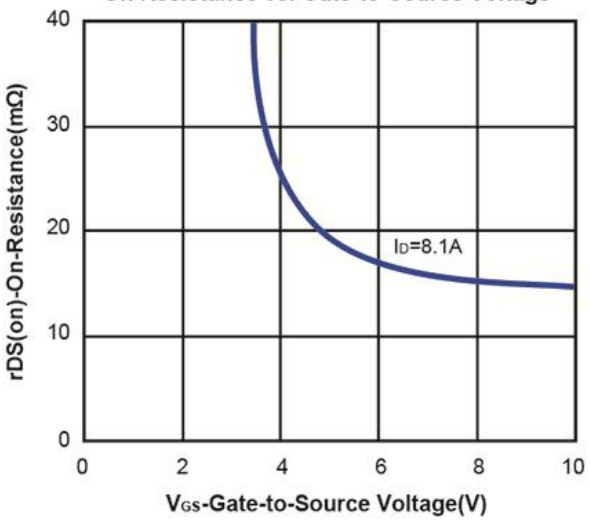
On Resistance vs. Drain Current



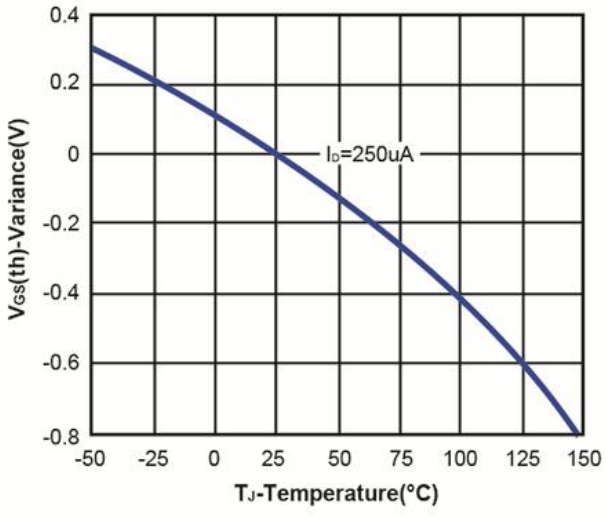
Capacitance



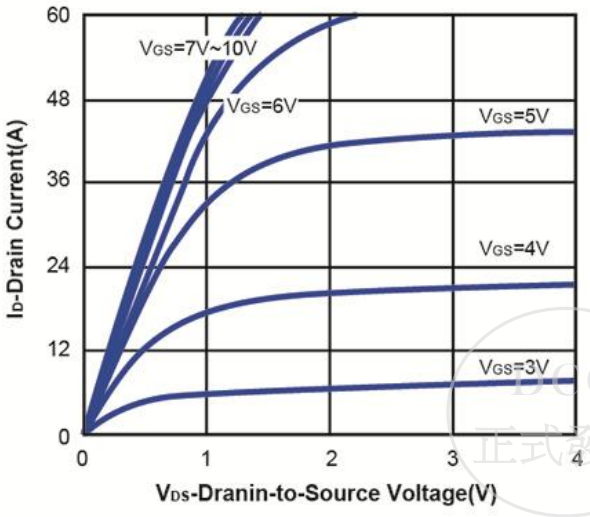
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



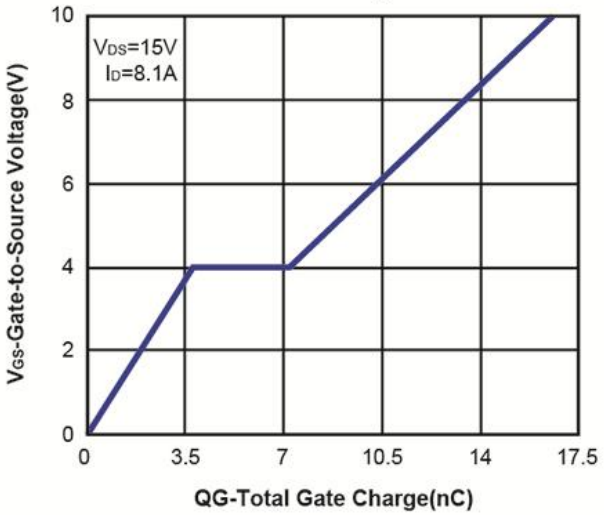
On-Region Characteristics



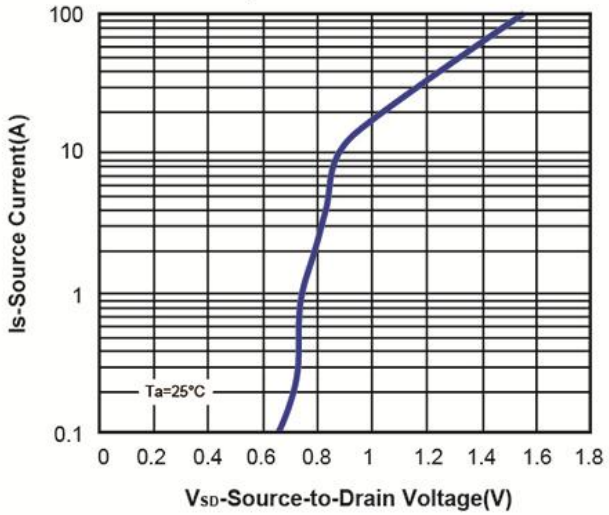
Dual N- and P-Channel 30-V (D-S)

Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

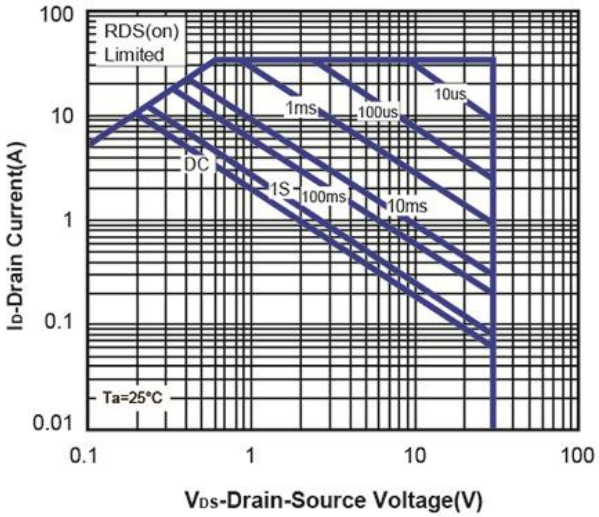
Gate Charge



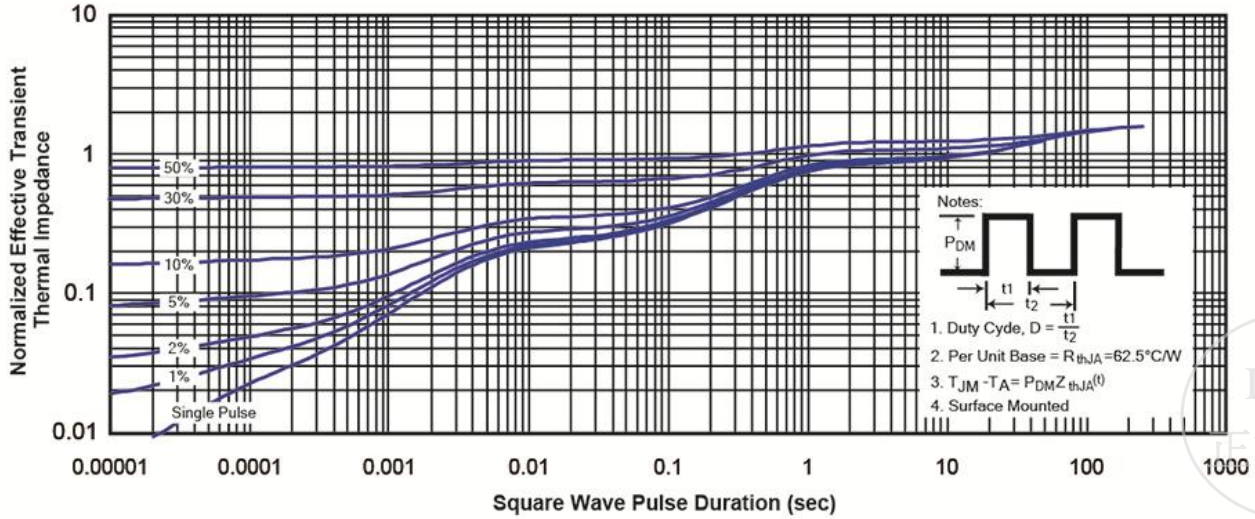
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



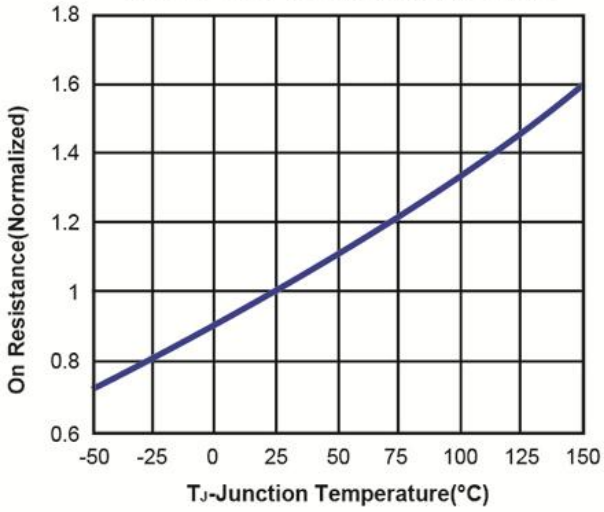
Normalized Thermal Transient Impedance, Junction-to-Ambient



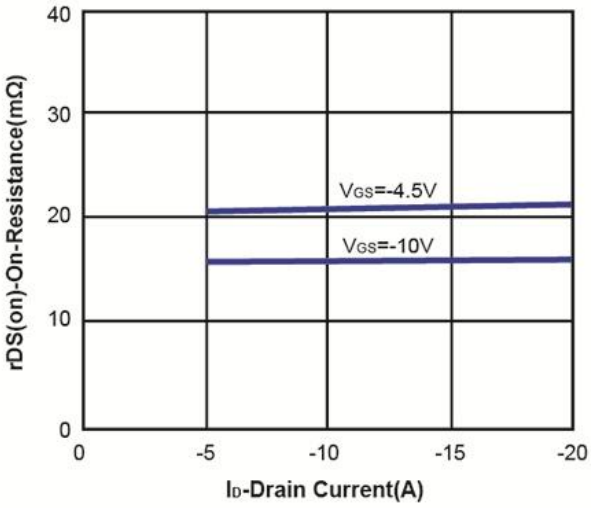
Dual N- and P-Channel 30-V (D-S)

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

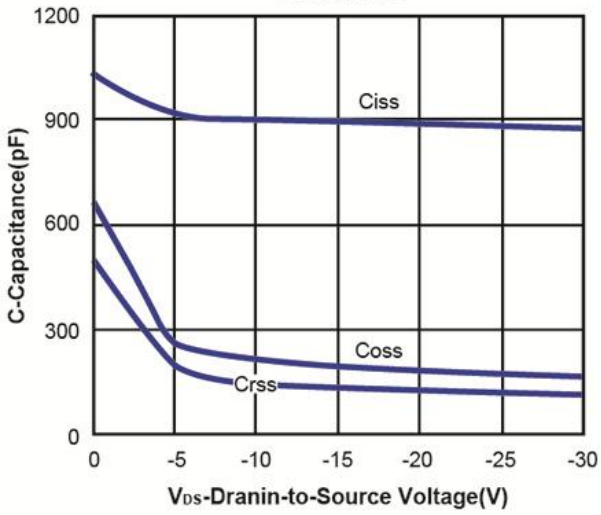
On Resistance vs. Junction Temperature



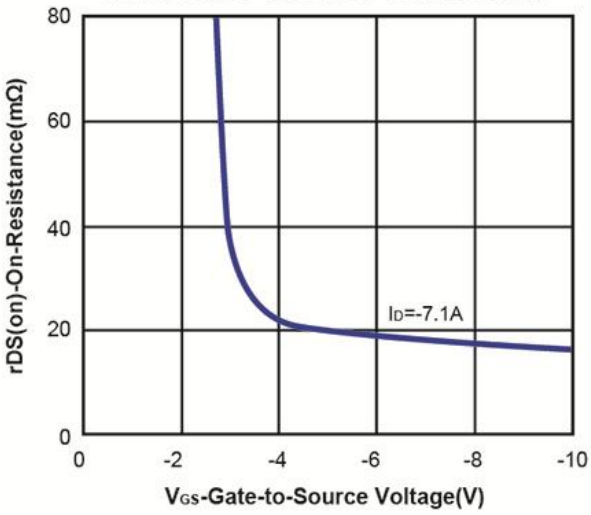
On Resistance vs. Drain Current



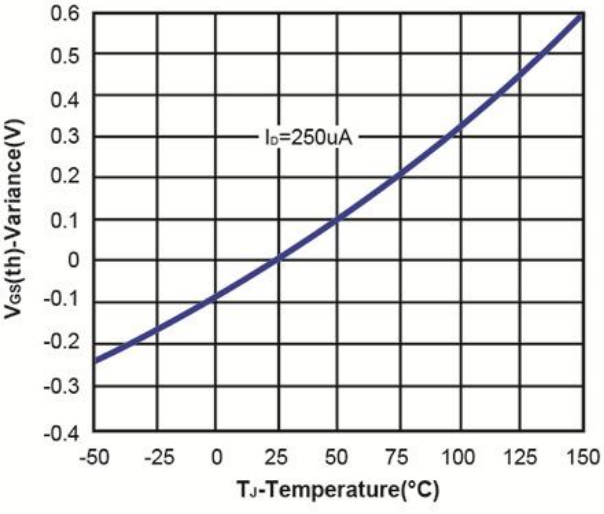
Capacitance



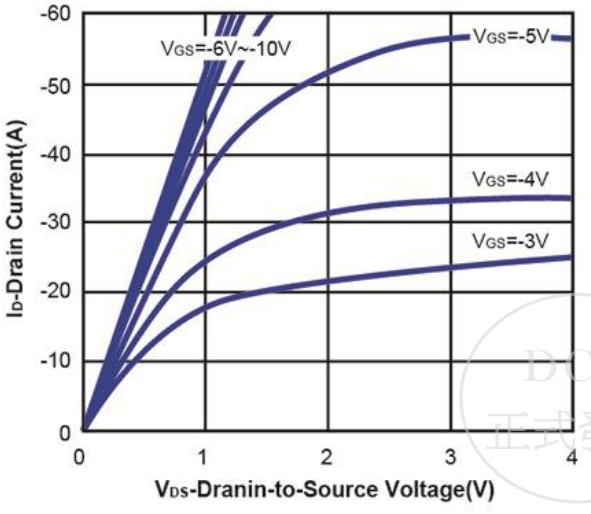
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



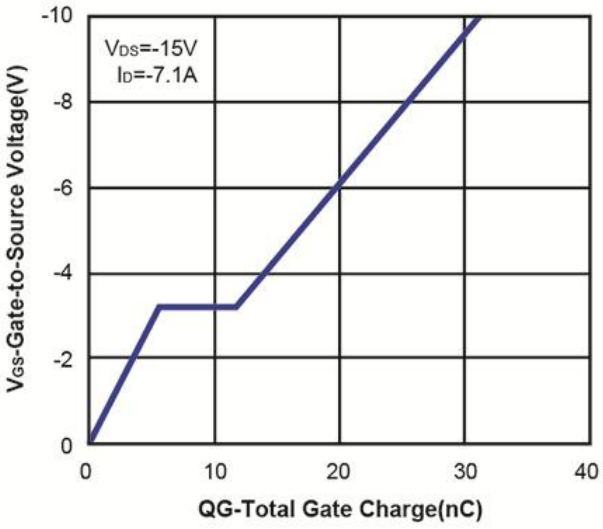
On-Region Characteristics



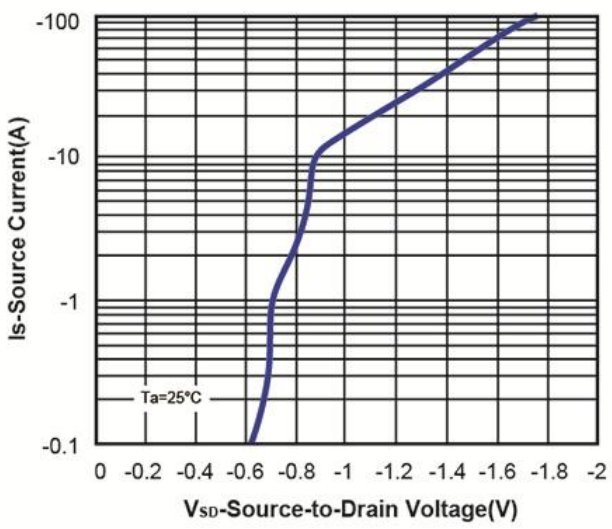
Dual N- and P-Channel 30-V (D-S)

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

Gate Charge



Body-diode characteristics



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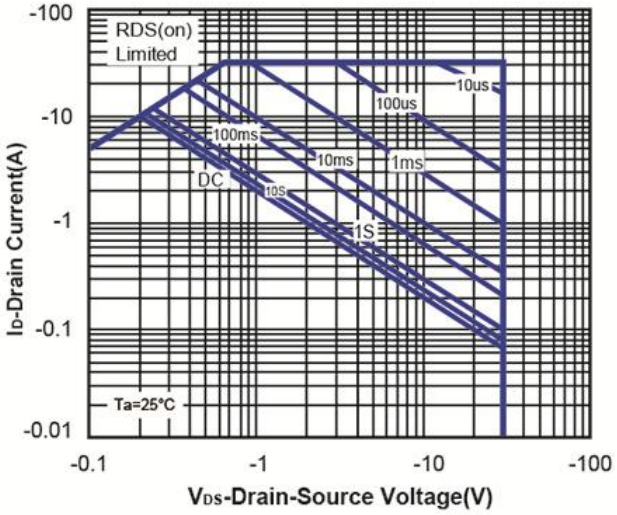

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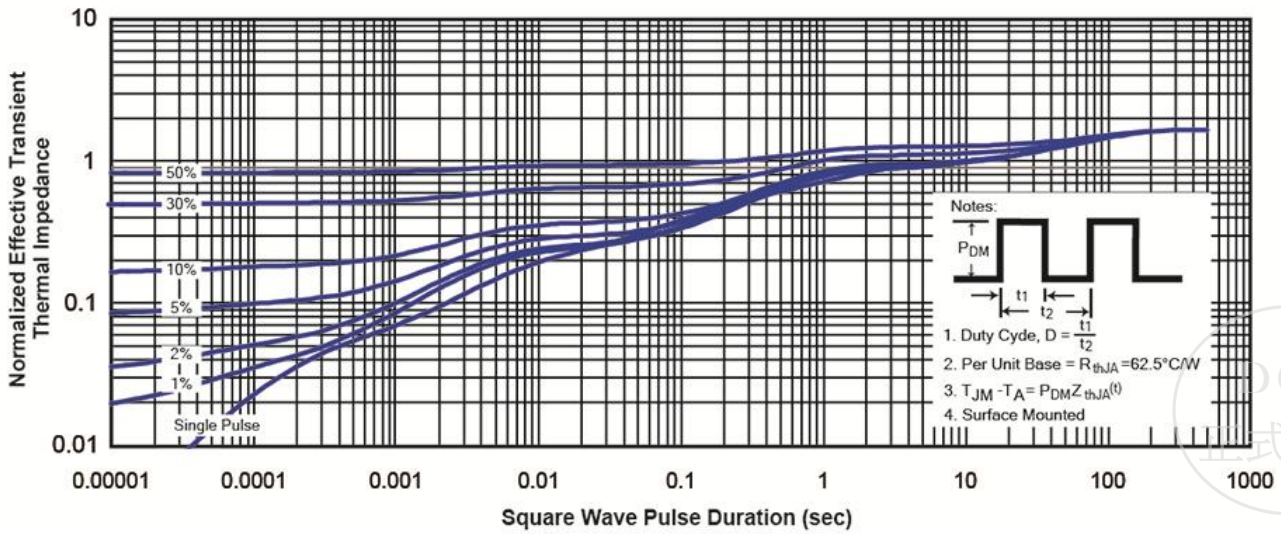
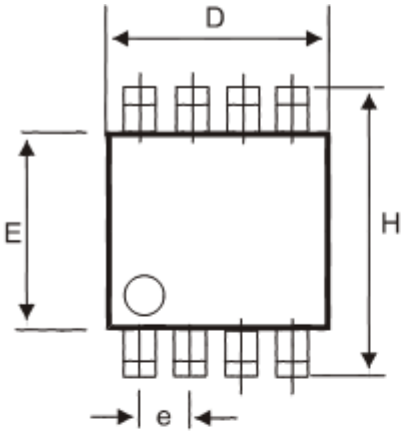
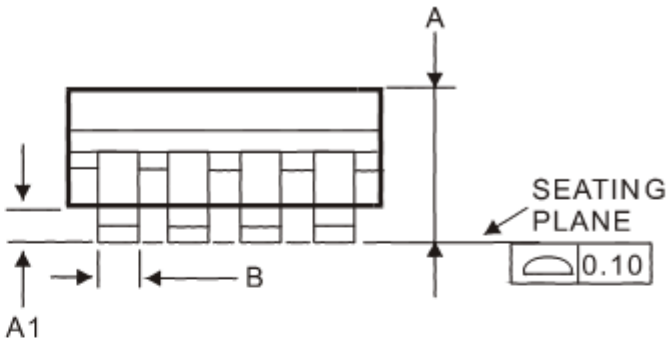
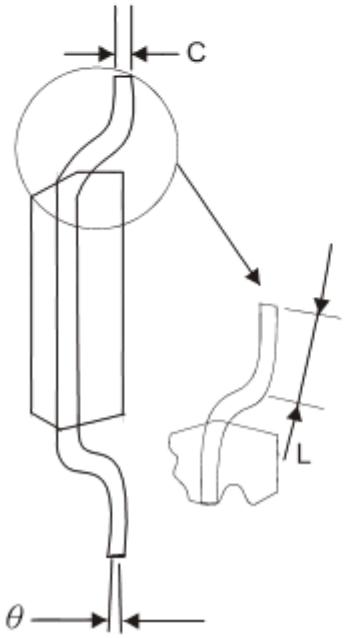


SOP-8 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.