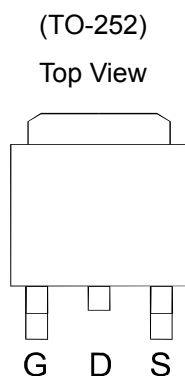


P- Channel 40-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME45P04-G is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

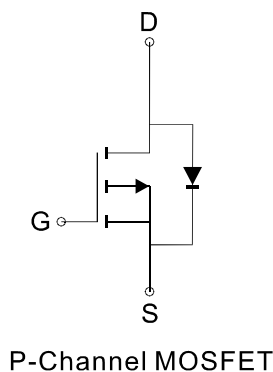


FEATURES

- $R_{DS(ON)} \leq 18m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 25m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter



Ordering Information: ME45P04 (Pb-free)
ME45P04-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current*	Tc=25°C	I_D	-30	A
	Tc=70°C		-23	
Pulsed Drain Current		I_{DM}	-120	A
Maximum Power Dissipation*	Tc=25°C	P_D	25	W
	Tc=70°C		16	
Operating Junction Temperature		T_J	-55 to 150	°C
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	5	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper

P- Channel 40-V (D-S) MOSFET

Electrical Characteristics (T_c =25°C Unless Otherwise Specified)

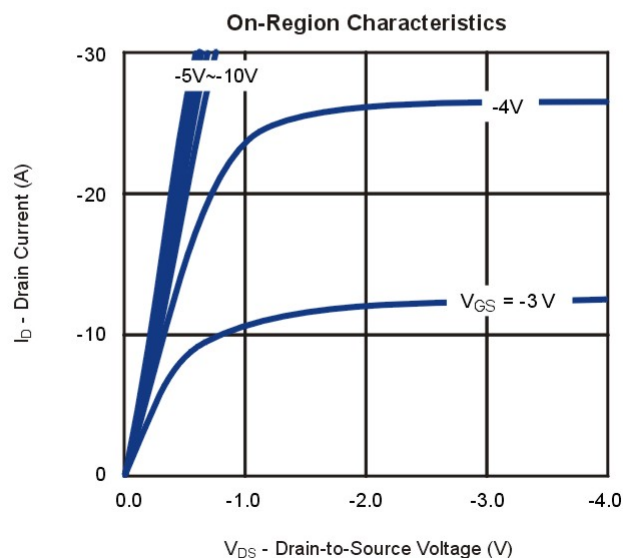
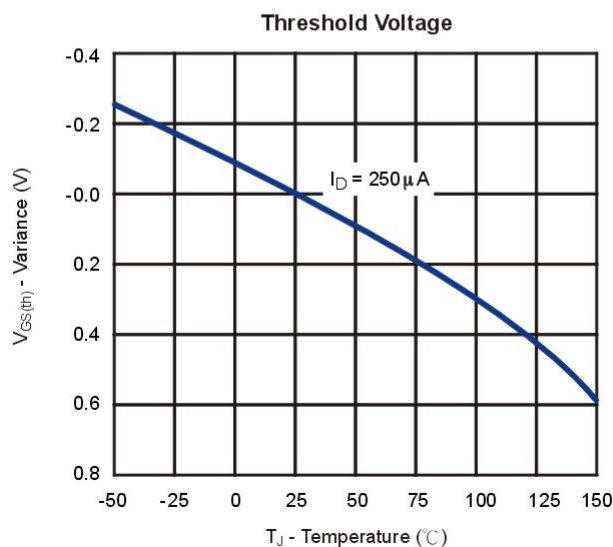
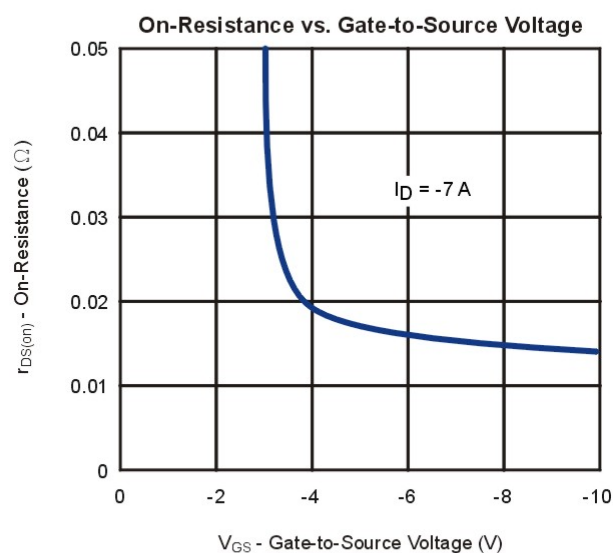
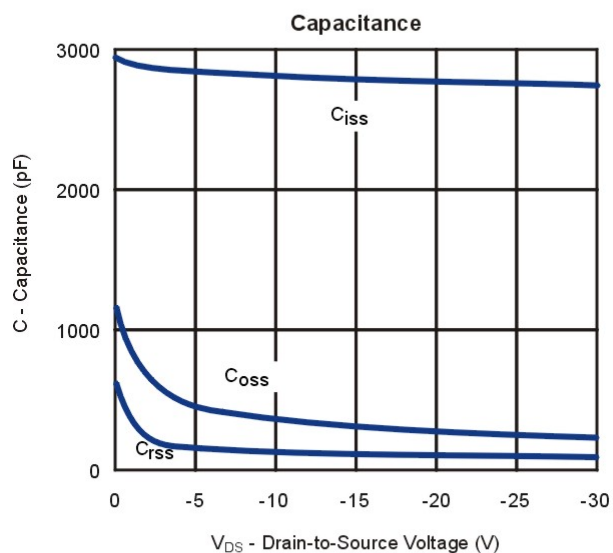
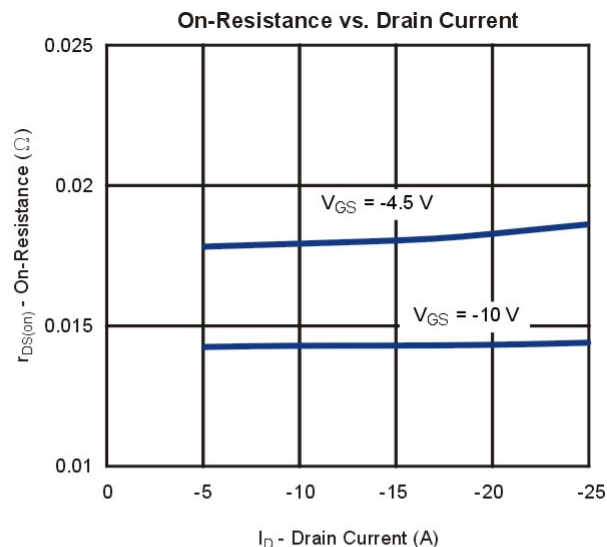
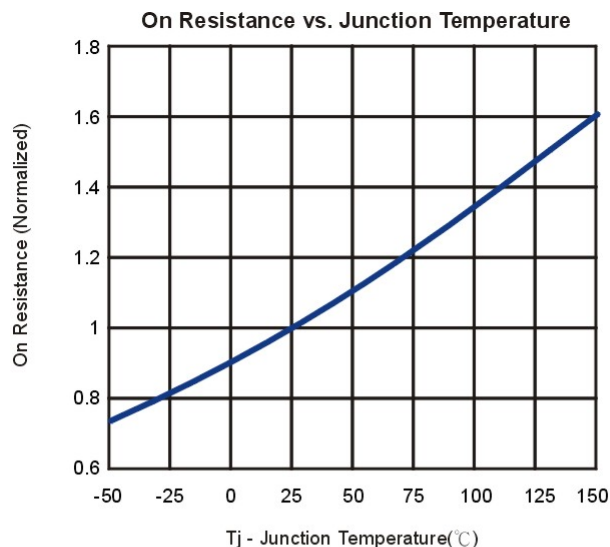
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-40			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1.5		-3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-40V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =-10V, I _D = -12A		15	18	mΩ
		V _{GS} =-4.5V, I _D = -6A		18	25	
V _{SD}	Diode Forward Voltage	I _S =-1.7A, V _{GS} =0V		-0.78	-1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-20V, V _{GS} =-4.5V, I _D =-12A		25		nC
Q _{gs}	Gate-Source Charge			11		
Q _{gd}	Gate-Drain Charge			9.5		
C _{iss}	Input capacitance	V _{DS} =-20V, V _{GS} =0V, F=1MHz		2760		pF
C _{oss}	Output Capacitance			260		
C _{rss}	Reverse Transfer Capacitance			85		
t _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, R _L =15Ω I _D =-1A, V _{GEN} =-10V, R _G =6Ω		48		ns
t _r	Turn-On Rise Time			24		
t _{d(off)}	Turn-Off Delay Time			88		
t _f	Turn-On Fall Time			34		

Notes:a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

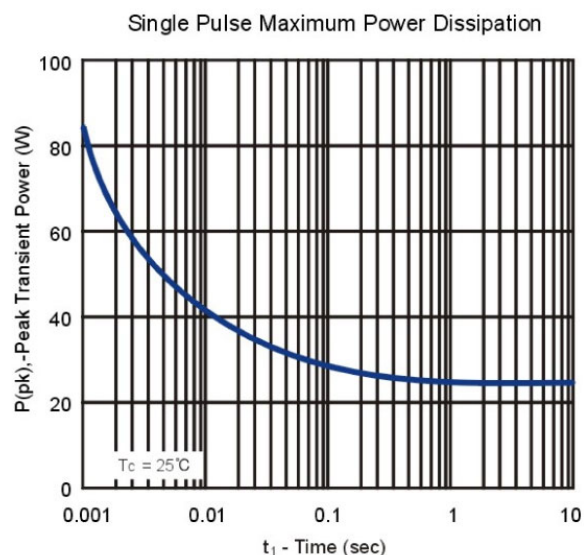
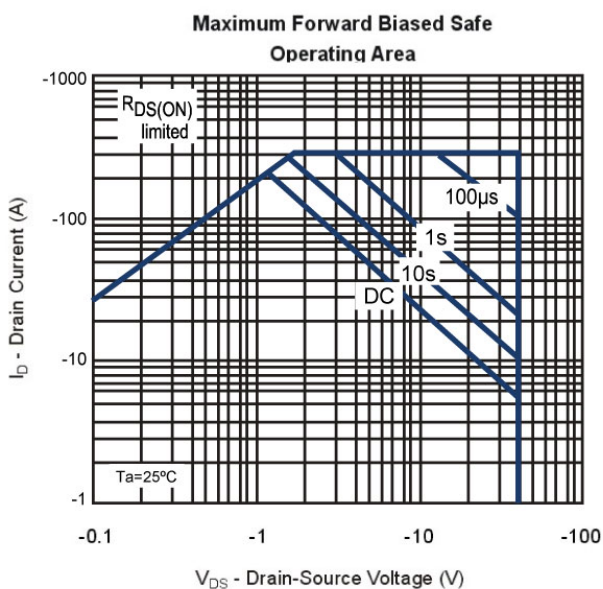
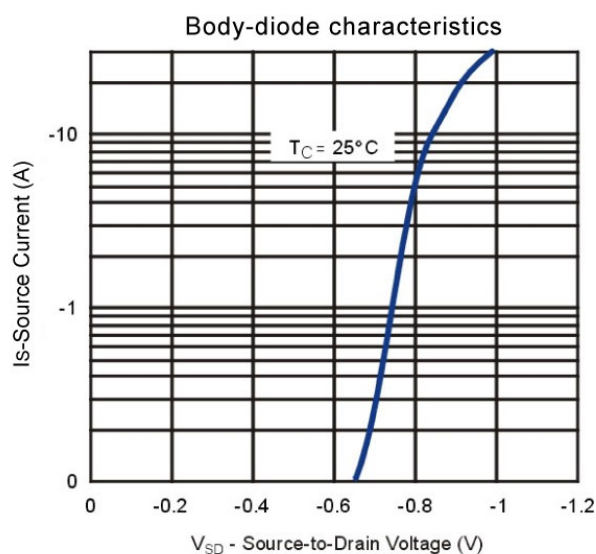
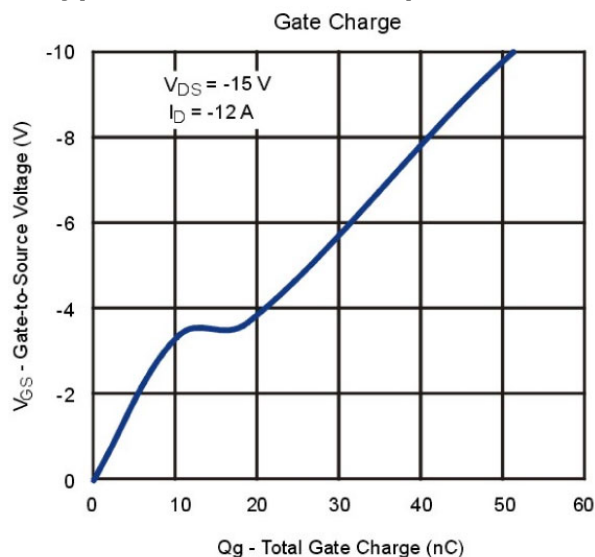
P- Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)

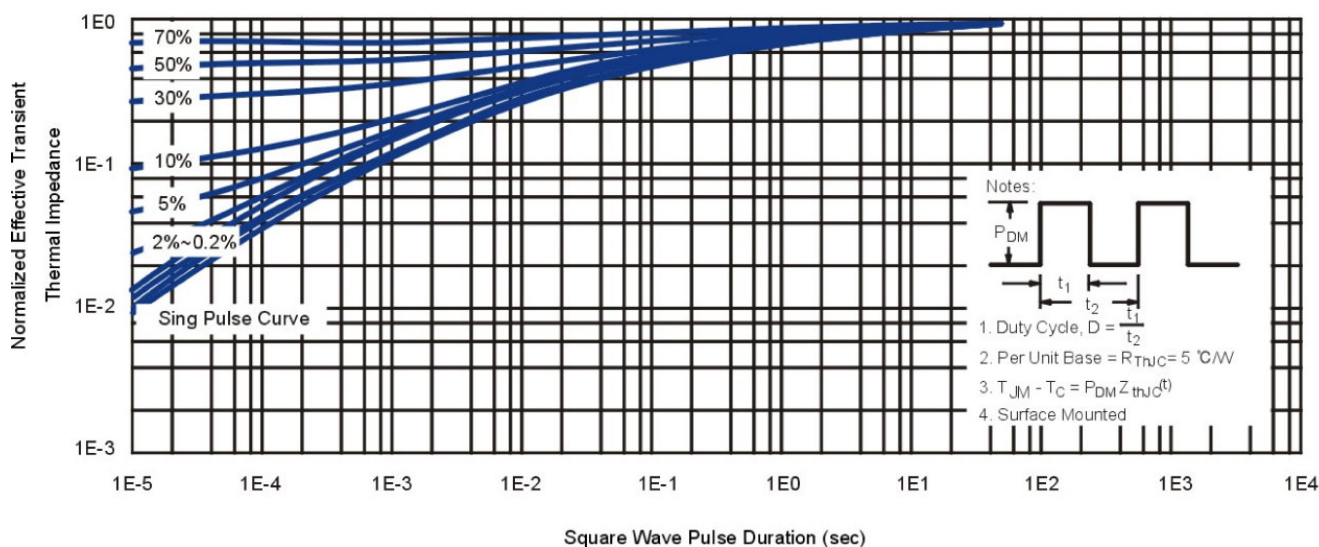


P- Channel 40-V (D-S) MOSFET

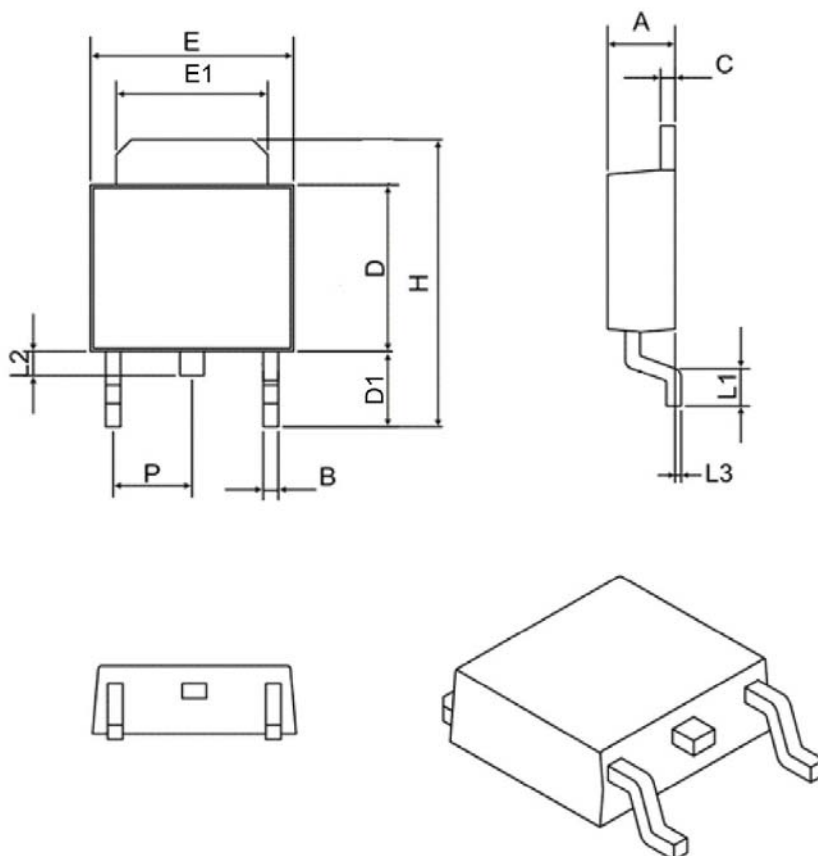
Typical Characteristics (T_J = 25°C Noted)



Normalized Thermal Transient Impedance, Junction-to-Case



TO-252 Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	