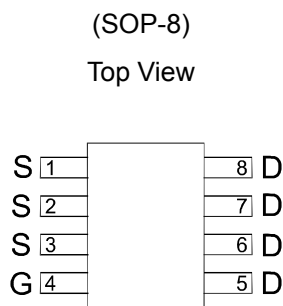


GENERAL DESCRIPTION

The ME4812 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology integrated Schottky diode. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

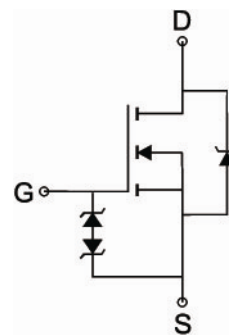


FEATURES

- Integrated Schottky diode
- $R_{DS(ON)} \leq 13m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 21.5m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Battery Powered System
- DC/DC Converter low side switching
- Load Switch



Ordering Information: ME4812 (Pb-free)

ME4812-G (Green product- Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J = 150^\circ C$)*	I_D	$T_A = 25^\circ C$	11.3
		$T_A = 70^\circ C$	8.9
Pulsed Drain Current	I_{DM}	45	A
Maximum Power Dissipation*	P_D	$T_A = 25^\circ C$	2.5
		$T_A = 70^\circ C$	1.6
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	50	$^\circ C/W$

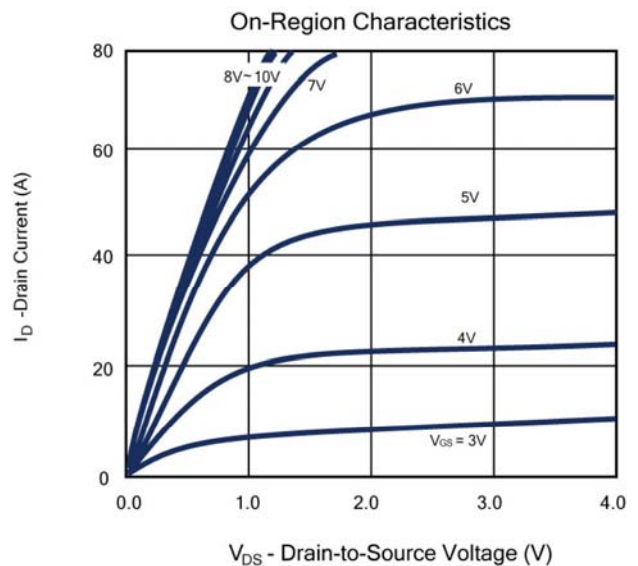
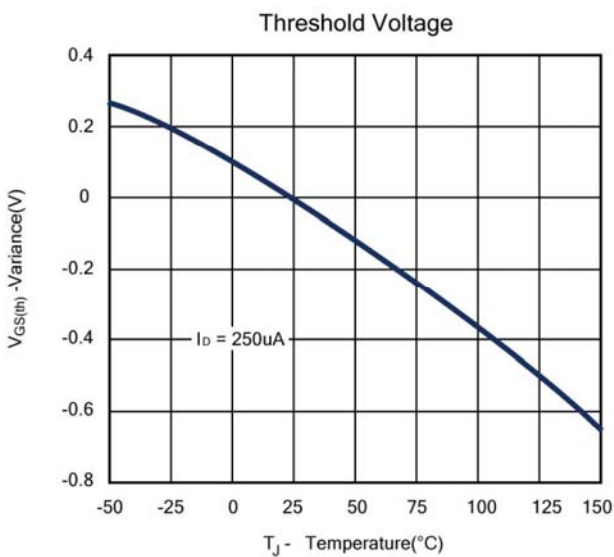
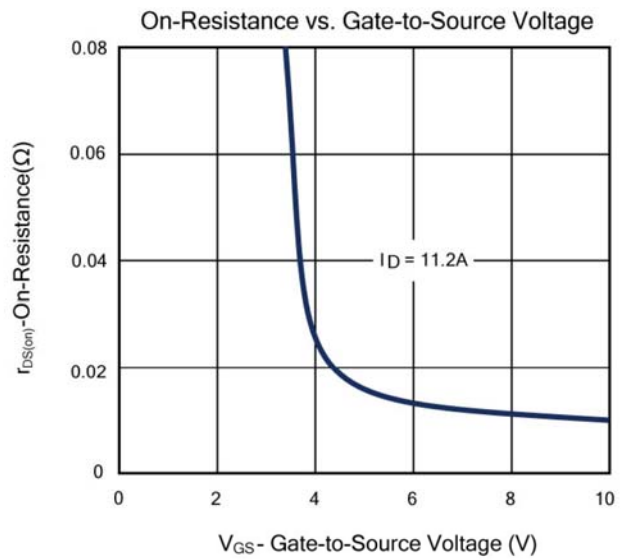
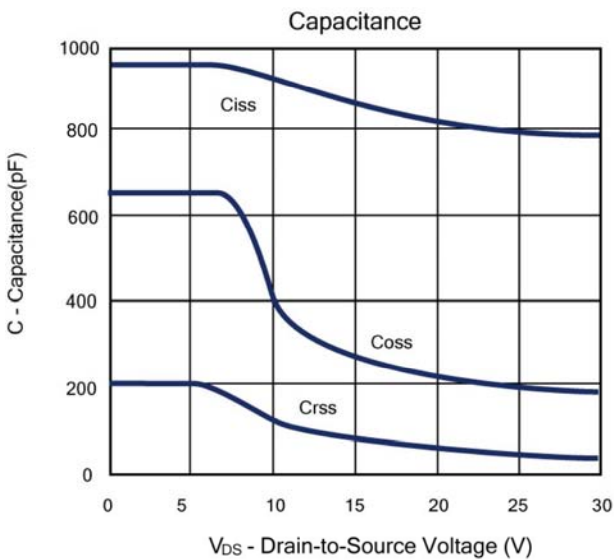
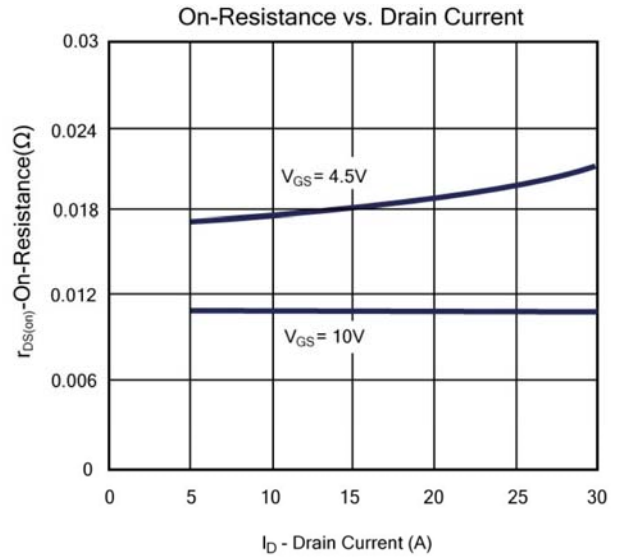
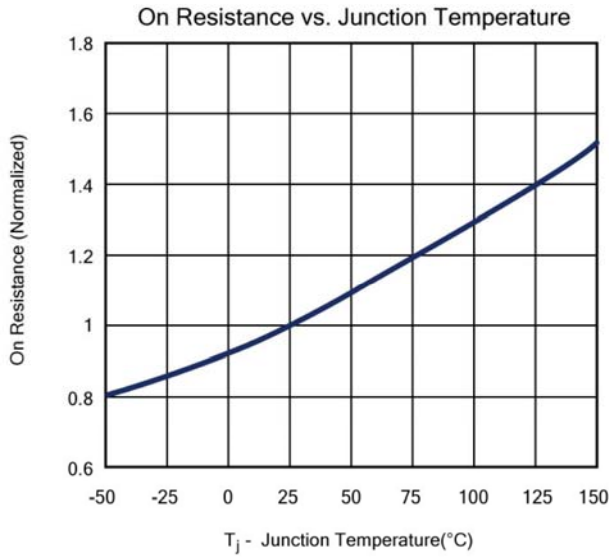
* The device mounted on 1in² FR4 board with 2 oz copper

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±16V			±10	μA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			1	mA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D = 11.2A		10	13	mΩ
		V _{GS} =4.5V, I _D = 10A		17.5	21.5	
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.4	0.5	V
DYNAMIC						
Q _g	Total Gate Charge(10V)	V _{DS} =15V, V _{GS} =10V, I _D =11.2A		19		nC
Q _g	Total Gate Charge(4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =11.2A		9.7		
Q _{gs}	Gate-Source Charge			4.2		
Q _{gd}	Gate-Drain Charge			4.6		
C _{iss}	Input capacitance	V _{DS} =15V, V _{GS} =0V, f=1.0MHz		830		pF
C _{oss}	Output Capacitance			280		
C _{rss}	Reverse Transfer Capacitance			84		
R _g	Gate-Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		1		Ω
t _{d(on)}	Turn-On Delay Time	V _{DD} =15V, R _L =15Ω I _D =1A, V _{GEN} =10V R _G =3Ω		14		ns
t _r	Turn-On Rise Time			14		
t _{d(off)}	Turn-Off Delay Time			39		
t _f	Turn-Off Fall Time			4		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

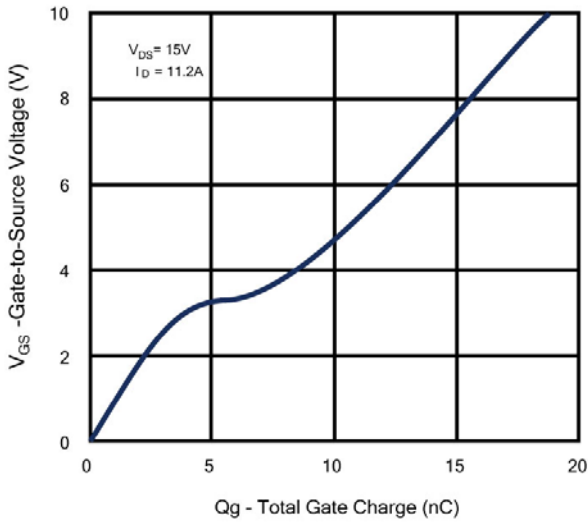
b. Matsuki reserves the right to improve product design, functions and reliability without notice.

Typical Characteristics (T_J = 25°C Noted)

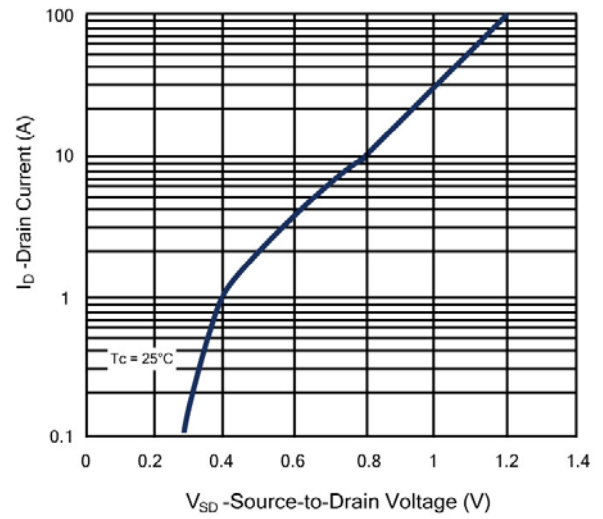


Typical Characteristics (T_J = 25°C Noted)

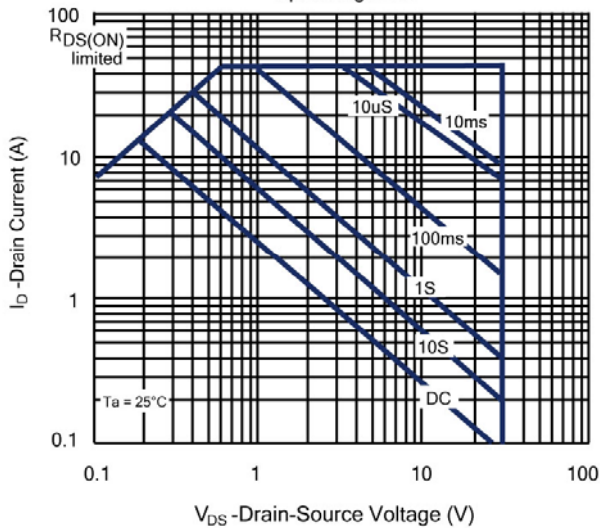
Gate Charge



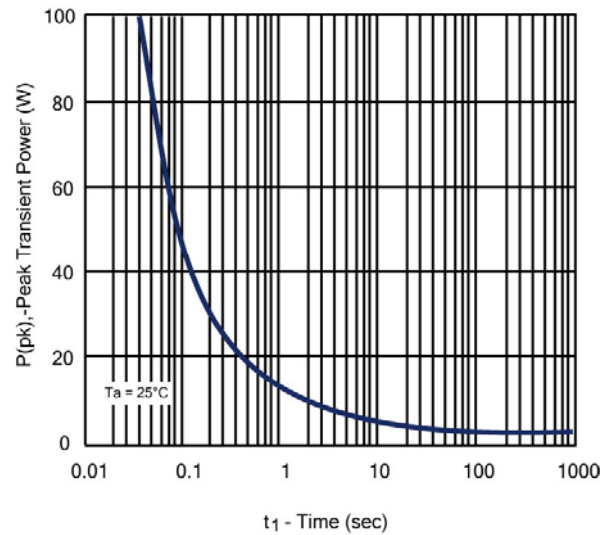
On-Resistance vs. Drain Current



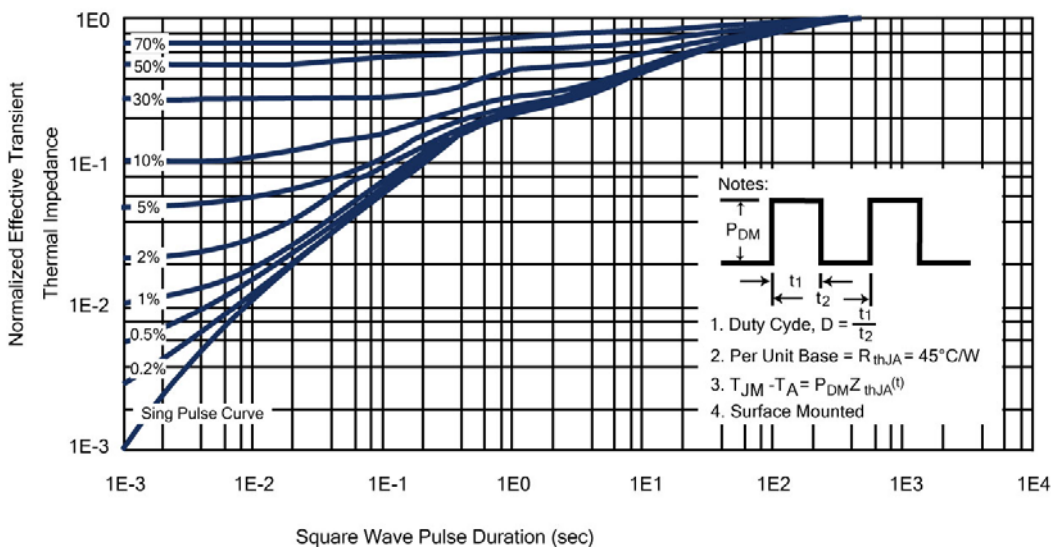
Maximum Forward Biased Safe Operating Area



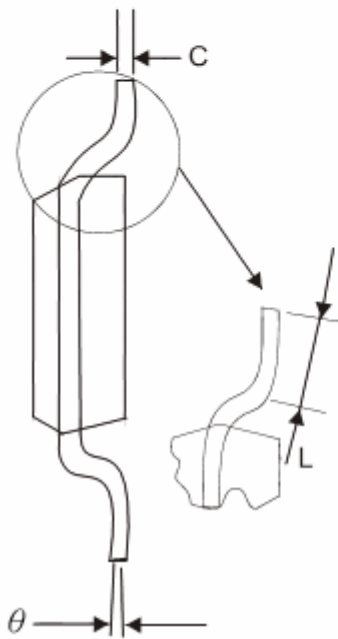
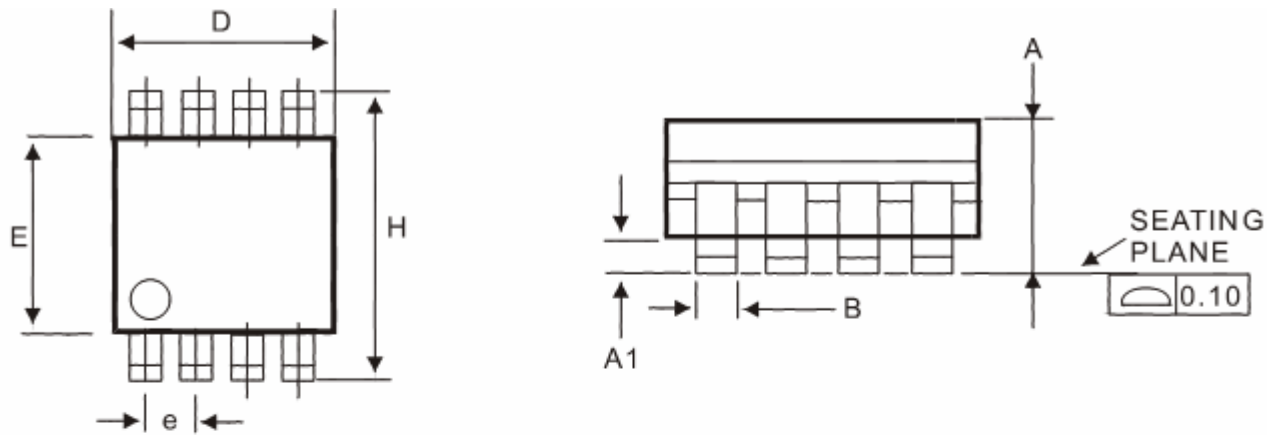
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.