ME4812B/ME4812B-G

N-Channel 30-V (D-S) MOSFET Integrated Schottky Diode

GENERAL DESCRIPTION

The ME4812B is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 12m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 21m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

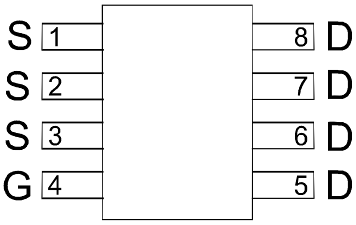
APPLICATIONS

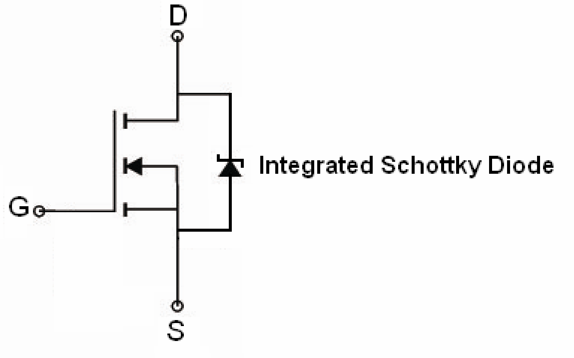
- Power Management in Note book
- Battery Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

(SOP-8)

Top View





N-Channel MOSFET

Ordering Information: ME4812B (Pb-free)

ME4812B-G (Green product- Halogen free)

Absolute Maximum Ratings (TA=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J =150℃)*	T_A=25℃	I_D	11.4	A
	T_A=70℃		9.1	
Pulsed Drain Current		I_{DM}	46	A
Maximum Power Dissipation*	T_A=25℃	P_D	2.5	W
	T_A=70℃		1.6	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	50	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

N-Channel 30-V (D-S) MOSFET Integrated Schottky Diode

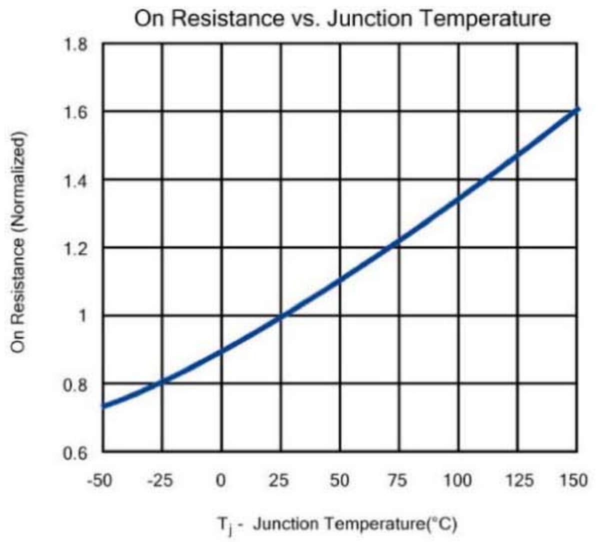
Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

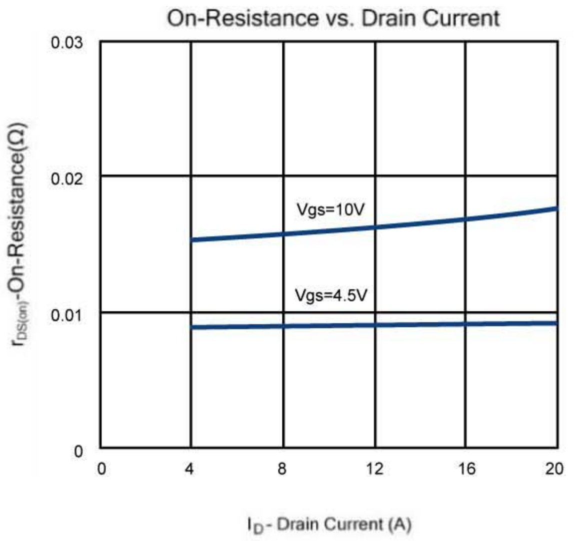
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			0.1	mA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=10V, I_D= 11.2A		9.5	12	mΩ
		V_{GS}=4.5V, I_D= 8A		16	21	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.47	0.55	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=11.2A		21		nC
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=11.2A		11		
Qgs	Gate-Source Charge			5.0		
Qgd	Gate-Drain Charge			4.6		
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1.0MHz		865		pF
Coss	Output Capacitance			295		
Crss	Reverse Transfer Capacitance			153		
Rg	Gate-Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		0.6		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L =15Ω, I=1A, V_{GEN}=10V, R_G=3Ω		15		ns
t_r	Turn-On Rise Time			14		
$t_{d(off)}$	Turn-Off Delay Time			41		
t_f	Turn-Off Fall Time			4		

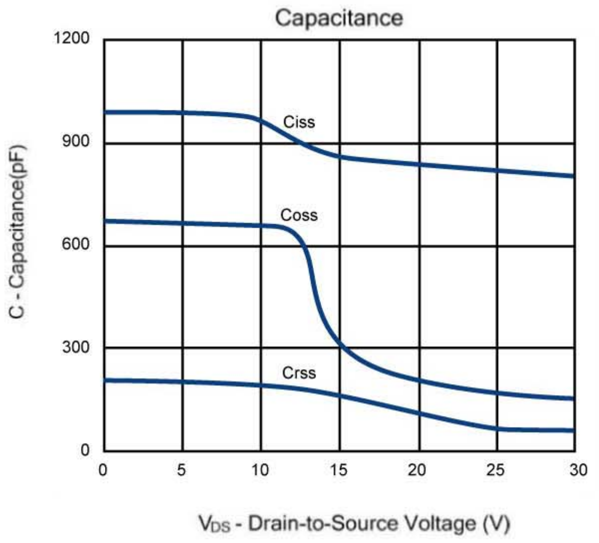
Notes: a. pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

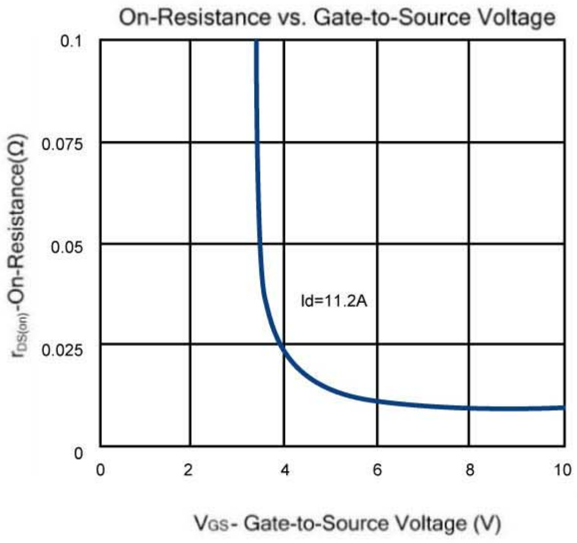
b. Matsuki reserves the right to improve product design, functions and reliability without notice.

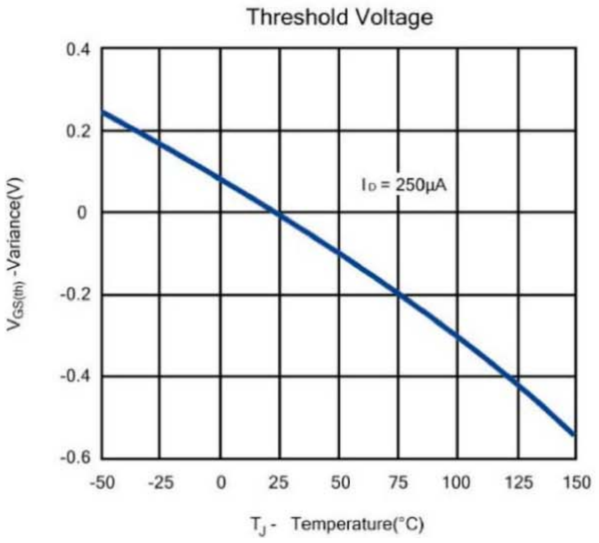
Typical Characteristics (T_J =25℃ Noted)

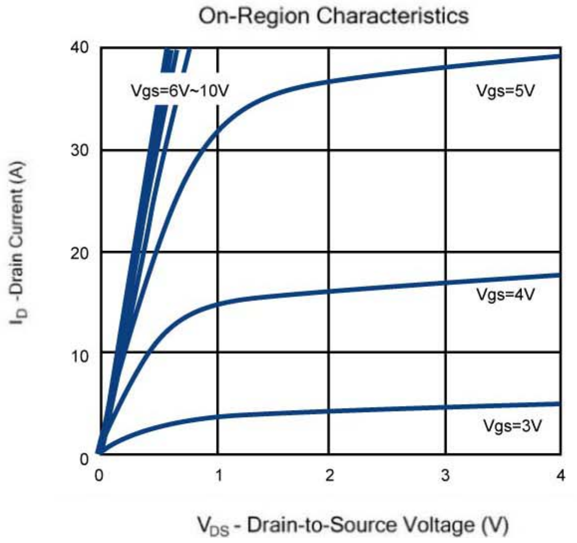












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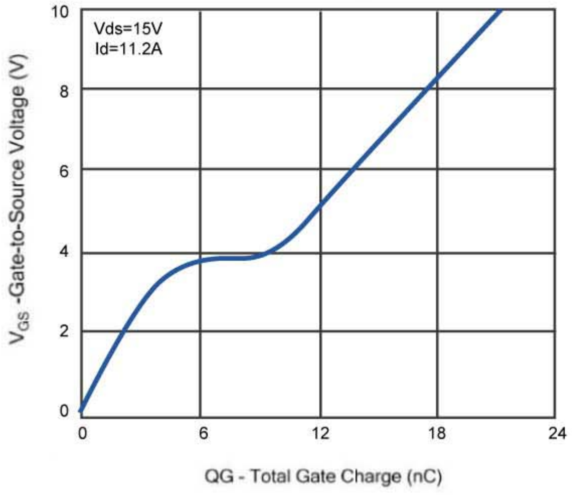
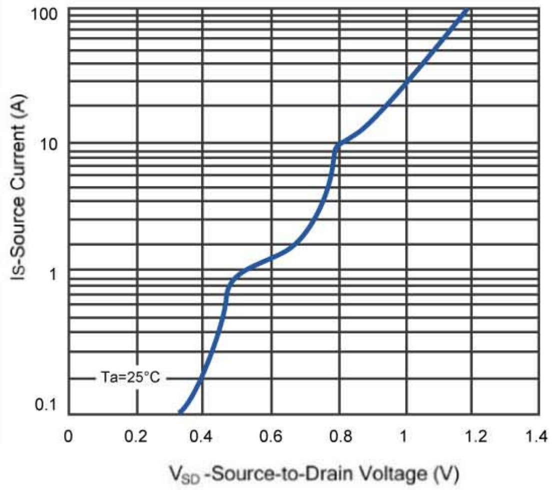
Typical Characteristics (TJ =25℃ Noted)

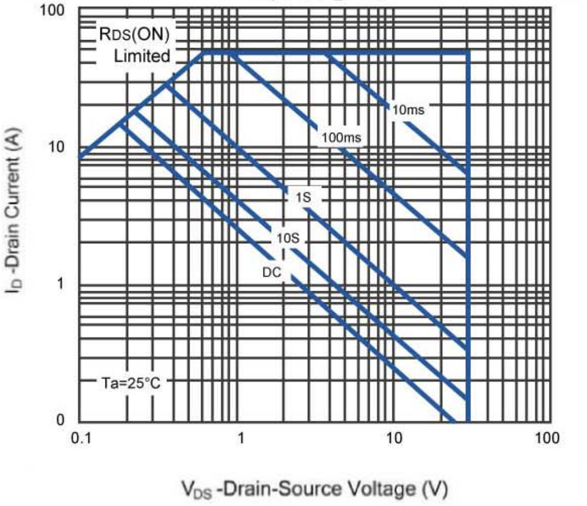
Gate Charge



Body-diode characteristics

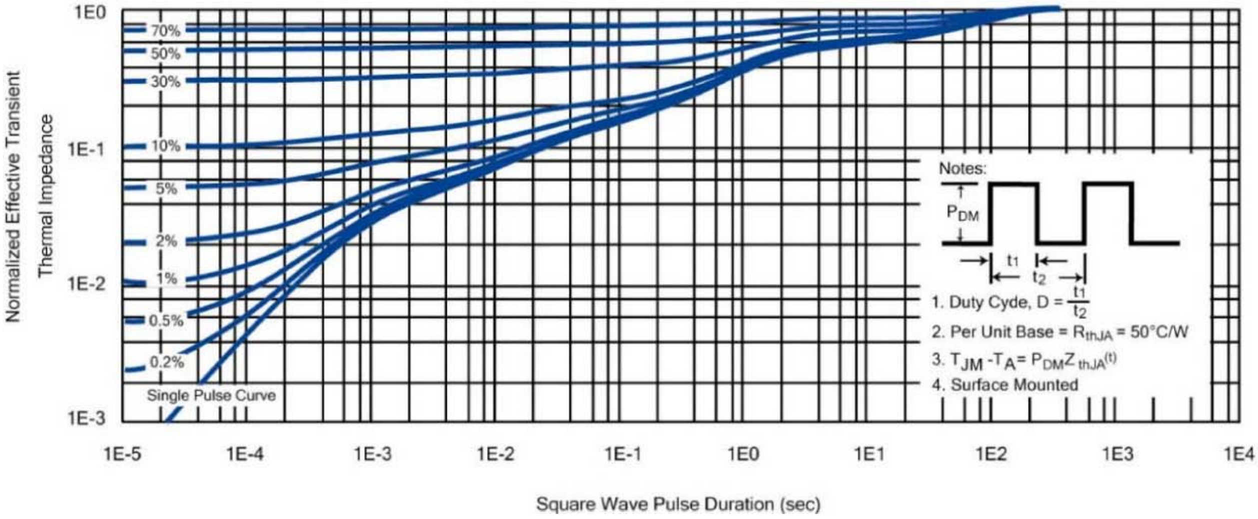


Maximum Forward Biased Safe Operating Area

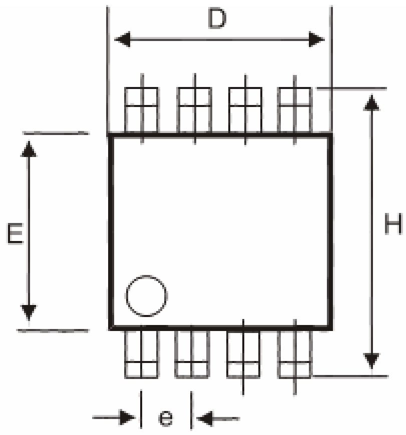


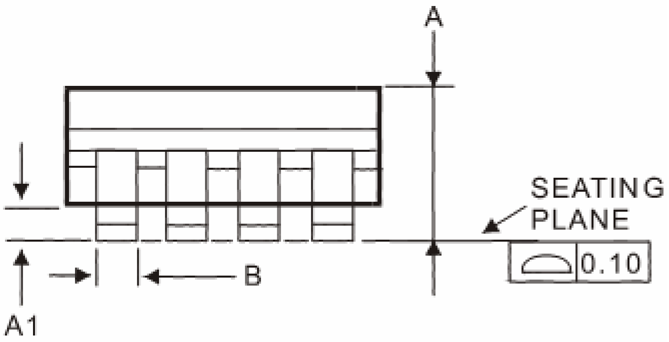
Single Pulse Maximum Power Dissipation

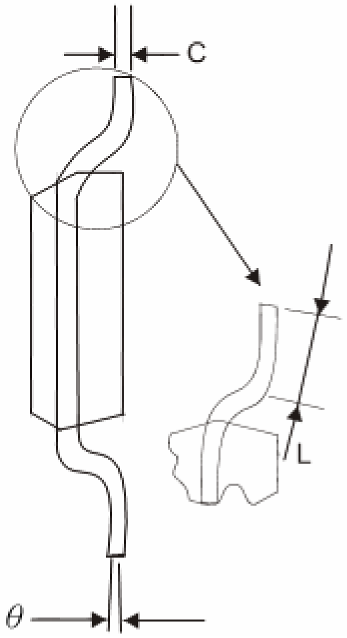
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°