N-Channel 30-V(D-S) MOSFET

GENERAL DESCRIPTION

The ME4856 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 6m\Omega @V_{GS}=10V$
- $R_{DS(ON)} \leqq 8.5m\Omega @V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

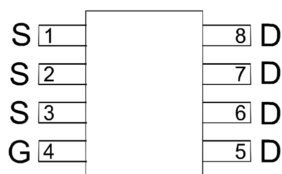
APPLICATIONS

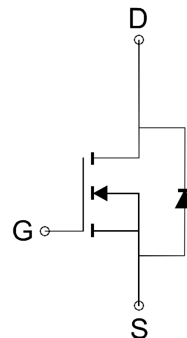
- Power Management in Note book
- Battery Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

(SOP-8)

Top View





N-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit		Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current(T_J =150℃)	T_A=25℃	I_D	17		A
	T_A=70℃		14		
Pulsed Drain Current		I_{DM}	50		A
Continuous Source Current (Diode Conduction)		I_S	2.7		A
Pulse Source-Drain Diode Current		I_{SM}	50		A
Maximum Power Dissipation	T_A=25℃	P_D	3.0		W
	T_A=70℃		2.0		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	T≦10 sec	30	℃/W
			Steady State	60	
thermal Resistance-Junction to Case		$R_{\theta JC}$	34		℃/W

* The device mounted on $1in^2$ FR4 board with 2 oz copper

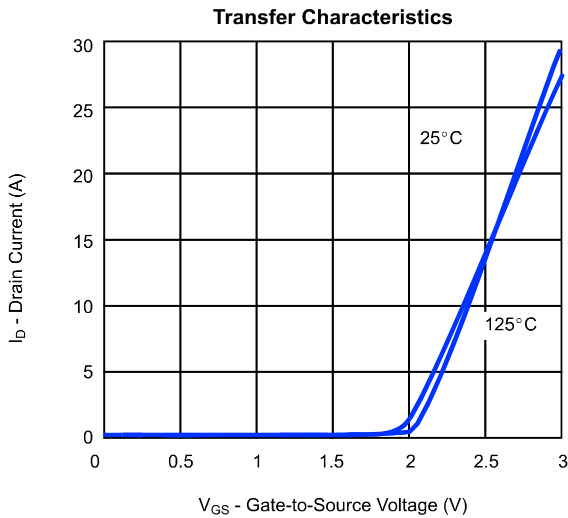
N-Channel 30-V(D-S) MOSFET

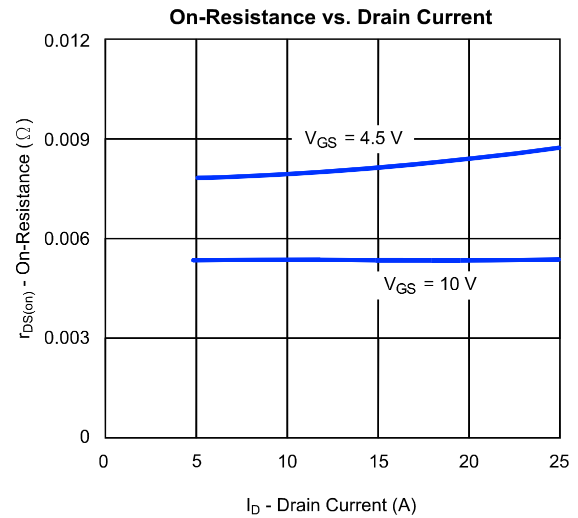
Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

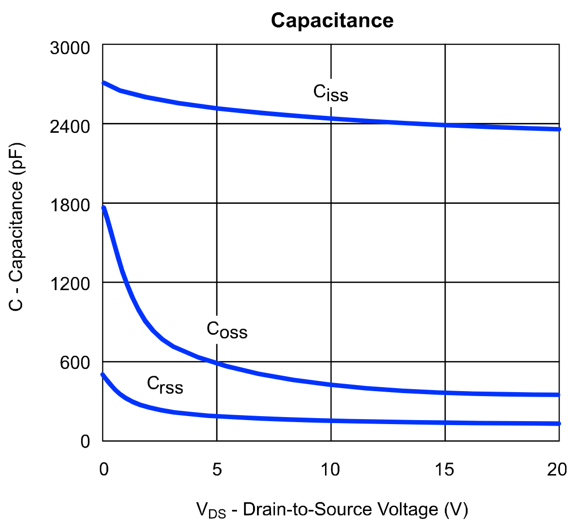
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250 μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250 μA	1.3	1.8	3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		V_{DS}=30V, V_{GS}=0V T_J=70℃			5	
$I_{D(ON)}$	On-State Drain Current [a]	V_{DS}≧5V, V_{GS}= 10V	40			A
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=10V, I_D= 10A		4.5	6	mΩ
		V_{GS}=4.5V, I_D= 7.5A		6.5	8.5	
G_{FS}	Forward Transconductance [a]	V_{DS}=15V, I_D=17A		14		S
V_{SD}	Diode Forward Voltage	I_S=2.7A, V_{GS}=0V		0.72	1.1	V
DYNAMIC						
Qg	Total Gate Charge(4.5V)	V_{DS}=15V, V_{GS}=4.5V, I_D=17A		55	60	nC
Qg	Total Gate Charge(10V)	V_{DS}=15V, V_{GS}=10V, I_D=17A		29		
Qgs	Gate-Source Charge			10		
Qgd	Gate-Drain Charge			15		
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1.0MHz		2400	2700	pF
Coss	Output Capacitance			350		
Crss	Reverse Transfer Capacitance			110		
Rg	Gate-Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz	0.7	1.2	2.0	Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L =15Ω I_D=1A, V_{GEN}=10V R_G=6Ω		23	30	ns
t_r	Turn-On Rise Time			12	16	
$t_{d(off)}$	Turn-Off Delay Time			86	111	
t_f	Turn-Off Fall Time			12	16	
trr	Source-Drain Reverse Recovery Time	I_F=2.7A, di/dt=100A/μs		40	60	
Qrr	Body diode Reverse Recovery charge	I_F=2.9A, di/dt=100A/μs		36	60	nC

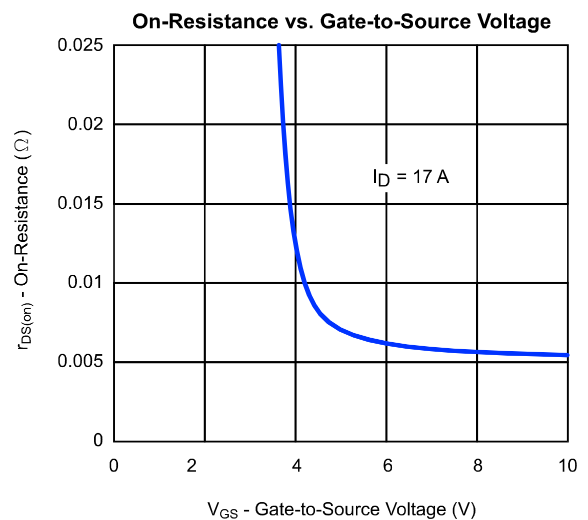
Note: a: Pulse test: pulse width<=300us, duty cycle<=2%

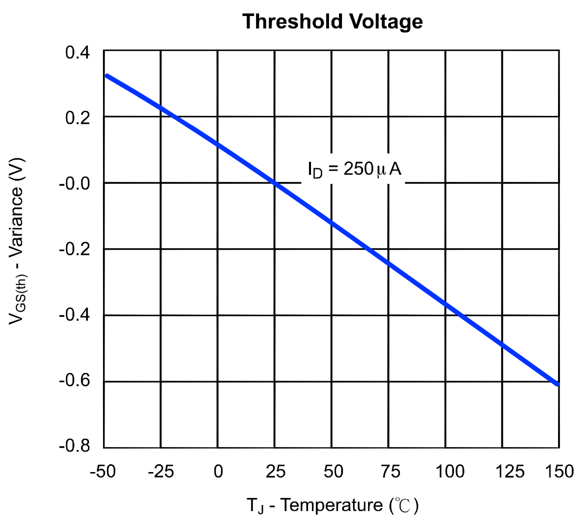
Typical Characteristics (TJ =25℃ Noted)

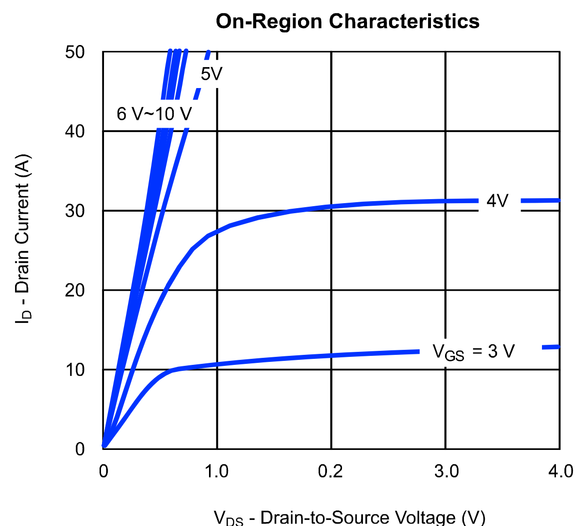












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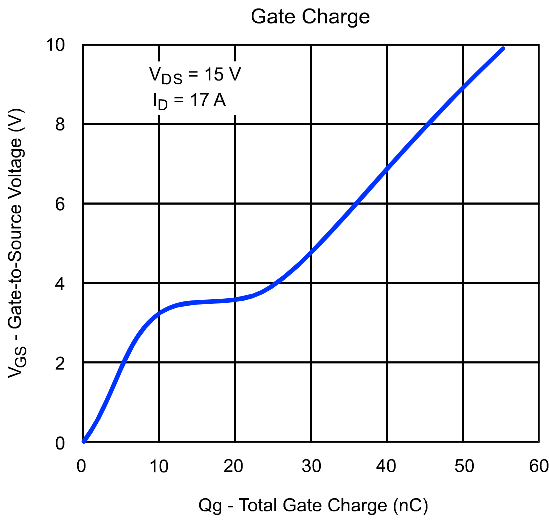
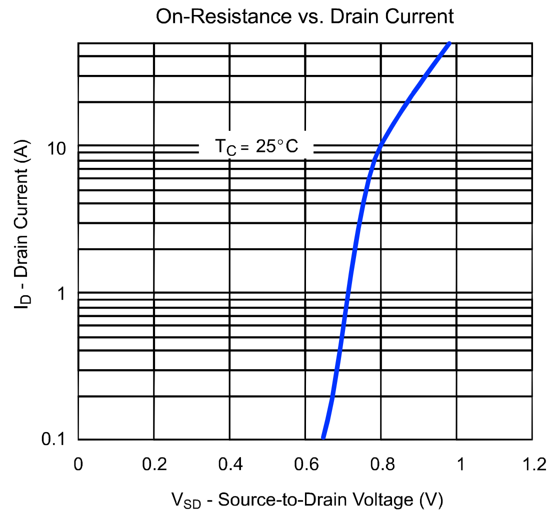
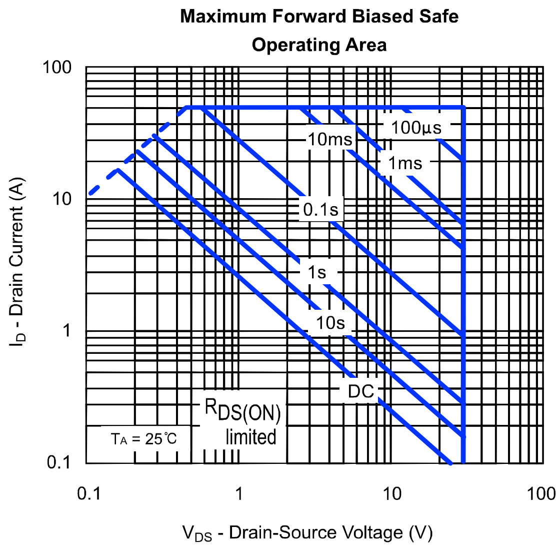
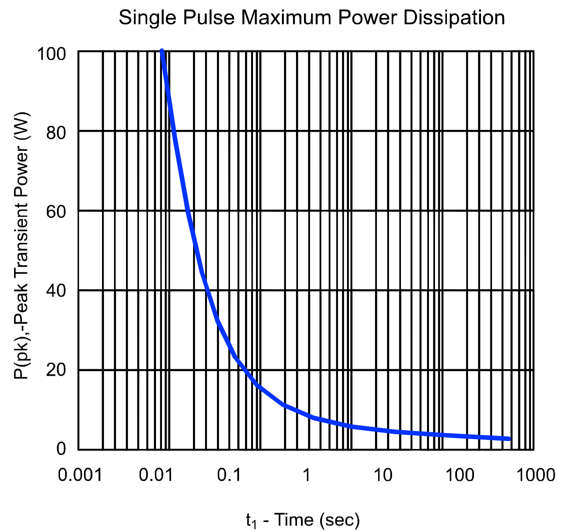
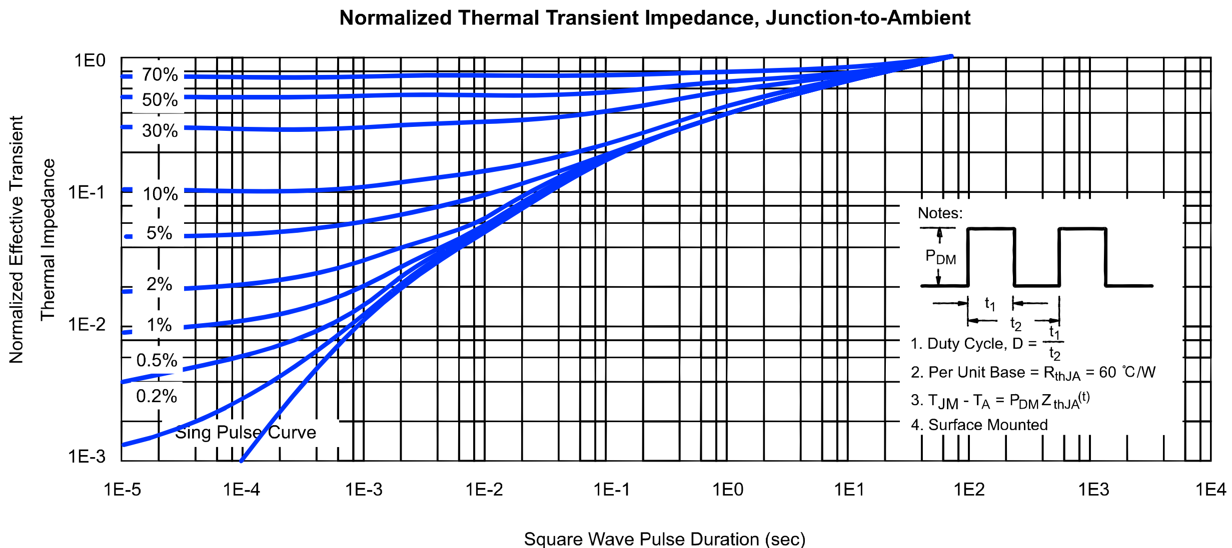


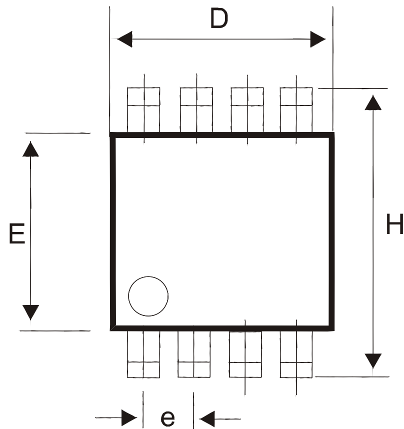


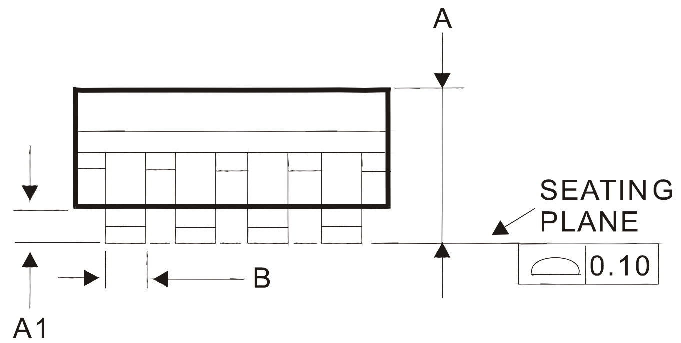


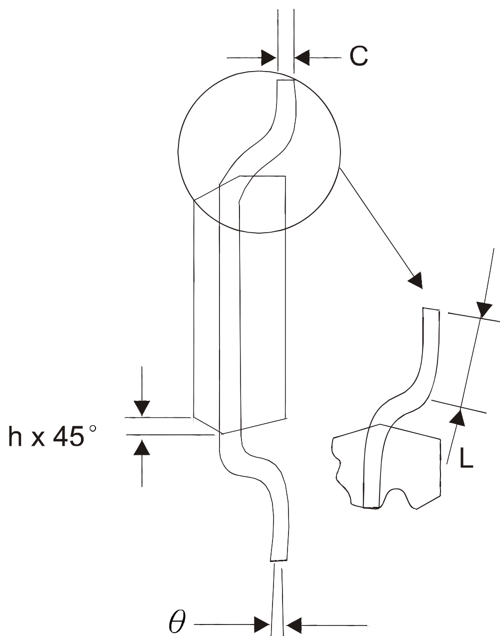




SOP-8 Package Outline







DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.