Dual N-Channel 30-V (D-S) MOSFET, ESD Protection

GENERAL DESCRIPTION

The ME4920D-G is the Dual N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology.This high density process is especially tailored to minimize on state resistance.These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 30\ m\Omega$ @VGS=10V
- $R_{DS(ON)} \leqq 40\ m\Omega$ @VGS=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

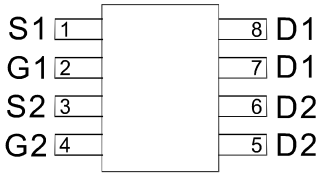
APPLICATIONS

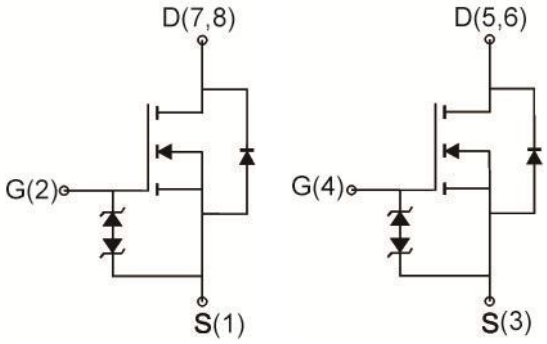
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(SOP-8)

Top View





Ordering Information: ME4920D (Pb-free)

ME4920D-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	6.7	A
	T_A=70℃		5.3	
Pulsed Drain Current		I_{DM}	27	A
Continuous Source Current (Diode Conduction)		I_S	1.7	A
Maximum Power Dissipation	T_A=25℃	P_D	2	W
	T_A=70℃		1.3	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	62.5	℃/W

The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±16V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			±1	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D= 6.9A		23	30	mΩ
		V_{GS}=4.5V, I_D= 5.8A		34	45	
V_{SD}	Diode Forward Voltage	I_S=6.9A, V_{GS}=0V		0.8	1.2	V
DYNAMIC[b]						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=6.9A		11		nC
Qgs	Gate-Source Charge			3		
Qgd	Gate-Drain Charge			2		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		360		pF
Coss	Output Capacitance			67		
Crss	Reverse Transfer Capacitance			20		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L=15Ω, I_D=1A, V_{GEN}=10V, R_G=6Ω		9.6		ns
tr	Turn-On Rise Time			12		
$t_{d(off)}$	Turn-Off Delay Time			31		
tf	Turn-Off Fall Time			3.7		

Notes: a. pulse test:pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice

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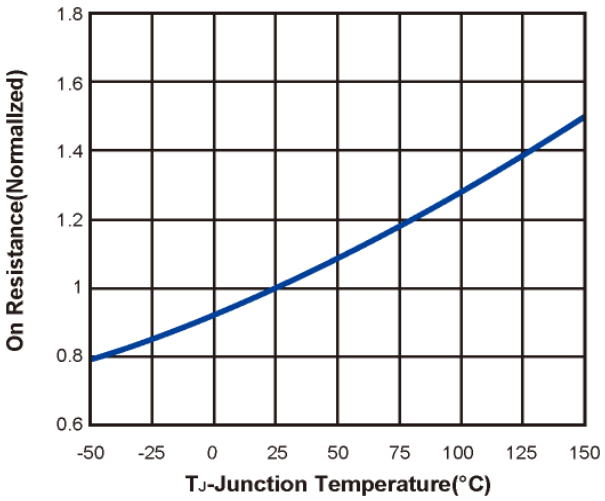
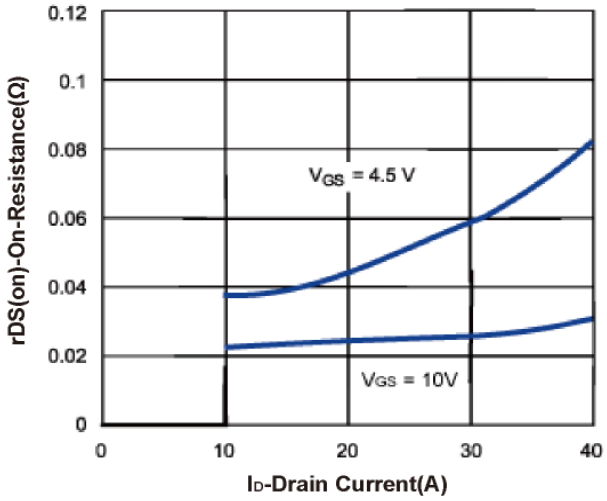
Typical Characteristics (T_J =25℃ Noted)

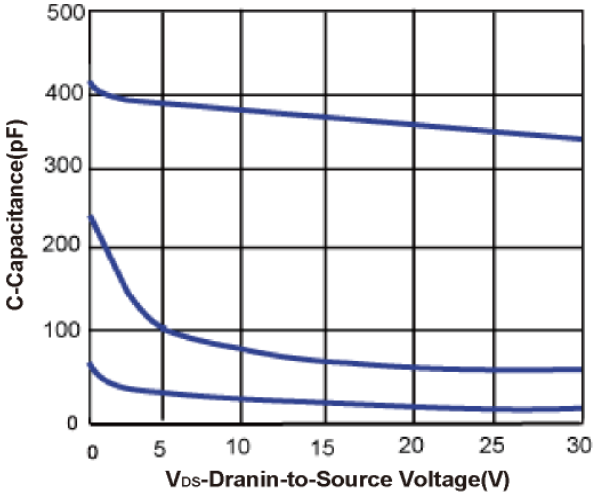
On Resistance vs. Junction Temperature



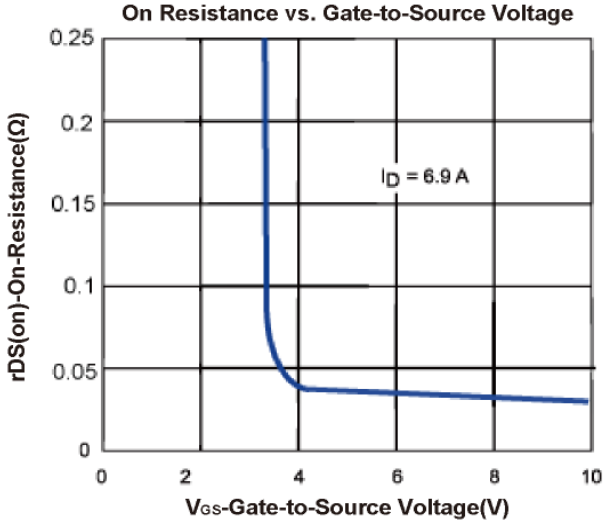
On Resistance vs. Drain Current



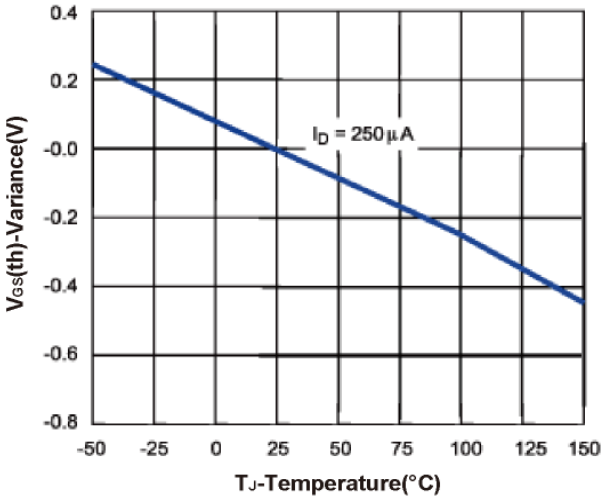
Capacitance



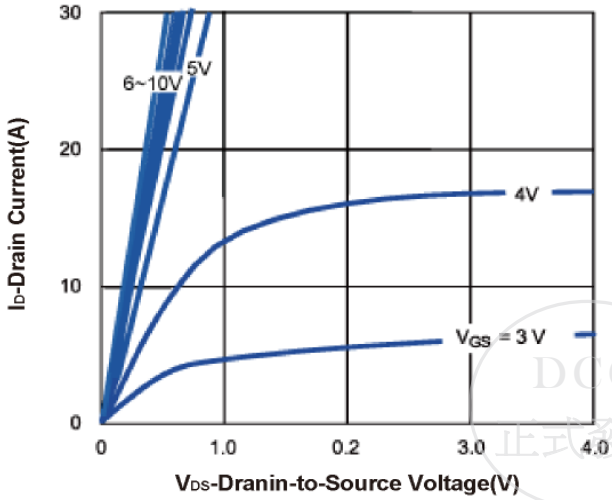
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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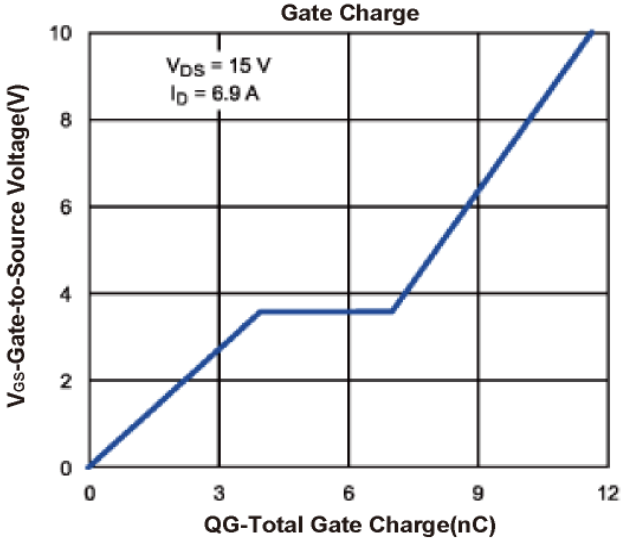
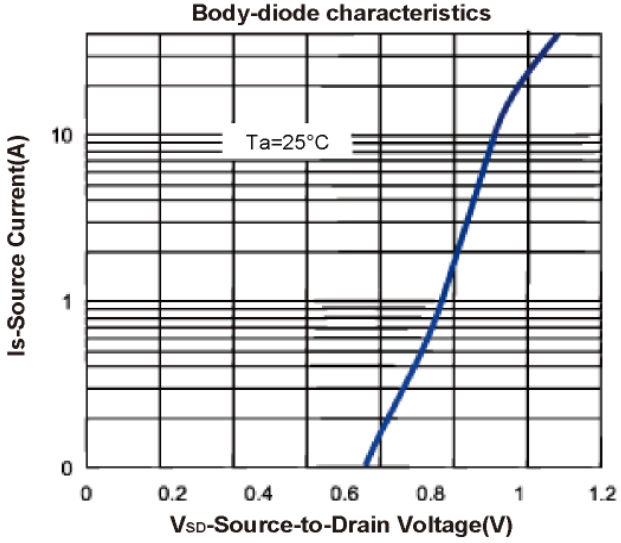
Typical Characteristics (T_J =25℃ Noted)

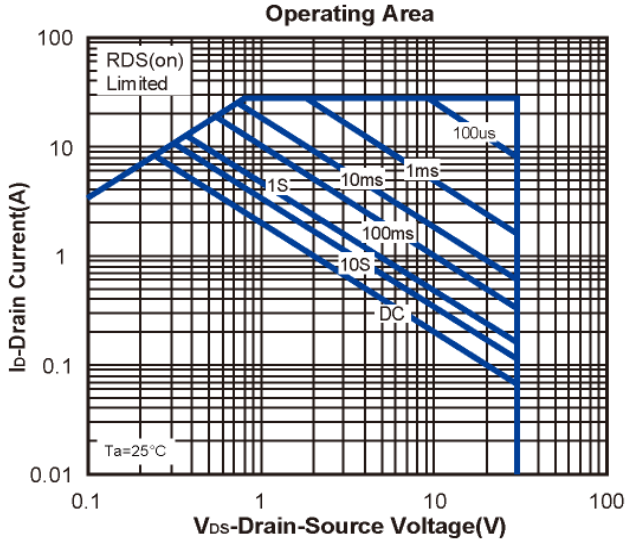
Gate Charge



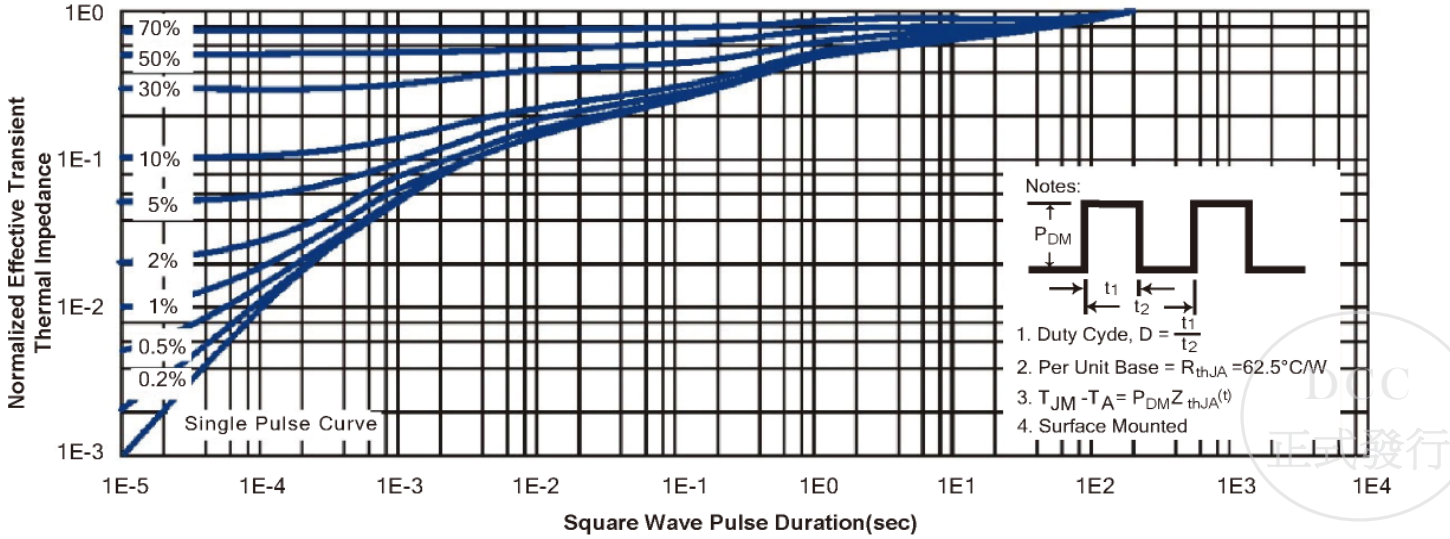
Body-diode characteristics



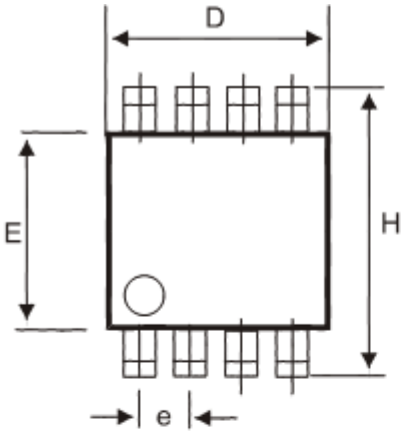
Maximum Forward Biased Safe Operating Area

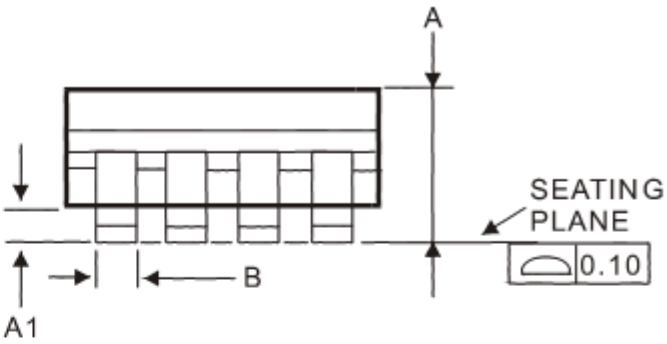


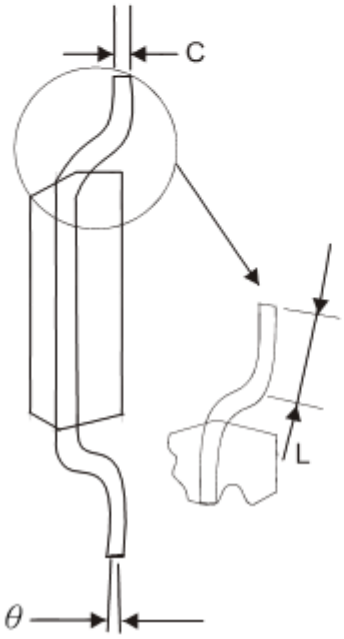
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







DIM	MILLIMETERS(mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.