ME4942/ME4942-G

Dual N-Channel 40-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4942 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 20m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 29m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

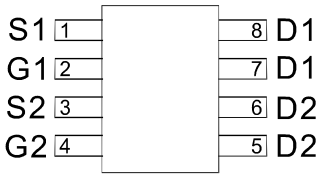
APPLICATIONS

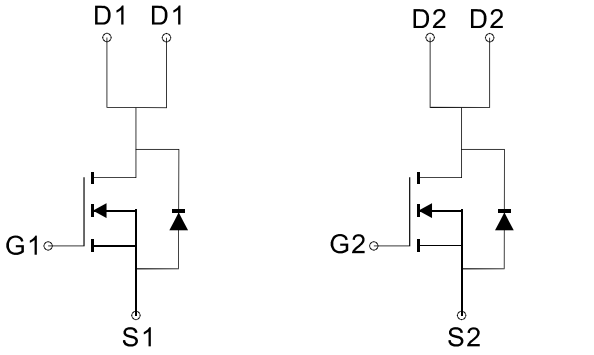
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(SOP-8)

Top View





Ordering Information: ME4942 (Pb-free)

ME4942-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	8	A
	T_A=70℃		6.3	
Pulsed Drain Current		I_{DM}	32	A
Maximum Power Dissipation	T_A=25℃	P_D	2	W
	T_A=70℃		1.3	
Junction & Storage Temperature Range		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient *		$R_{\theta JA}$	62.5	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

Dual N-Channel 40-V (D-S) MOSFET

Electrical Characteristics (T_J =25℃ Unless Otherwise Specified)

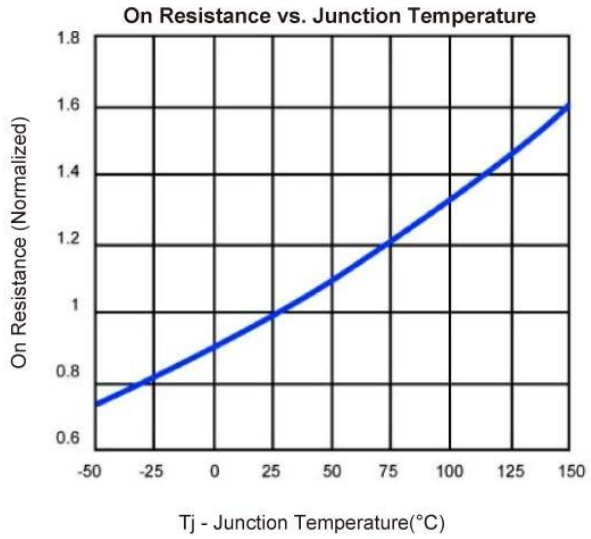
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=10V, I_D= 7.4A		16	20	mΩ
		V_{GS}=4.5V, I_D= 6.4A		22	29	
V_{SD}	Diode Forward Voltage	I_S=1.8A		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=20V, V_{GS}=10V, I_D=5.7A		21		nC
Qg	Total Gate Charge	V_{DS}=20V, V_{GS}=4.5V, I_D=5.7A		11		
Qgs	Gate-Source Charge			4.9		
Qgd	Gate-Drain Charge			4.7		
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1.0MHz		884		pF
Coss	Output Capacitance			124		
Crss	Reverse Transfer Capacitance			39		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=20V, R_L =20Ω V_{GEN}=10V, R_G=6Ω		15		ns
t_r	Turn-On Rise Time			11		
$t_{d(off)}$	Turn-Off Delay Time			45		
t_f	Turn-Off Fall Time			6		

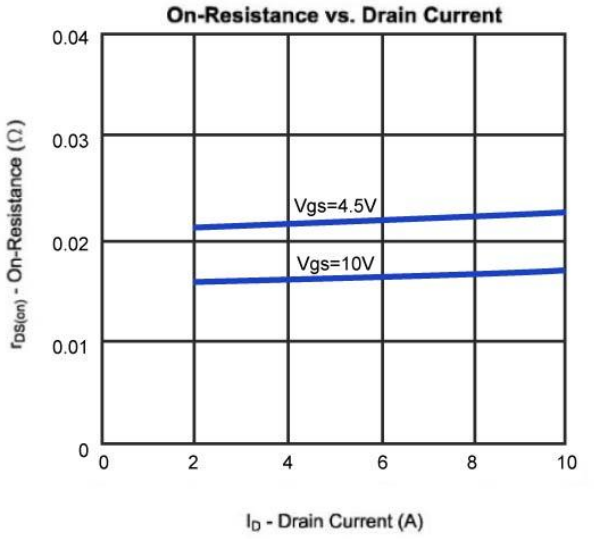
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

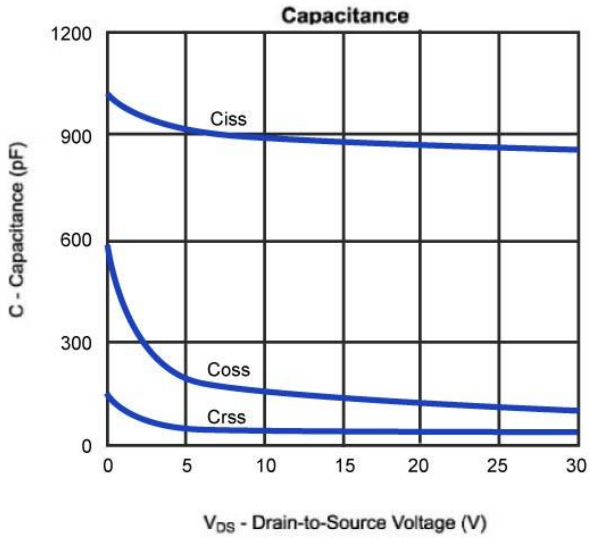
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

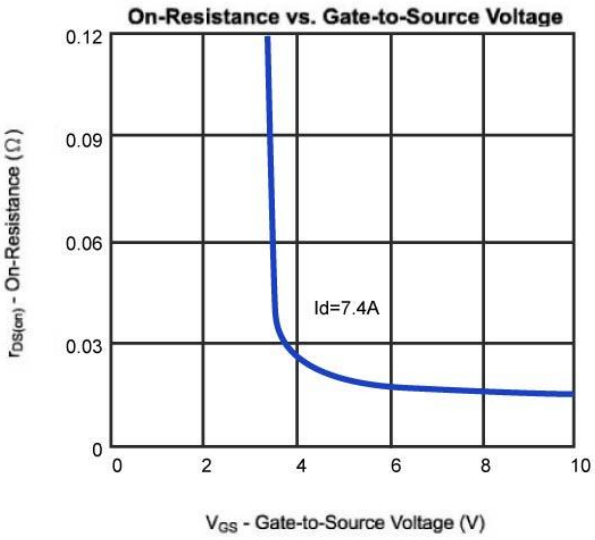
Dual N-Channel 40-V (D-S) MOSFET

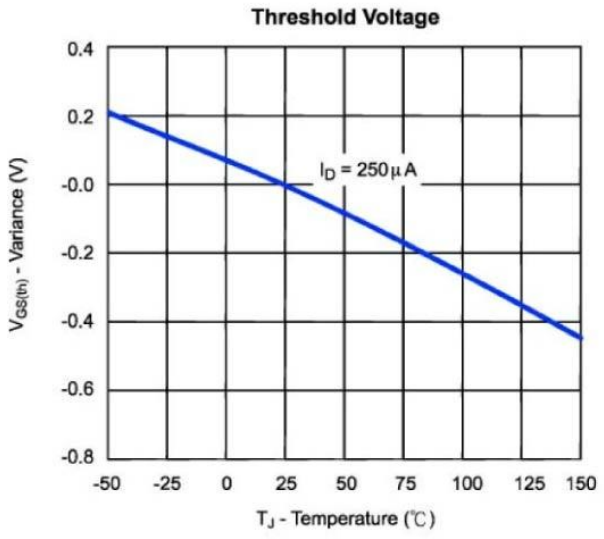
Typical Characteristics (T_J =25℃ Noted)

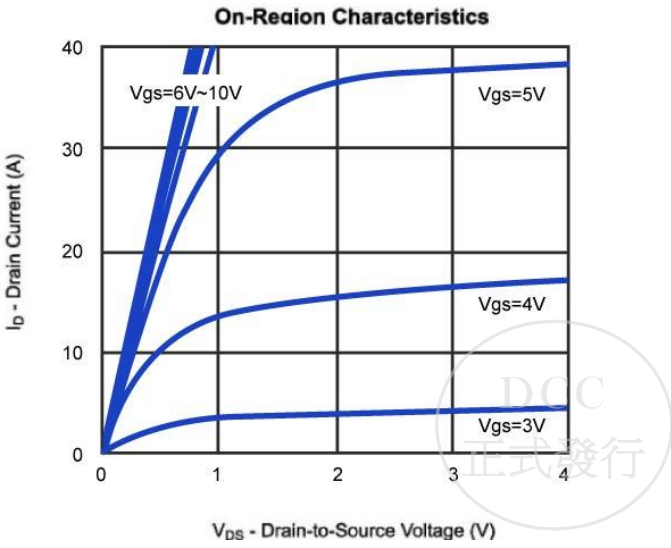








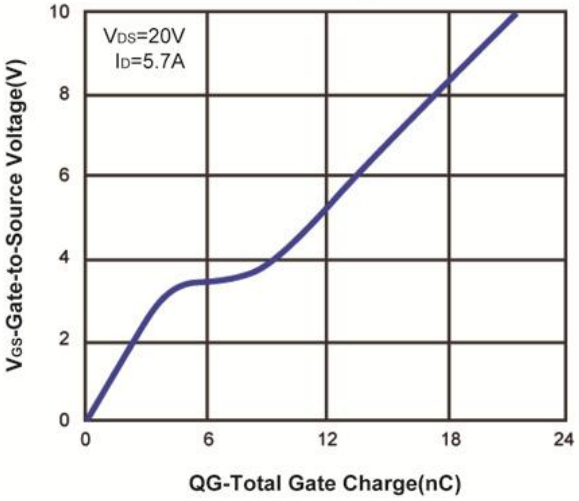




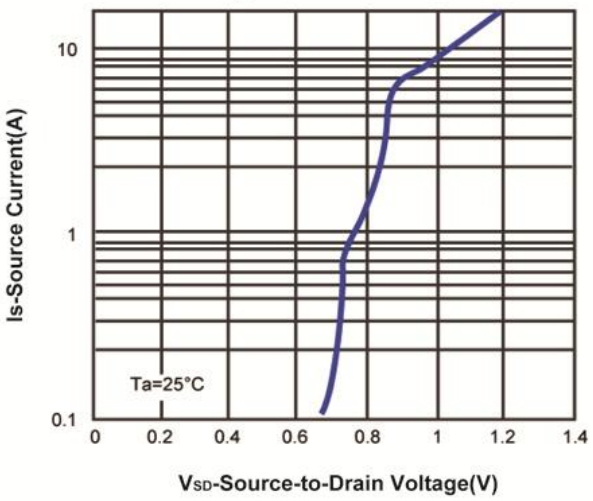
Dual N-Channel 40-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

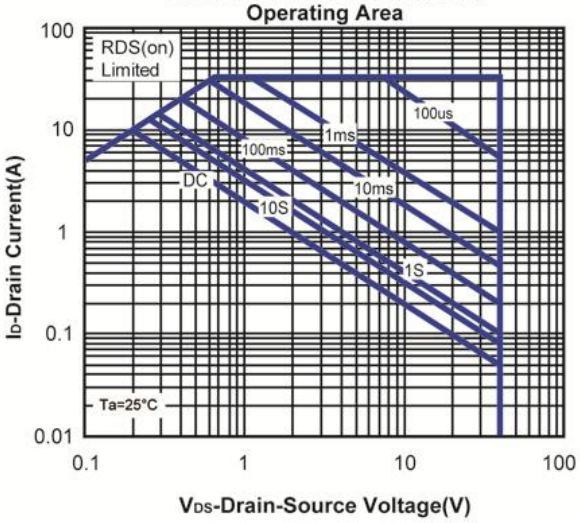
Gate Charge



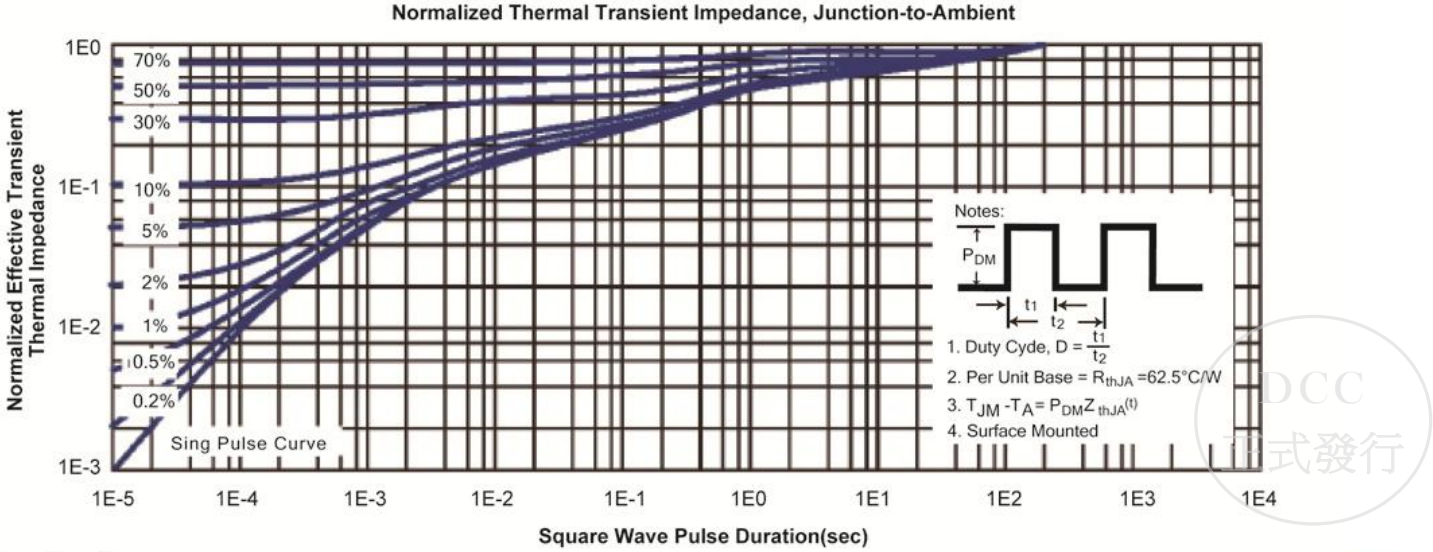
Body-diode characteristics



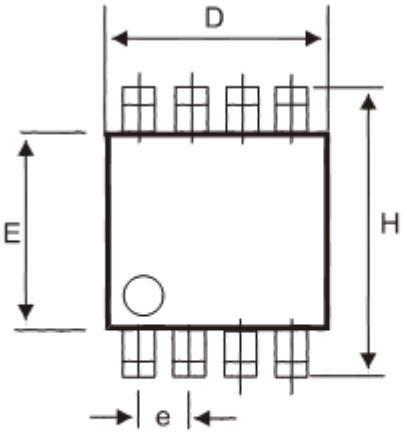
Maximum Forward Biased Safe Operating Area

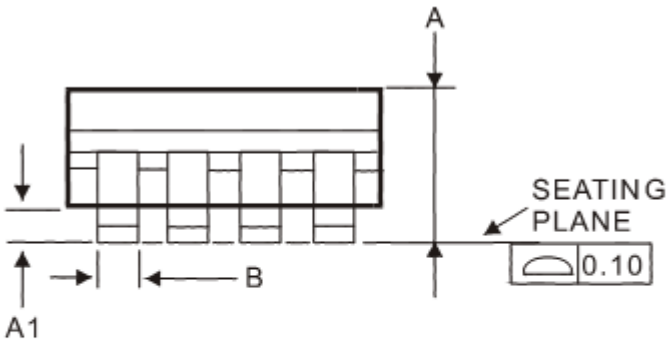


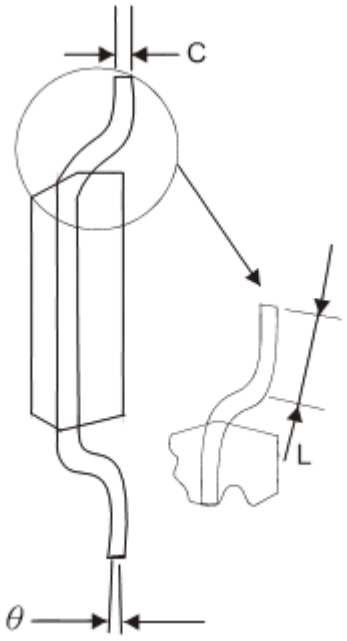
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°