

Dual N-Channel 60-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4948 is the Dual N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance. These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

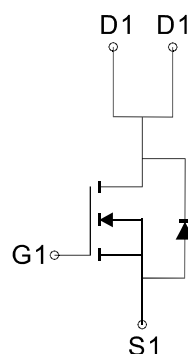
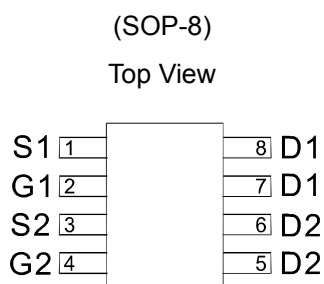
FEATURES

- $R_{DS(ON)} \leq 53 \text{ m}\Omega @ V_{GS}=10\text{V}$
- $R_{DS(ON)} \leq 78 \text{ m}\Omega @ V_{GS}=4.5\text{V}$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

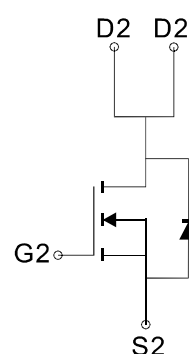
APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION



N-Channel MOSFET



N-Channel MOSFET

Ordering Information: ME4948 (Pb-free)

ME4948-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ($T_j=150^\circ\text{C}$)	$T_A=25^\circ\text{C}$	I_D	4.9	A
	$T_A=70^\circ\text{C}$		3.9	
Pulsed Drain Current		I_{DM}	19	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2	W
	$T_A=70^\circ\text{C}$		1.3	
Operating Junction Temperature		T_J	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient *		$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

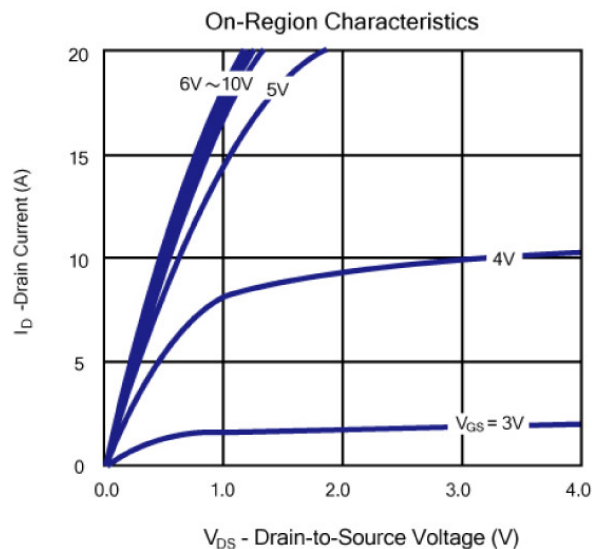
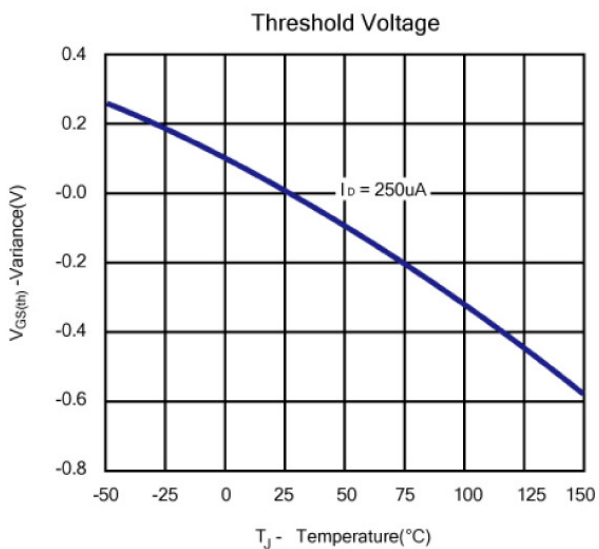
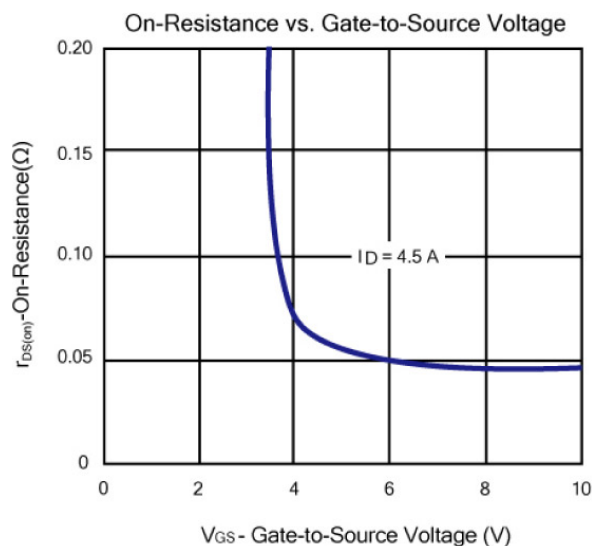
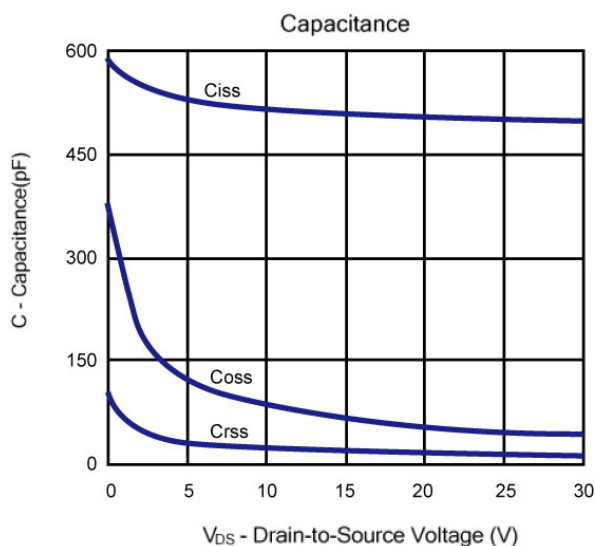
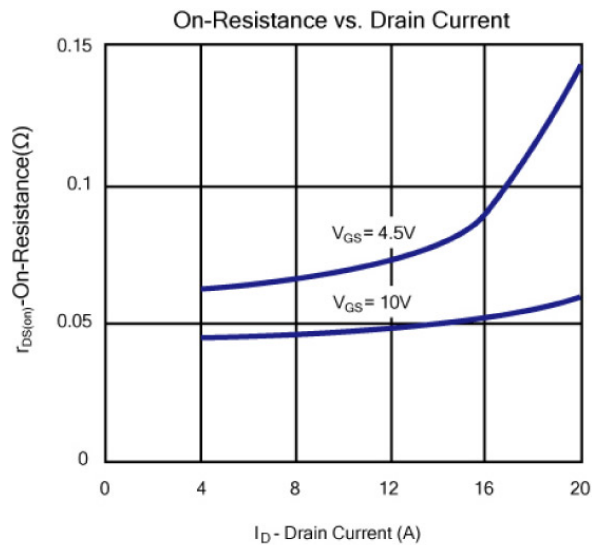
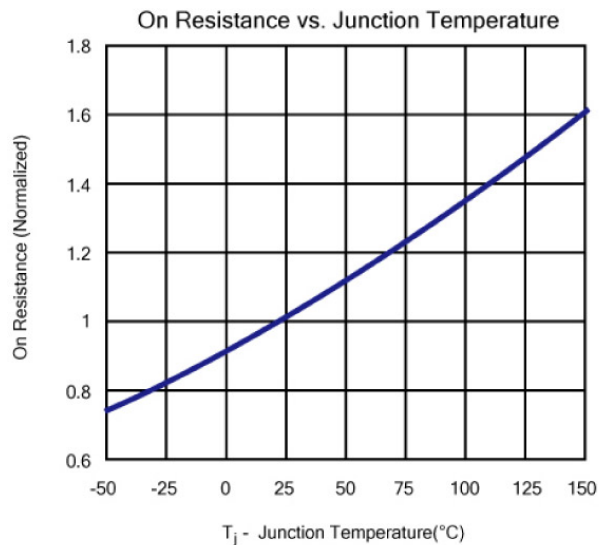
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V, ID=250 μ A	60			V
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250 μ A	1		3	V
IGSS	Gate Leakage Current	VDS=0V, VGS=±20V			±100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=60V, VGS=0V			1	μ A
RDS(ON)	Drain-Source On-Resistance ^a	VGS=10V, ID= 4.5A		45	53	m Ω
		VGS=4.5V, ID= 3.6A		60	78	
VSD	Diode Forward Voltage	IS=2.0A, VGS=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	VDS=30V, VGS=10V, ID=4.5A		16		nC
Qg	Total Gate Charge	VDS=30V, VGS=4.5V, ID=4.5A		8.4		
Qgs	Gate-Source Charge			3.5		
Qgd	Gate-Drain Charge			4.2		
Ciss	Input Capacitance	VDS=15V, VGS=0V, f=1MHz		507		pF
Coss	Output Capacitance			65		
Crss	Reverse Transfer Capacitance			20		
td(on)	Turn-On Delay Time	VDD=30V, RL =15 Ω , VGEN=10V, RG=1 Ω		11		ns
tr	Turn-On Rise Time			12		
td(off)	Turn-Off Delay Time			33		
tf	Turn-Off Fall Time			3		

Notes: a. Pulse test: pulse width $\leq$ 300 μ s, duty cycle $\leq$ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

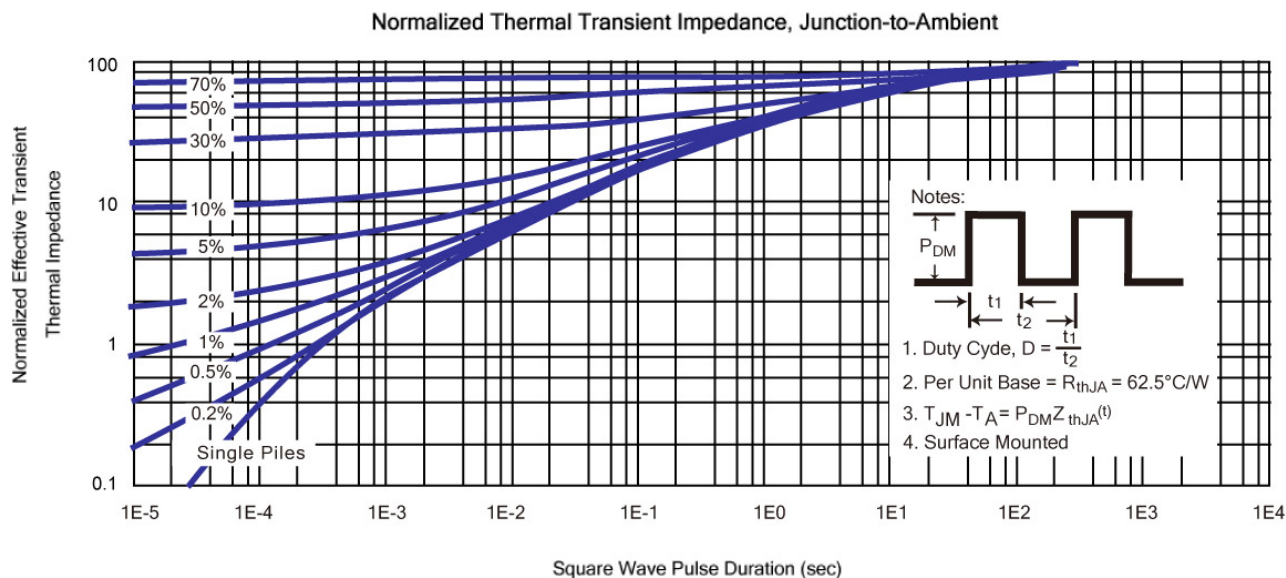
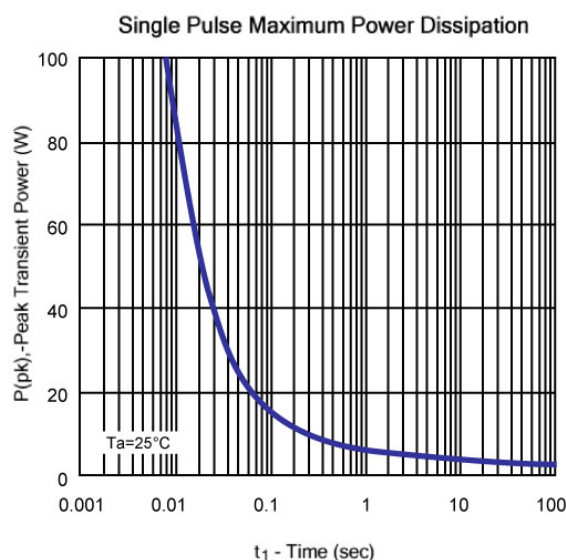
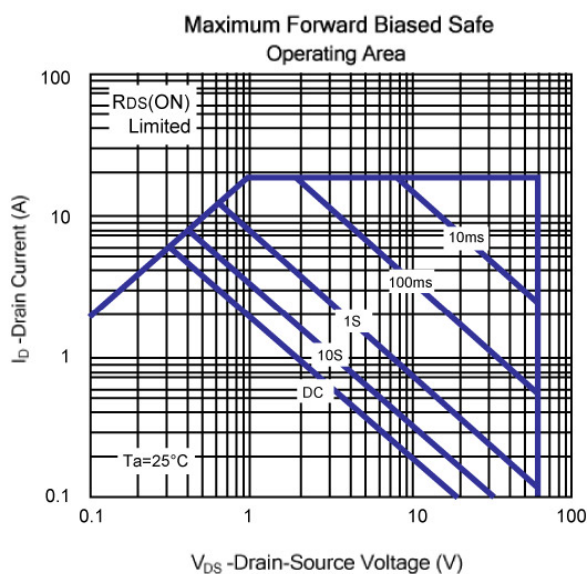
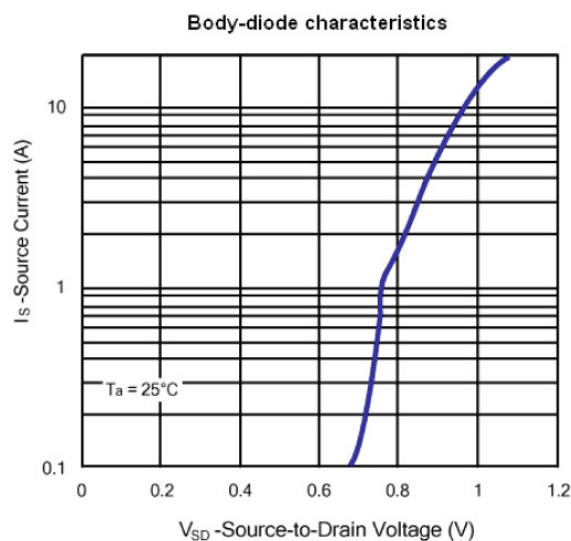
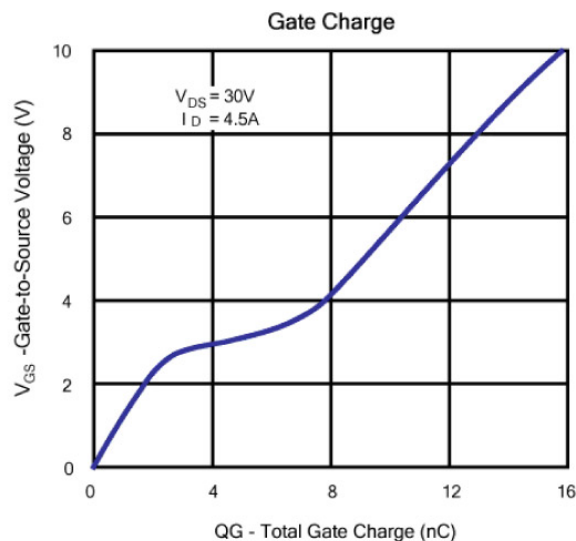
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Typical Characteristics (T_J = 25°C Noted)

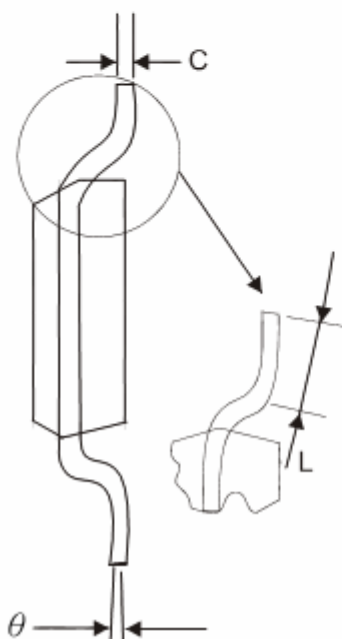
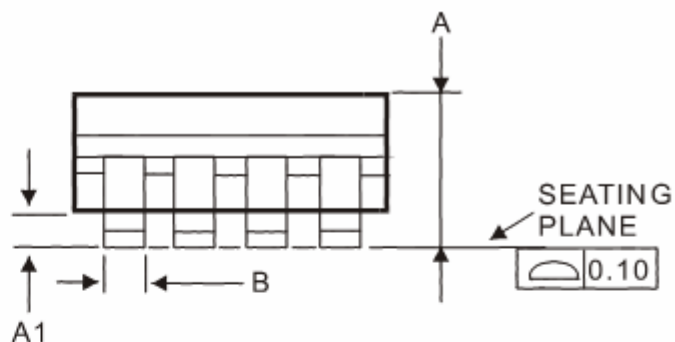
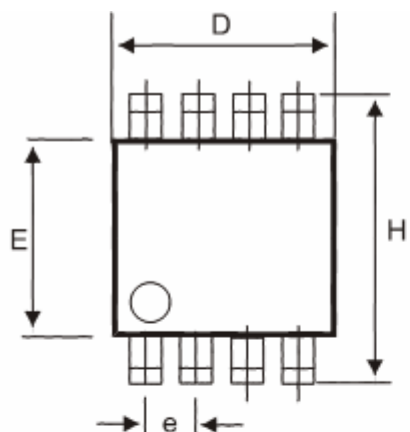


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SOP-8 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°