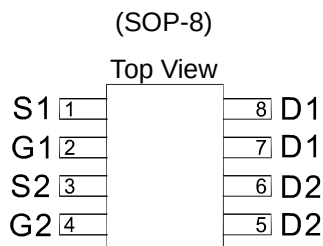


Dual N-Channel 30-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4970A-G is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

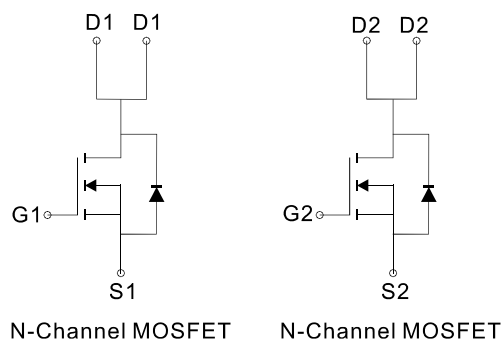


FEATURES

- $R_{DS(ON)} \leq 14m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 20m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter



Ordering Information: ME4970A /ME4970A-G (Green product-Halogen -free)

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A=25^\circ\text{C}$	I_D	10	A
	$T_A=70^\circ\text{C}$		8	
Pulsed Drain Current		I_{DM}	40	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2	W
	$T_A=70^\circ\text{C}$		1.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

*The device mounted on 1in^2 FR4 board with 2 oz copper



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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D = 10A		10	14	mΩ
		V _{GS} =4.5V, I _D = 8A		15	20	
V _{SD}	Diode Forward Voltage	I _S =8.2A, V _{GS} =0V		0.8	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =10V, V _{GS} =4.5V, I _D =8.2A		12.3		nC
Q _{gs}	Post-V _{th} Gate-Source Charge			5.7		
Q _{gd}	Gate-Drain Charge			5.5		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		1138		pF
C _{oss}	Output Capacitance			272		
C _{rss}	Reverse Transfer Capacitance			121		
t _{d(on)}	Turn-On Delay Time	V _{DD} =15V, R _L =15Ω I _D =1A, V _{GEN} =10V, R _G =6Ω		16.3		ns
t _r	Turn-On Rise Time			16.4		
t _{d(off)}	Turn-Off Delay Time			45.7		
t _f	Turn-Off Fall Time			7.7		

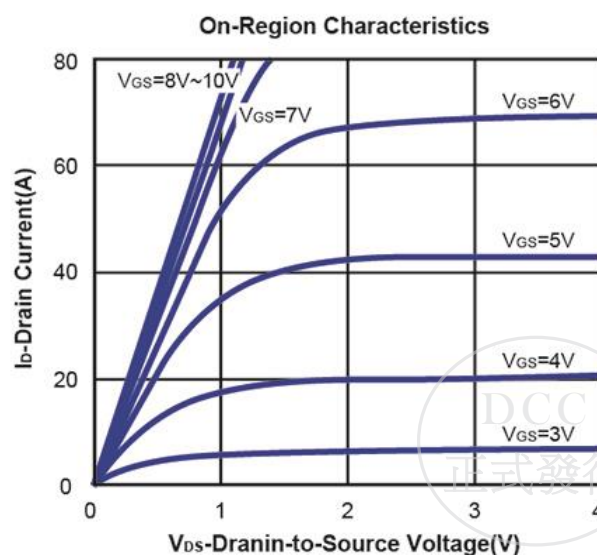
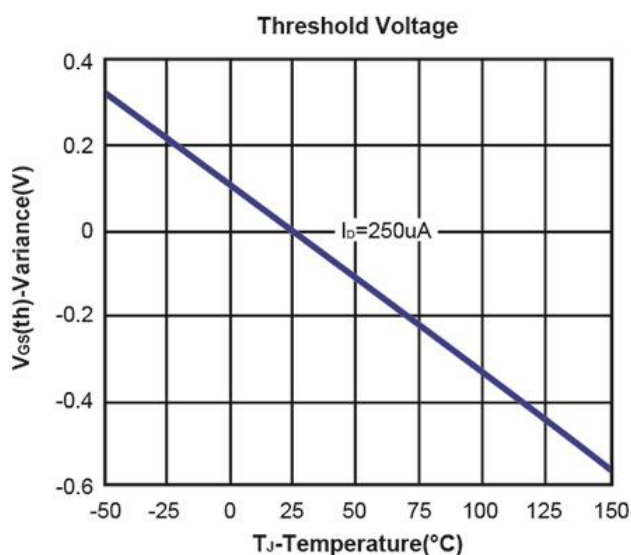
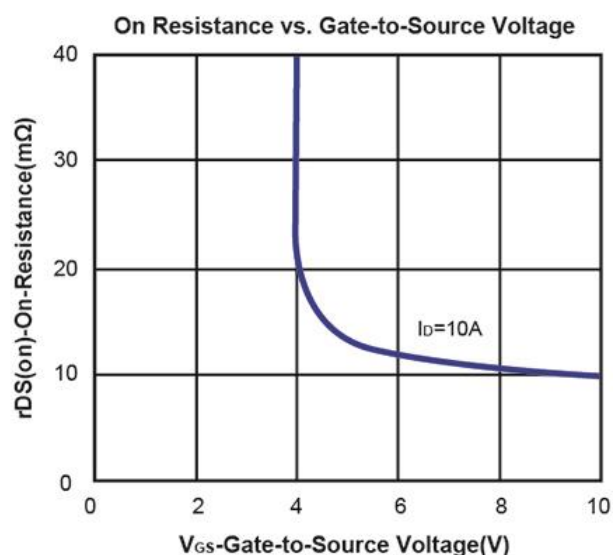
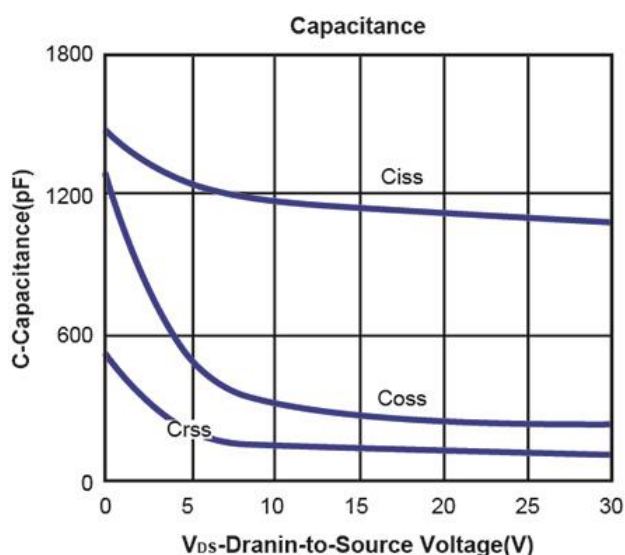
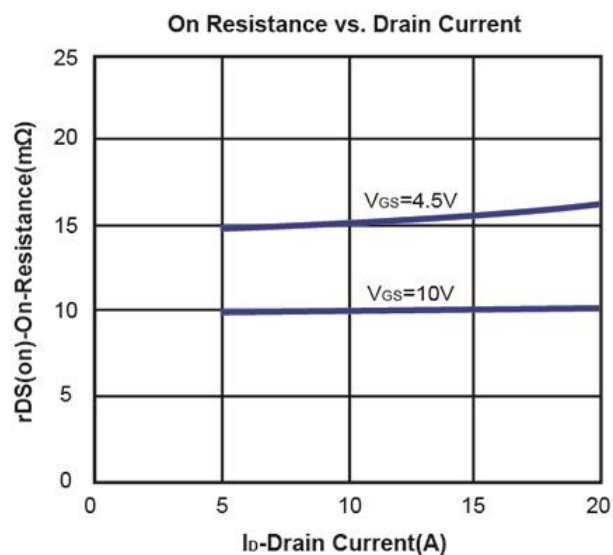
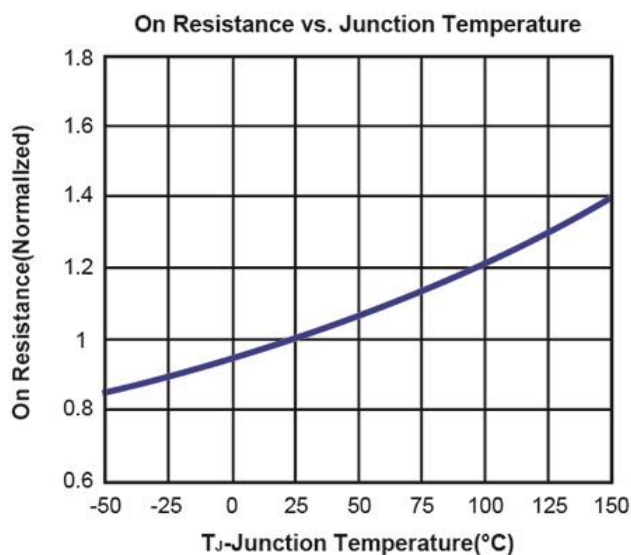
Notes: a. pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice



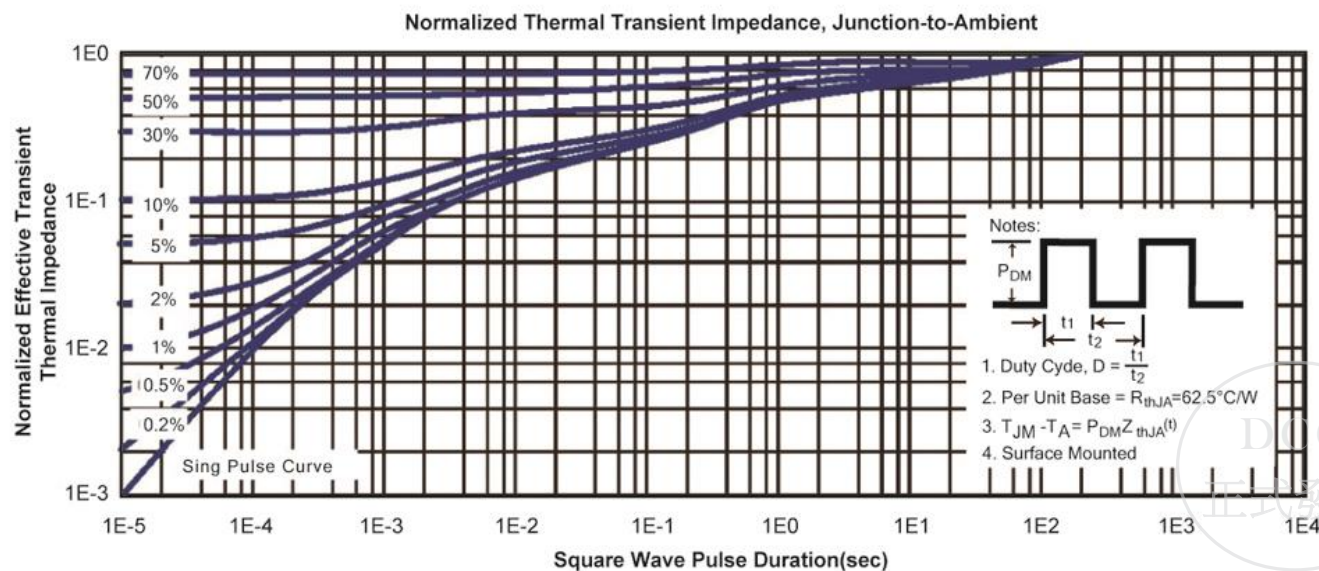
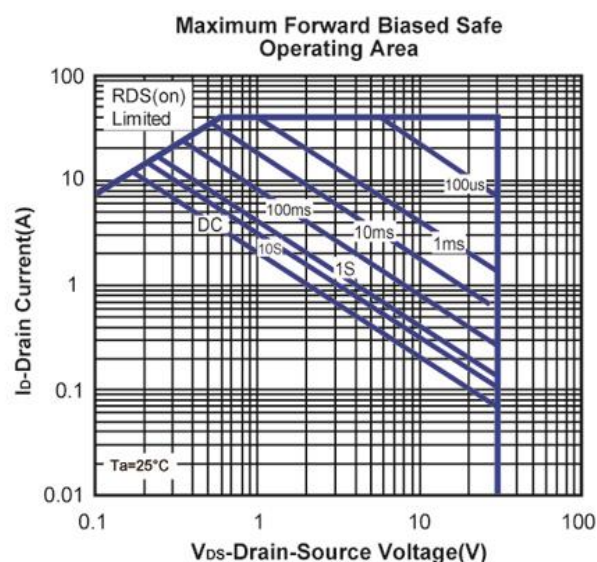
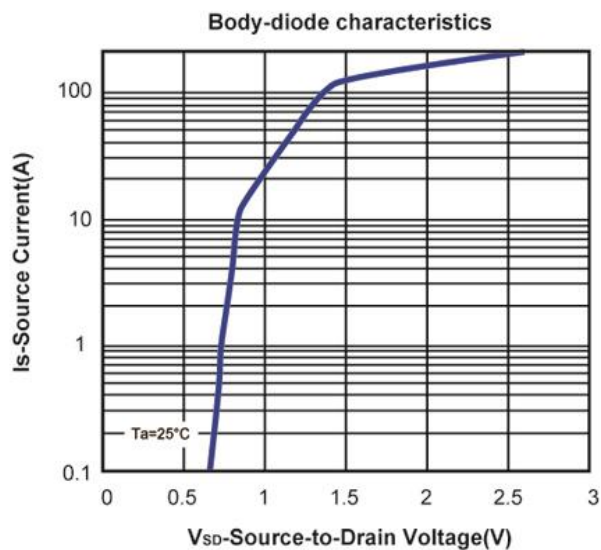
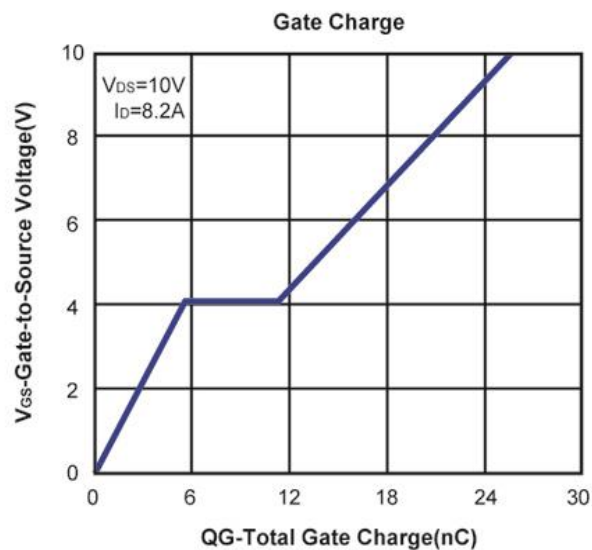
Dual N-Channel 30-V (D-S) MOSFET

Typical Characteristics (T_J =25°C Noted)

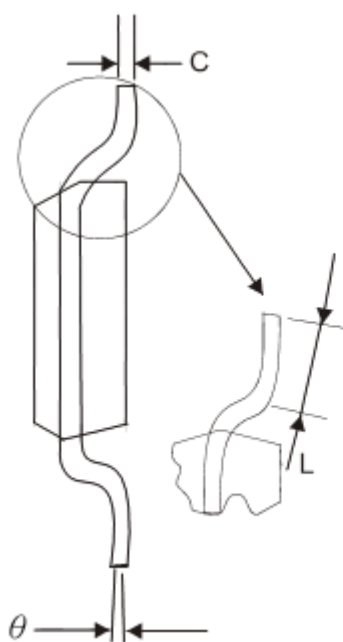
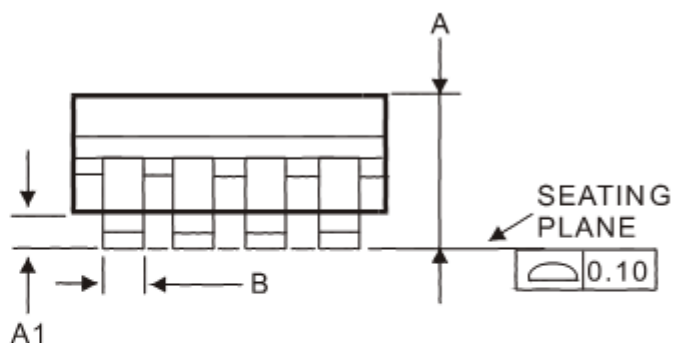
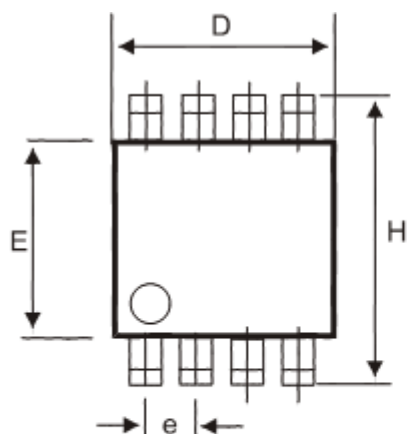


Dual N-Channel 30-V (D-S) MOSFET

Typical Characteristics (T_J =25°C Noted)



SOP-8 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

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