

N-Channel 60-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME50N06T is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

- $R_{DS(ON)} \leq 22m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

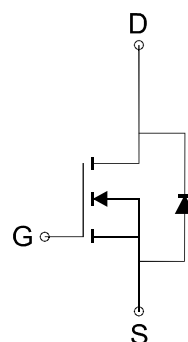
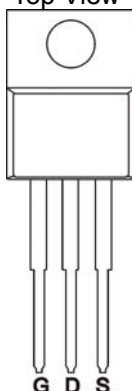
APPLICATIONS

- Power Management
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

(TO-220)

Top View



N-Channel MOSFET

Ordering Information: ME50N06T (Pb-free)

ME50N06T-G (Green product-Halogen free)

Absolute Maximum Ratings (T_c=25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DSS}	60	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current	T _c =25°C	I _D	53	A
	T _c =70°C		44	
Pulsed Drain Current		I _{DM}	212	A
Maximum Power Dissipation	T _c =25°C	P _D	136	W
	T _c =70°C		95	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 175	°C
Thermal Resistance-Junction to Case*		R _{θJC}	1.1	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper.

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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0		4.0	V
I_{GSS}	Gate-Body Leakage	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	$V_{GS}=10V, I_D=50A$		17	22	$m\Omega$
V_{SD}	Diode Forward Voltage *	$I_S=50A, V_{GS}=0V$		1.0	1.2	V
DYNAMIC						
Q_g	Total Gate Charge	$V_{DS}=48V, V_{GS}=10V, I_D=50A$		38		nC
Q_g	Total Gate Charge	$V_{DS}=48V, V_{GS}=4.5V, I_D=50A$		11		
Q_{gs}	Gate-Source Charge			15		
Q_{gd}	Gate-Drain Charge			8		
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$		2		Ω
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$		2270		pF
C_{oss}	Output Capacitance			197		
C_{rss}	Reverse Transfer Capacitance			62		
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V, R_L=30\Omega,$ $V_{GS}=10V, R_G=3.6\Omega$		29		ns
t_r	Turn-On Rise Time			5		
$t_{d(off)}$	Turn-Off Delay Time			53		
T_f	Turn-Off Fall Time			6		

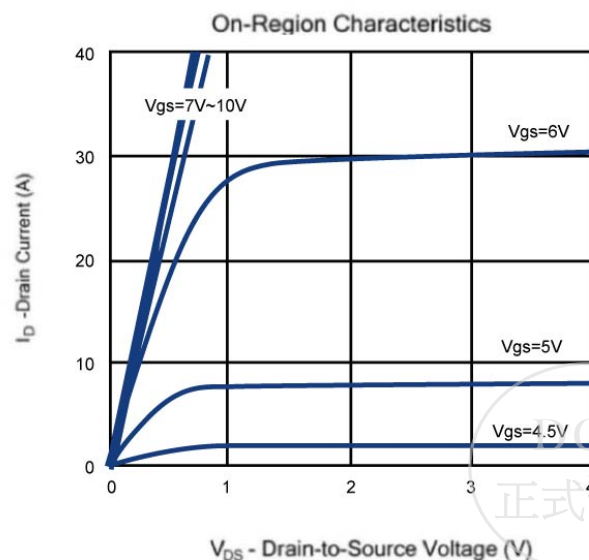
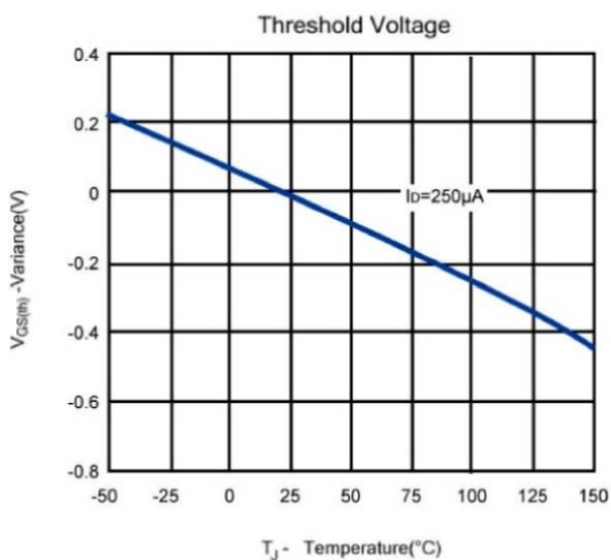
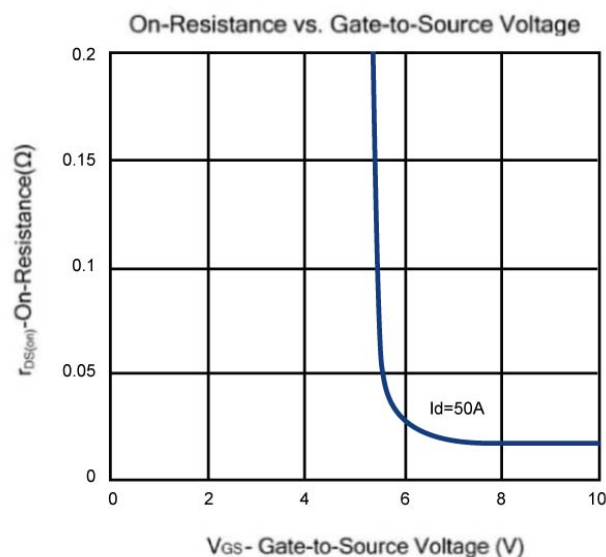
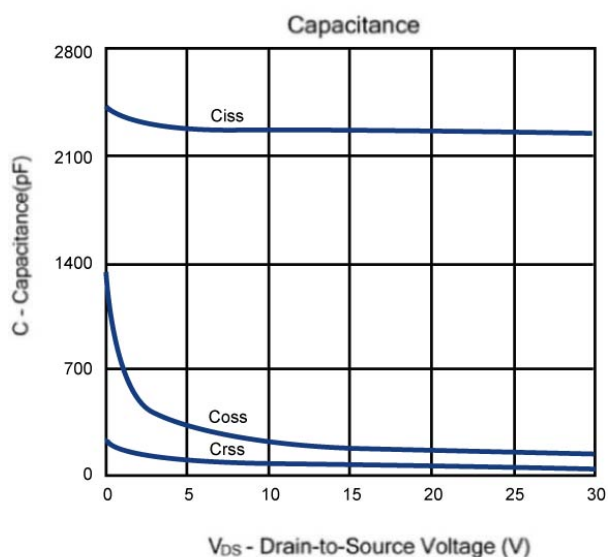
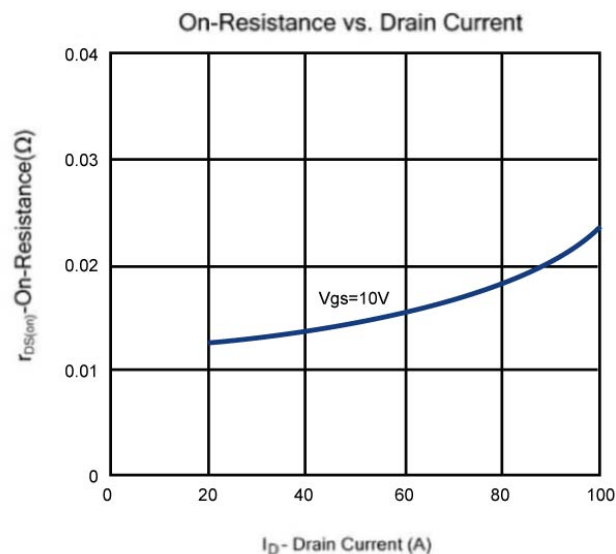
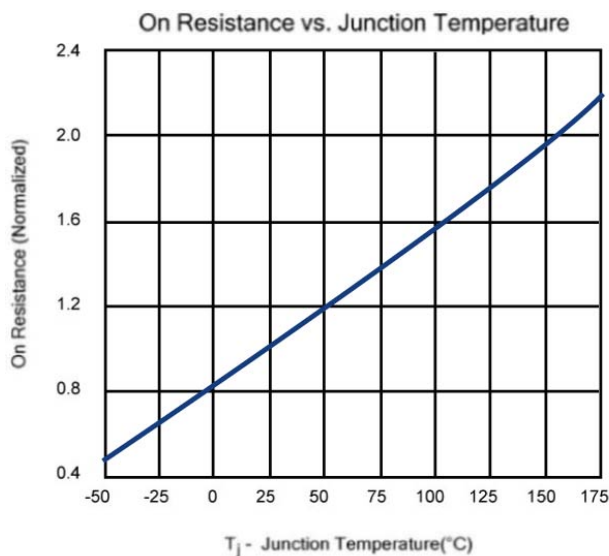
Notes: a. pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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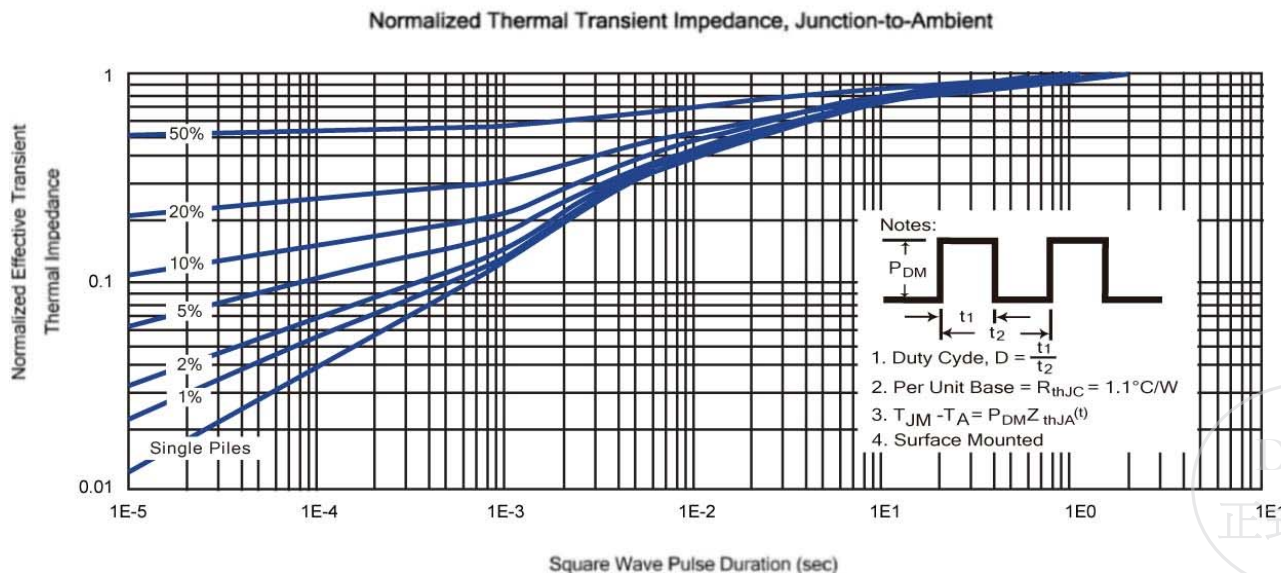
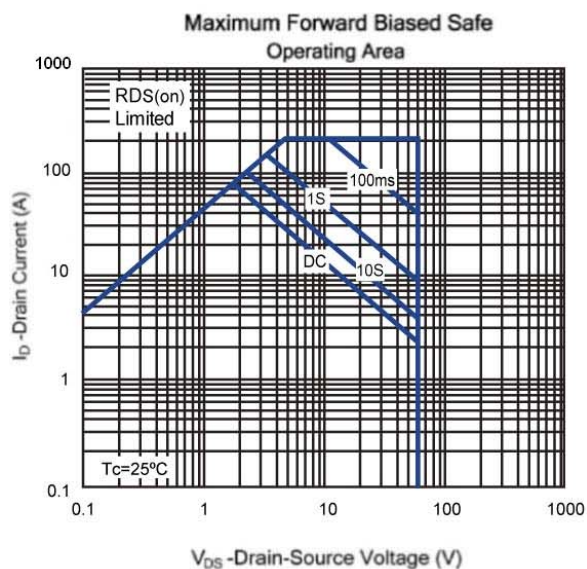
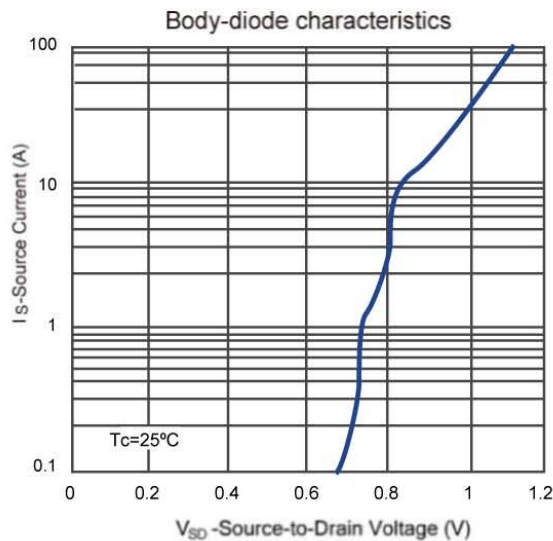
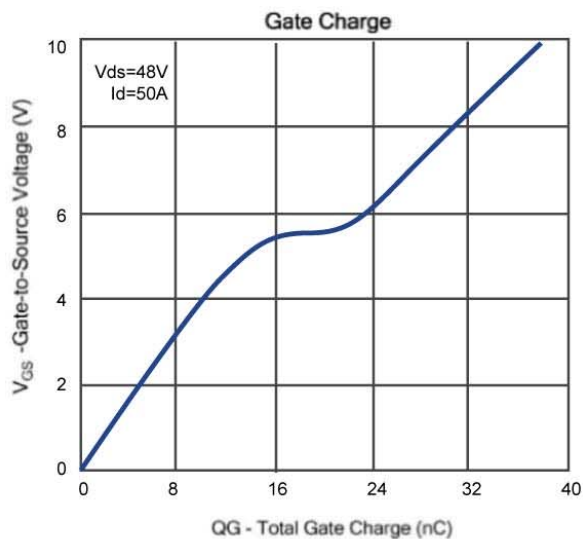
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Typical Characteristics (T_J =25°C Noted)

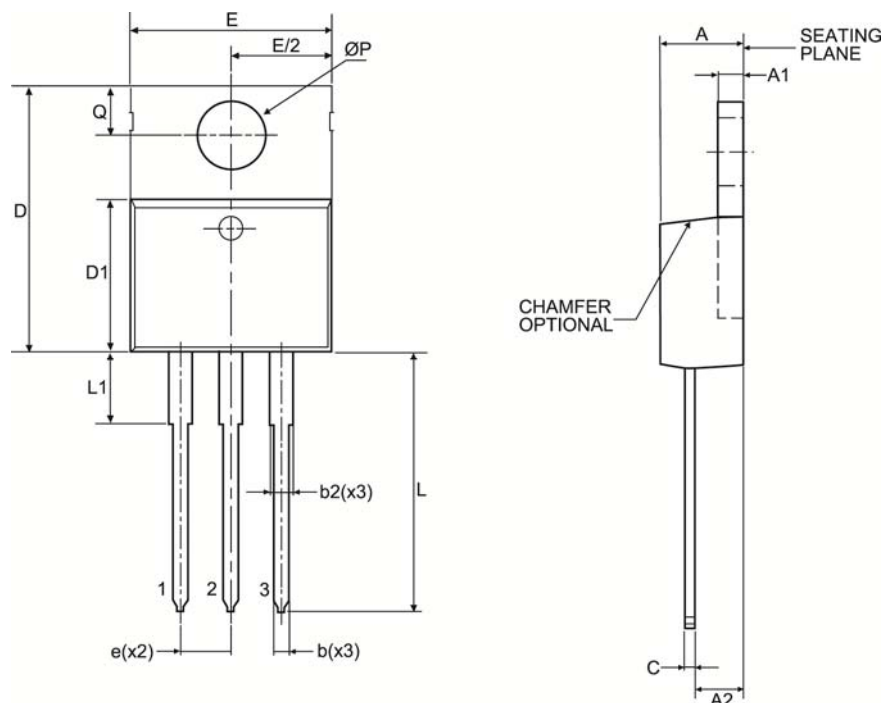


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TO-220 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	3.50	4.90
A1	1.00	1.40
A2	2.00	3.00
b	0.70	1.40
c	0.35	0.65
D	14.00	16.50
D1	8.30	9.50
E	9.60	10.70
e	2.54 BSC	
L	12.50	15.00
ØP	3.60 TYP	
Q	2.50	3.10
b2	1.10	1.80
L1	2.40	3.20

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