

N- Channel 100V (D-S) MOSFET

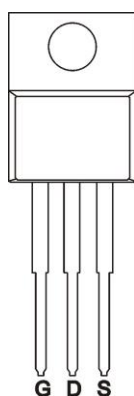
GENERAL DESCRIPTION

The ME50N10AT-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

(TO-220)

Top View

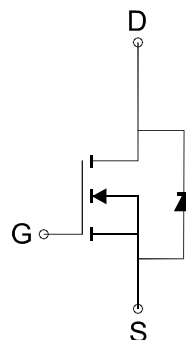


FEATURES

- $R_{DS(ON)} \leq 40m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 60m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter



N-Channel MOSFET

Ordering Information: ME50N10AT /ME50N10AT-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current*	Tc=25°C	I_D	64.5	A
	Tc=70°C		54	
Pulsed Drain Current		I_{DM}	258	A
Maximum Power Dissipation*	Tc=25°C	P_D	300	W
	Tc=70°C		210	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 175	°C
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	0.5	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (T_c =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	100			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D = 20A		34	40	mΩ
		V _{GS} =4.5V, I _D = 20A		43	60	
V _{SD}	Diode Forward Voltage	I _S =35A, V _{GS} =0V		1		V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =5.5V, I _D =20A		26		nC
Q _{gs}	Gate-Source Charge			10.5		
Q _{gd}	Gate-Drain Charge			8.6		
C _{iss}	Input capacitance	V _{DS} =30V, V _{GS} =0V, F=1MHz		2435		pF
C _{oss}	Output Capacitance			95		
C _{rss}	Reverse Transfer Capacitance			62		
t _{d(on)}	Turn-On Delay Time	V _{DS} =50V, R _L =2.5Ω V _{GEN} =10V, R _G =6Ω		19.4		ns
t _r	Turn-On Rise Time			21.9		
t _{d(off)}	Turn-Off Delay Time			60.5		
t _f	Turn-Off Fall Time			10.2		

Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

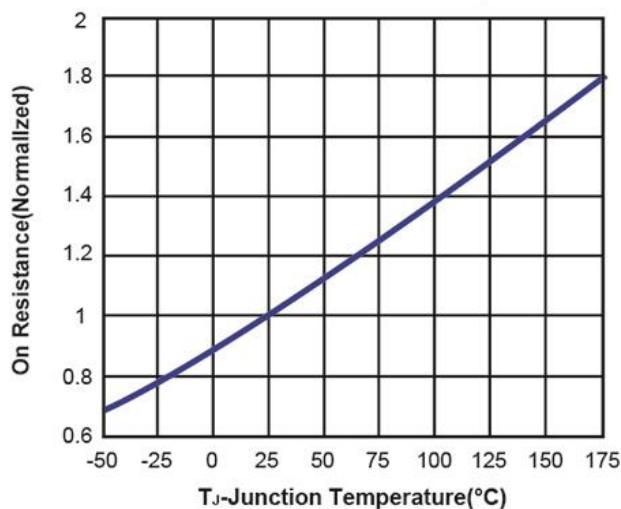
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



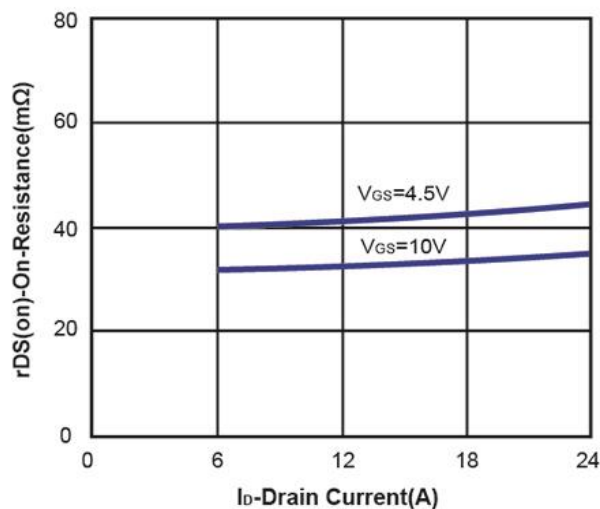
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Typical Characteristics (T_J =25°C Noted)

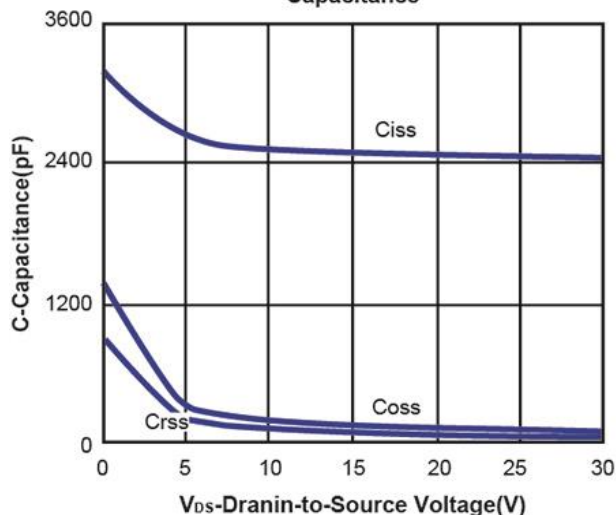
On Resistance vs. Junction Temperature



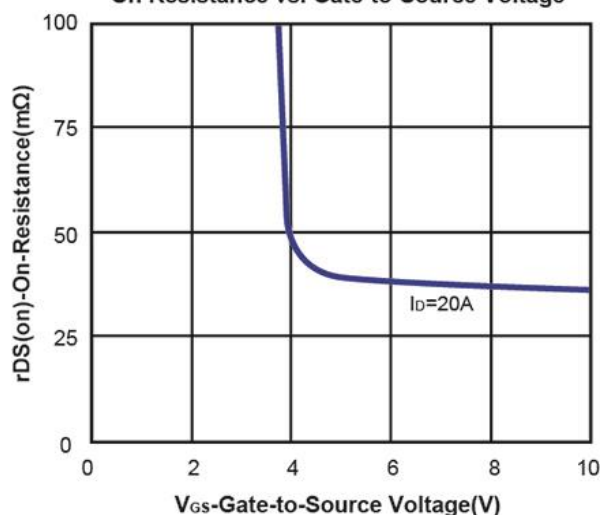
On Resistance vs. Drain Current



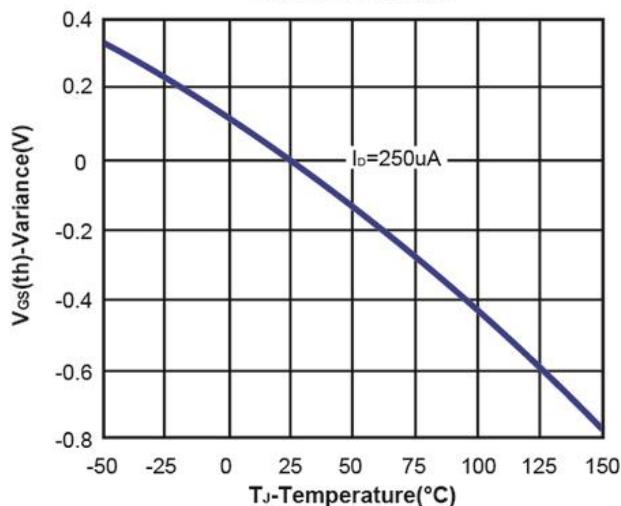
Capacitance



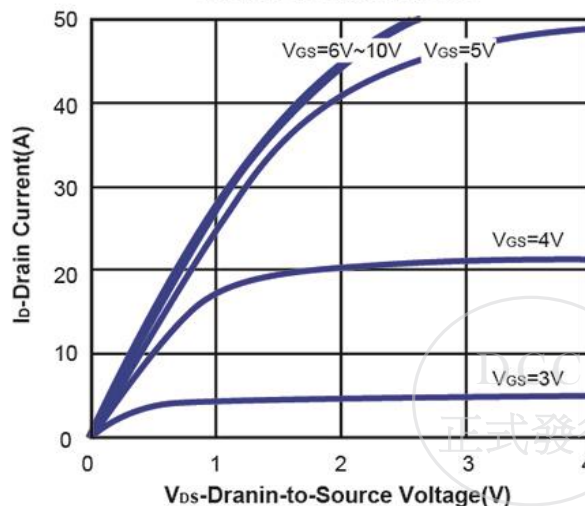
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage

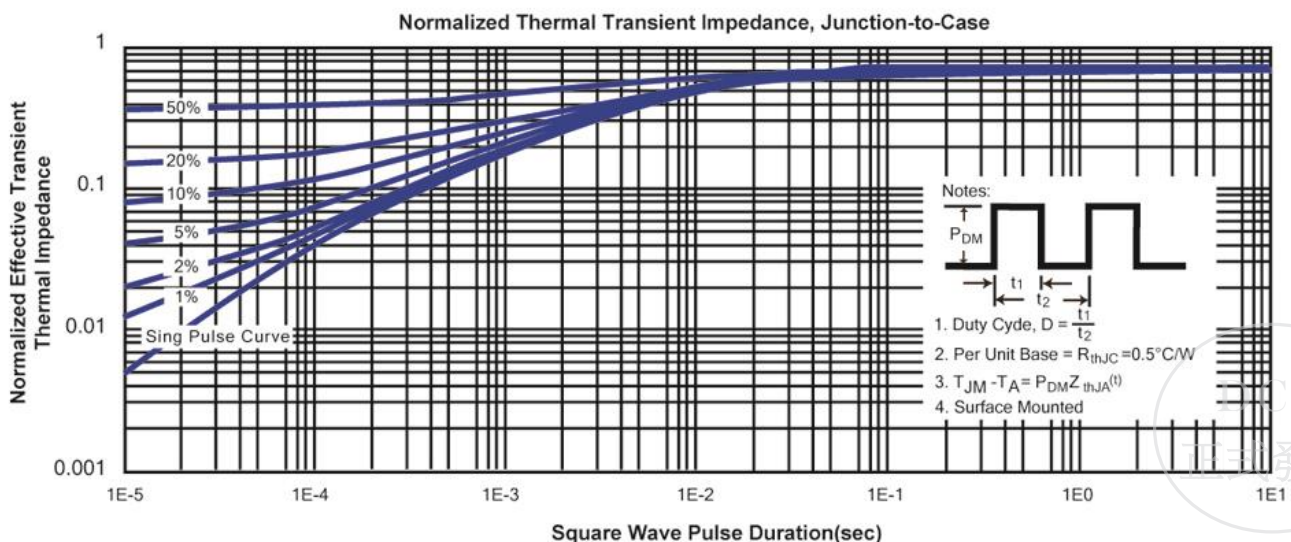
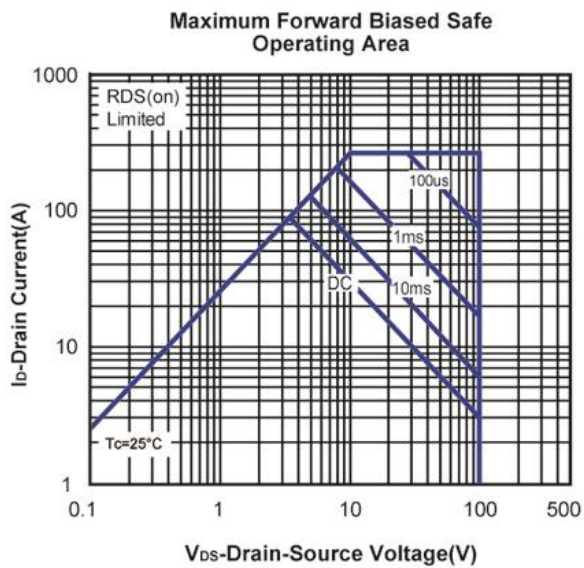
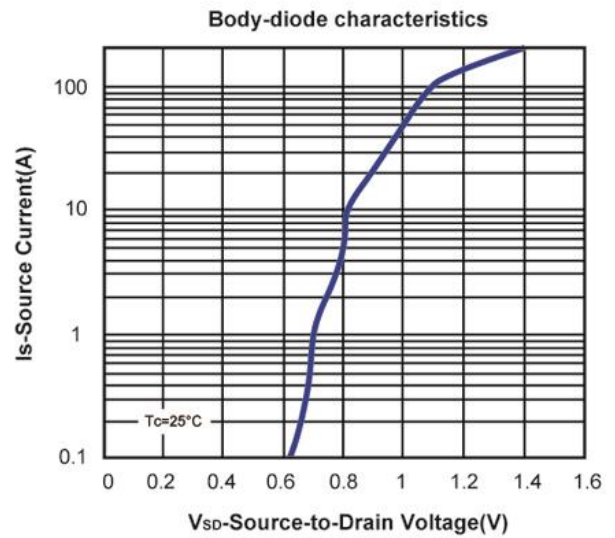
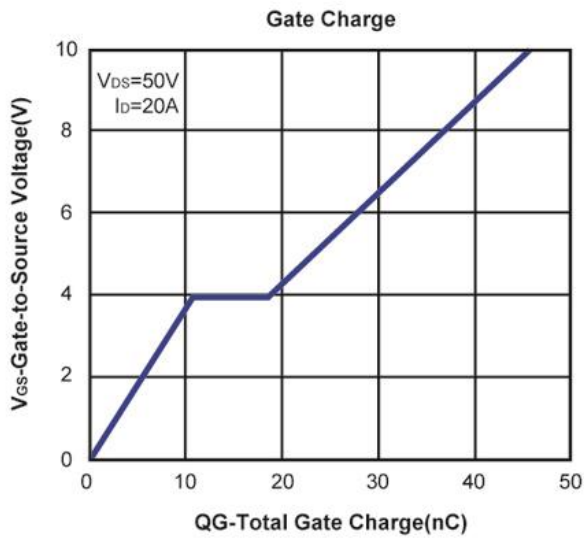


On-Region Characteristics

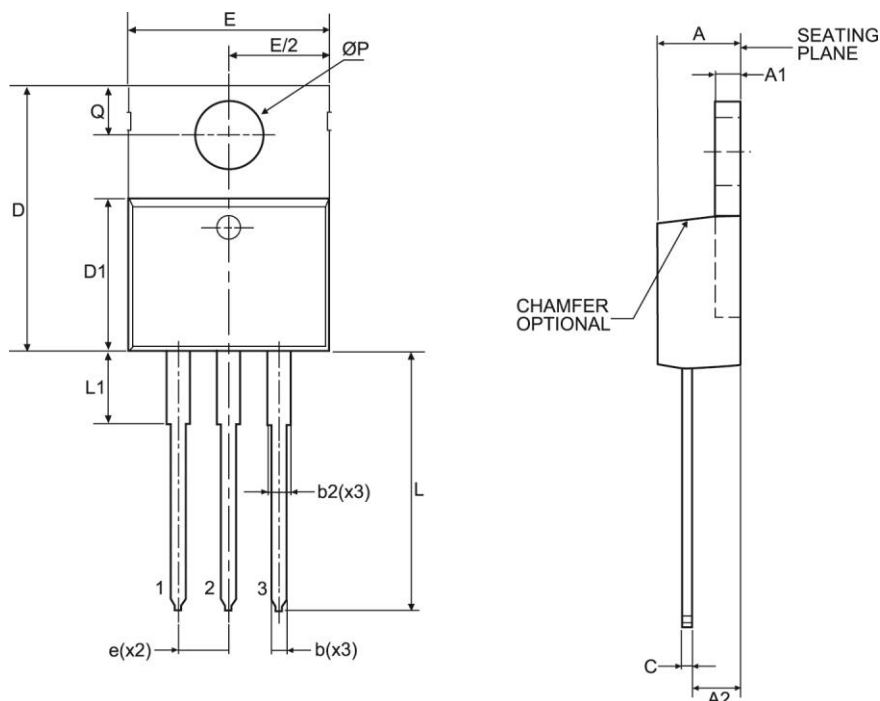


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Typical Characteristics (T_J =25°C Noted)



TO220 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	3.50	4.90
A1	1.00	1.40
A2	2.00	3.00
b	0.70	1.40
c	0.35	0.65
D	14.00	16.50
D1	8.30	9.50
E	9.60	10.70
e	2.54 BSC	
L	12.50	15.00
ØP	3.60 TYP	
Q	2.50	3.10
b2	1.10	1.80
L1	2.40	3.20

