ME50P06P/ME50P06P-G

P- Channel 60-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME50P06P is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 17m\Omega @ V_{GS}=-10V$
- $R_{DS(ON)} \leqq 20m\Omega @ V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

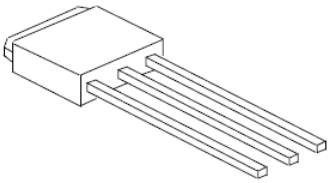
APPLICATIONS

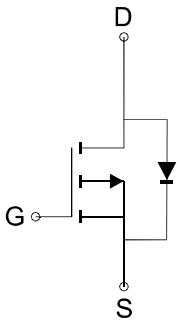
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-251)

Top View





P-Channel MOSFET

Ordering Information: ME50P06P (Pb-free)

ME50P06P-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	-60	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	-61	A
	T_C=70℃		-49	
Pulsed Drain Current		I_{DM}	-244	A
Maximum Power Dissipation*	T_C=25℃	P_D	114	W
	T_C=70℃		73	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{stg}	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	1.1	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1		-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-60V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=-10V, I_D= -17A		14	17	mΩ
		V_{GS}=-4.5V, I_D= -14A		16	20	
V_{SD}	Diode Forward Voltage	I_S=-17A, V_{GS}=0V		-0.9	-1.2	V
DYNAMIC						
Qg	Total Gate Charge(10V)	V_{DS}=-30V, V_{GS}=-10V, I_D=-50A		94		nC
Qg	Total Gate Charge(4.5V)	V_{DS}=-30V, V_{GS}=-4.5V, I_D=-50A		46		
Qgs	Gate-Source Charge			18		
Qgd	Gate-Drain Charge			24		
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, F=1MHz		4130		pF
Coss	Output Capacitance			420		
Crss	Reverse Transfer Capacitance			145		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-30V, R_L =30Ω V_{GEN}=-10V, R_G=6Ω		53		ns
t_r	Turn-On Rise Time			19		
$t_{d(off)}$	Turn-Off Delay Time			221		
t_f	Turn-On Fall Time			61		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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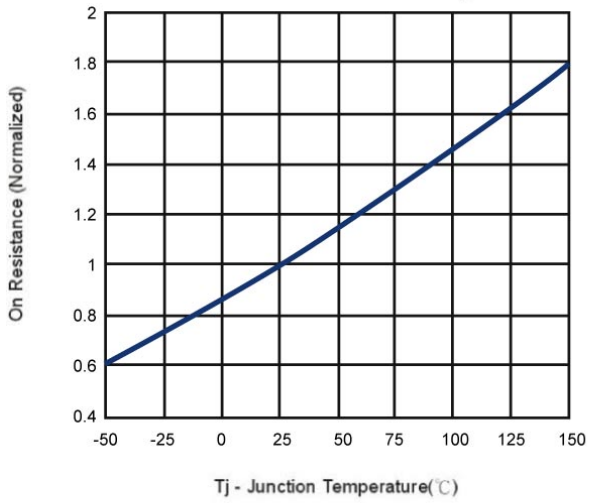
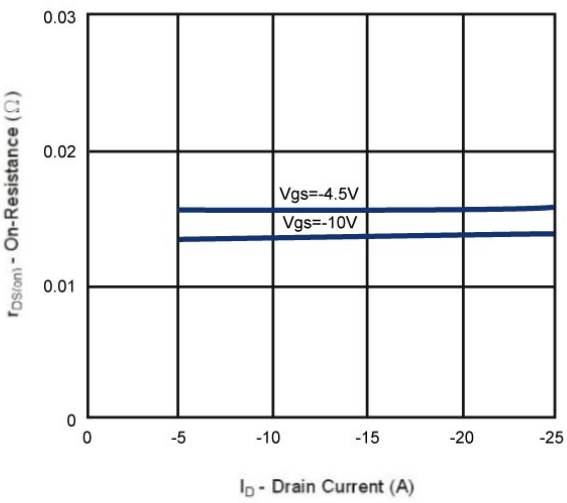
Typical Characteristics (T_J =25℃ Noted)

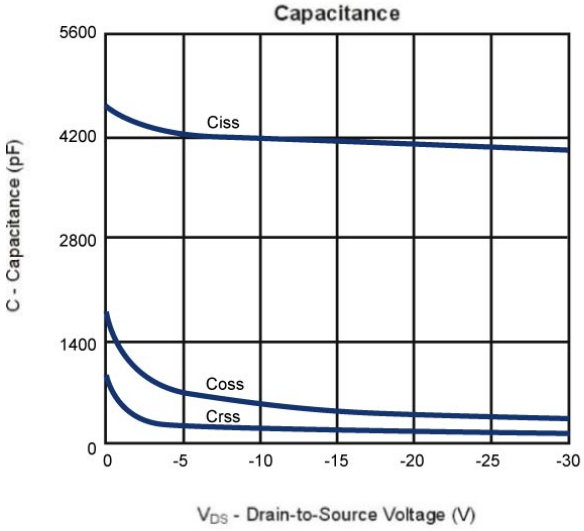
On Resistance vs. Junction Temperature



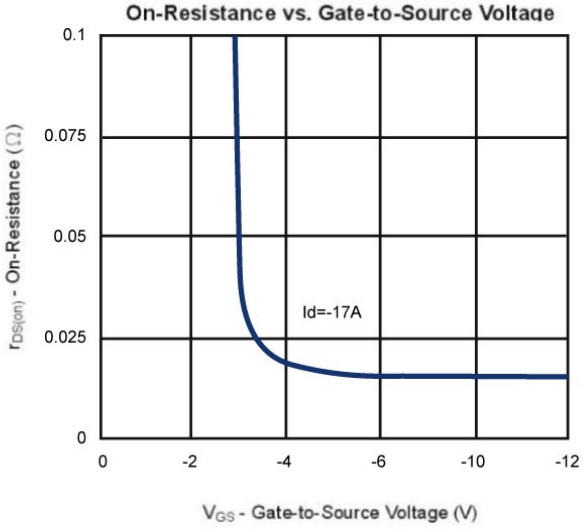
On-Resistance vs. Drain Current



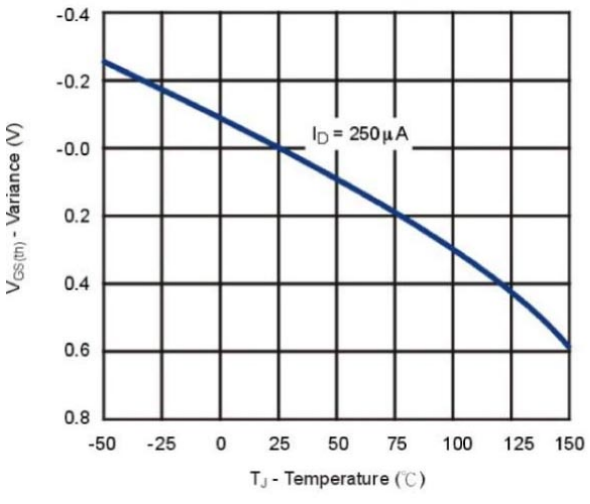
Capacitance



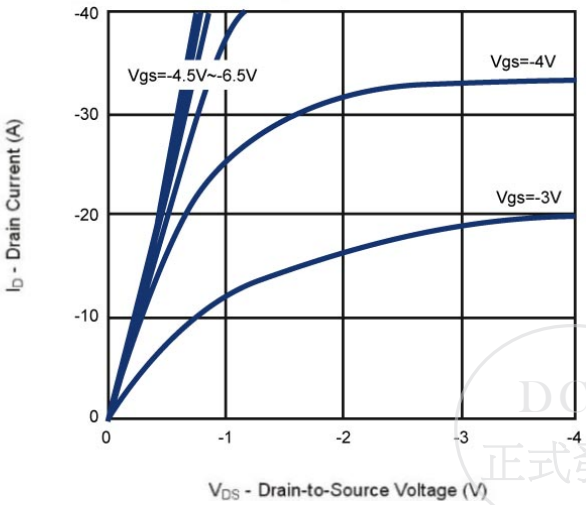
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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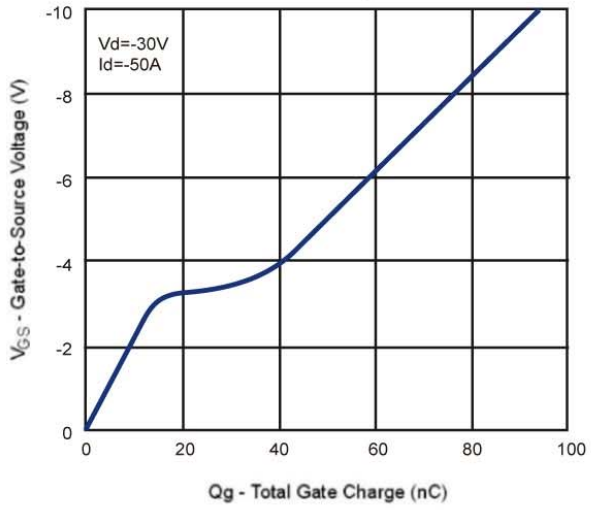
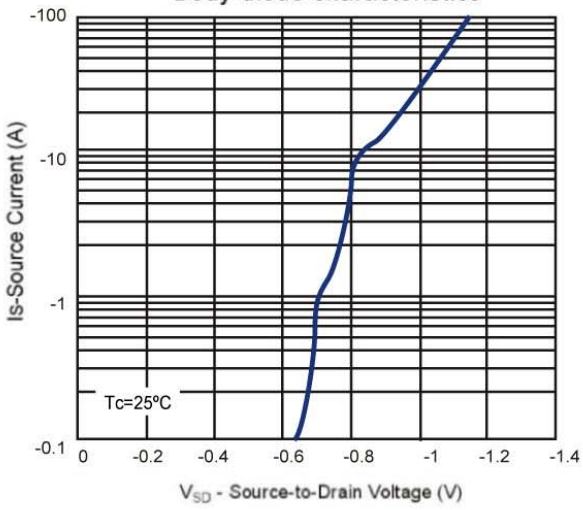
Typical Characteristics (T_J =25℃ Noted)

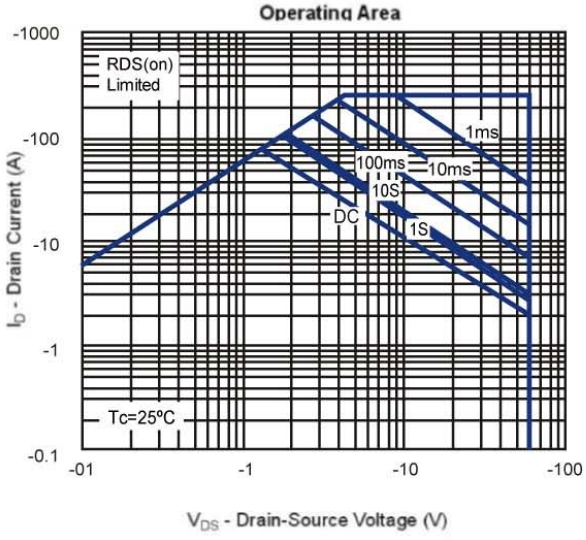
Gate Charge



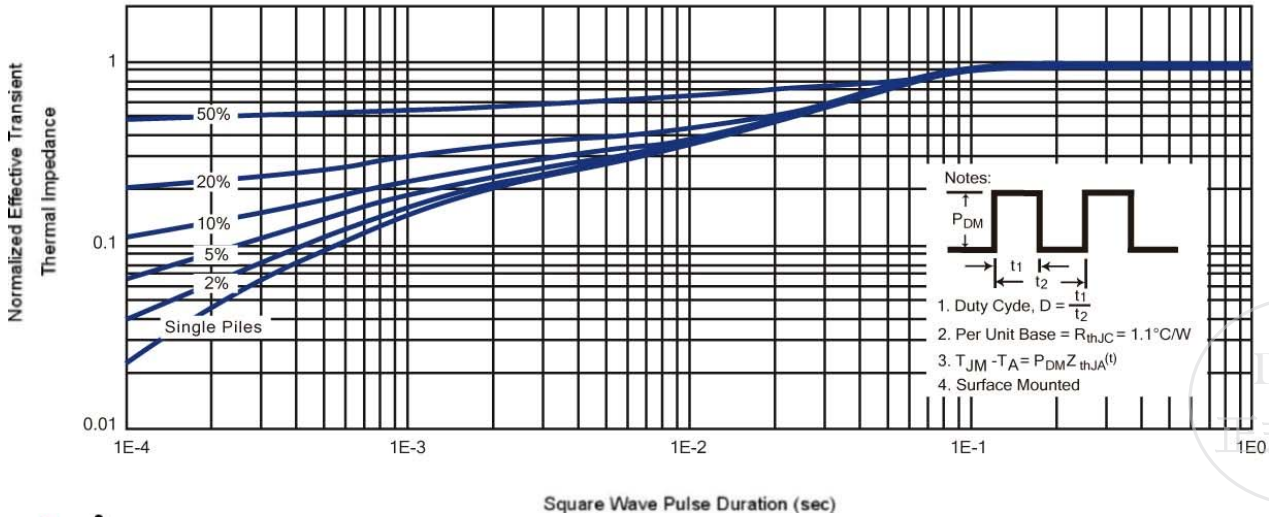
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



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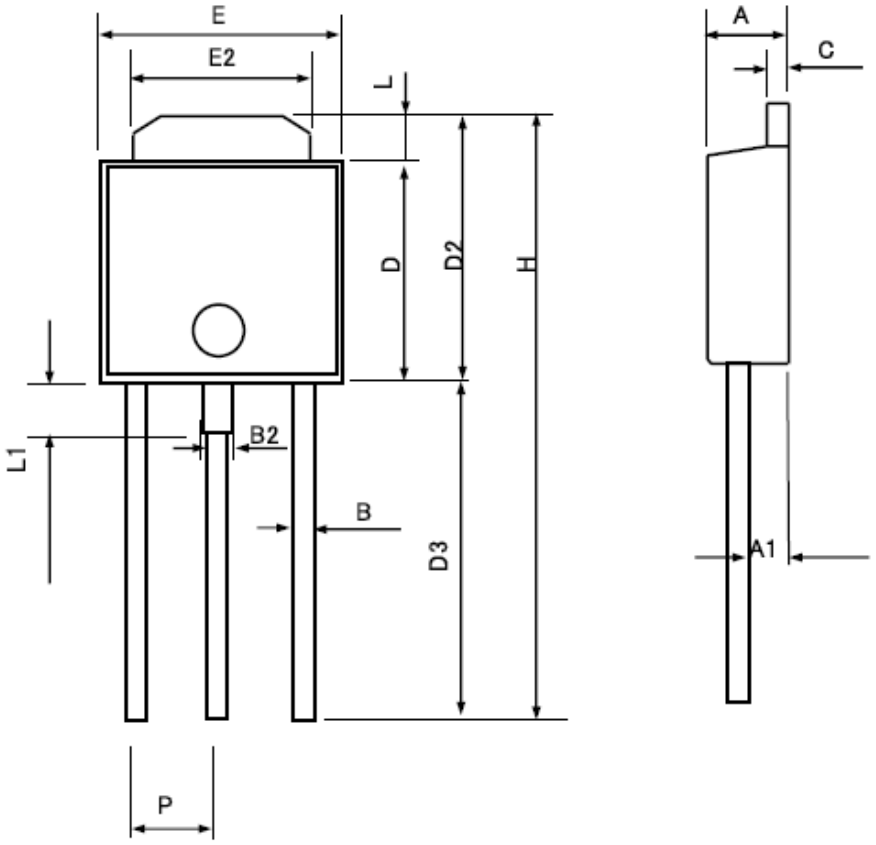
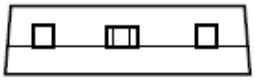
TO-251 Package Outline





SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	2.10	2.50
A1	1.10	1.30
B	0.40	0.88
B2	0.60	1.14
C	0.40	0.60
D	5.30	6.23
D2	6.60	7.30
D3	3.98	8.00
H	10.98	15.0
E	6.30	6.74
E2	4.80	5.46
L	1.30	1.70
L1	0.91	1.80
P	2.30	2.40