ME5937ED/ ME5937ED-G

Dual P-Channel 12-V (D-S) MOSFET，ESD Protected

GENERAL DESCRIPTION

The ME5937ED is the Dual P-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and lower power loss that are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 62m\Omega @ V_{GS}=-4.5V$
- $R_{DS(ON)} \leqq 77m\Omega @ V_{GS}=-2.5V$
- $R_{DS(ON)} \leqq 110m\Omega @ V_{GS}=-1.8V$
- $R_{DS(ON)} \leqq 180m\Omega @ V_{GS}=-1.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC

PIN CONFIGURATION

(DFN 2x3 NEP)

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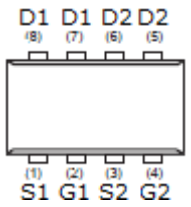

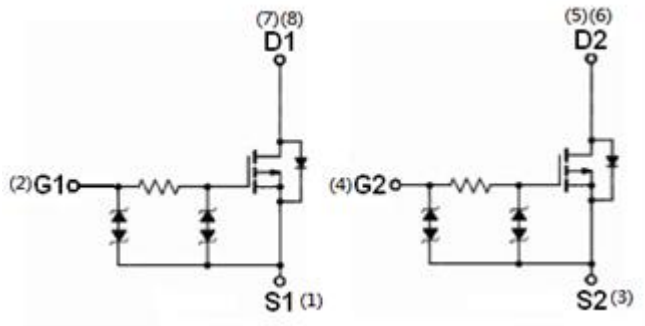

Ordering Information: ME5937ED (Pb-free)

ME5937ED-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-12	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current*	T_A=25℃	I_D	-3.3	A
	T_A=70℃		-2.7	
Pulsed Drain Current		I_{DM}	-13.5	A
Maximum Power Dissipation*	T_A=25℃	P_D	1.1	W
	T_A=25℃		0.7	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Junction-to-Ambient Thermal Resistance*		$R_{\theta JA}$	110	℃/W

*The device mounted on 1in2 FR4 board with 2 oz copper

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Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-12			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.3		-1.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-12V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=-4.5V, I_D= -2.5A		40	62	mΩ
		V_{GS}=-2.5V, I_D= -1.2A		48	77	
		V_{GS}=-1.8V, I_D= -1.2A		60	110	
		V_{GS}=-1.5V, I_D= -0.5A		78	180	
V_{SD}	Diode Forward Voltage	Is=-2.5A, V_{GS}=0V,			-1.2	V
DYNAMIC						
Ciss	Input capacitance	V_{DS}=-6V, V_{GS}=0V, f=1.0MHz		170		pF
Coss	Output Capacitance			122		
Crss	Reverse Transfer Capacitance			14		
Qg	Total Gate Charge	V_{DS}=-6V, V_{GS}=-4.5V, I_D=-2.5A		13		nC
Qgs	Gate-Source Charge			1.1		
Qgd	Gate-Drain Charge			2.4		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-10V, R_L =2.5Ω R_{GEN}=3Ω, V_{GS}=-4.5V		560		ns
tr	Turn-On Rise Time			4000		
$t_{d(off)}$	Turn-Off Delay Time			400		
t_f	Turn-Off Fall Time			4000		

Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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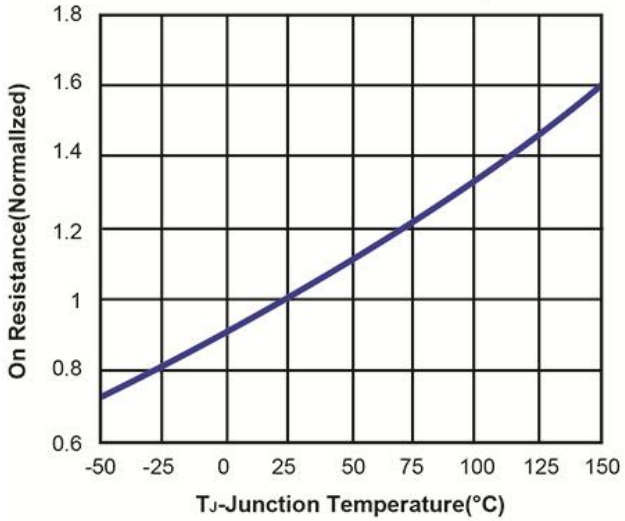
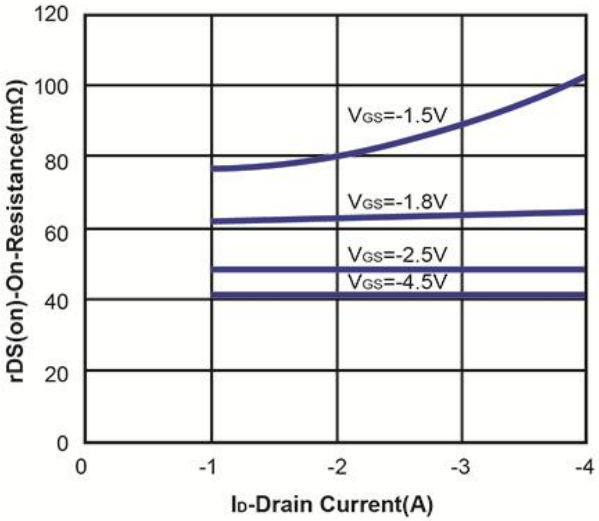
Typical Characteristics (T_J =25℃ Noted)

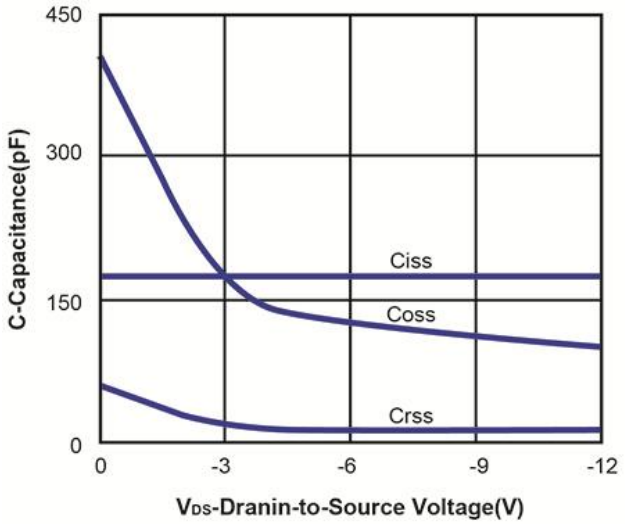
On Resistance vs. Junction Temperature



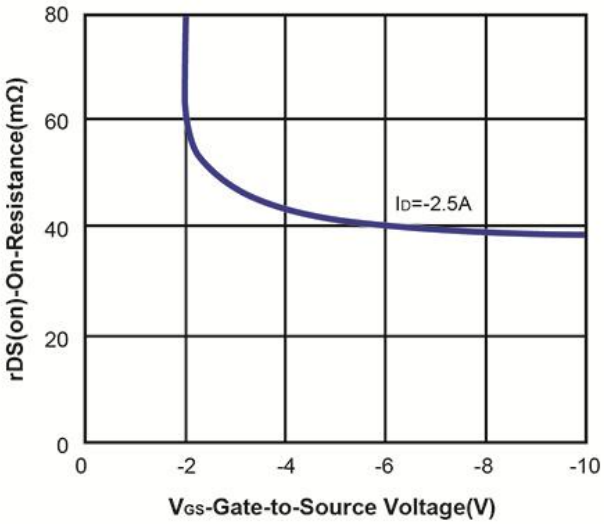
On Resistance vs. Drain Current



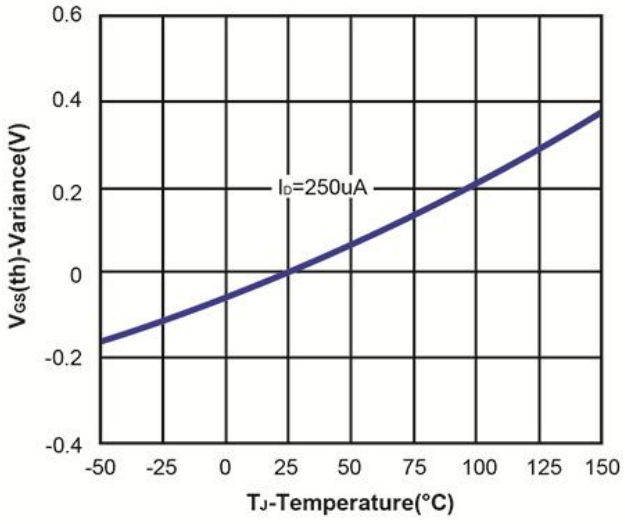
Capacitance



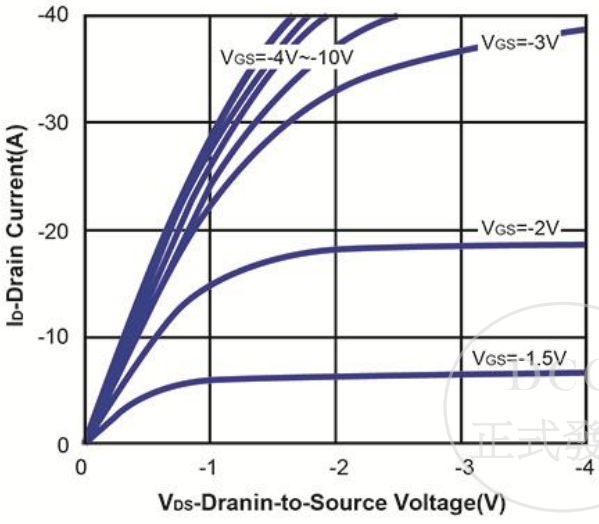
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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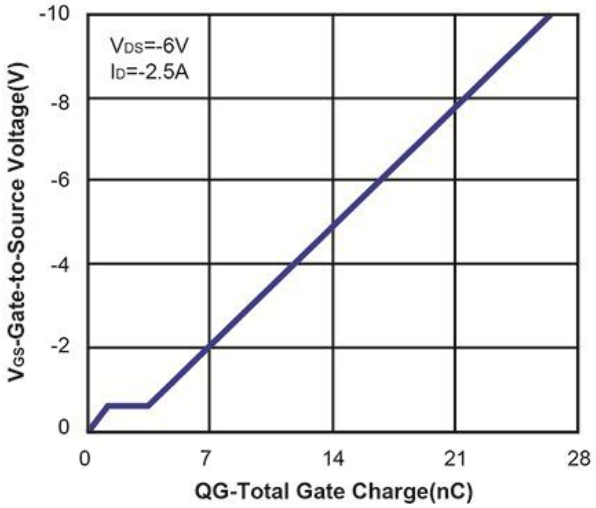
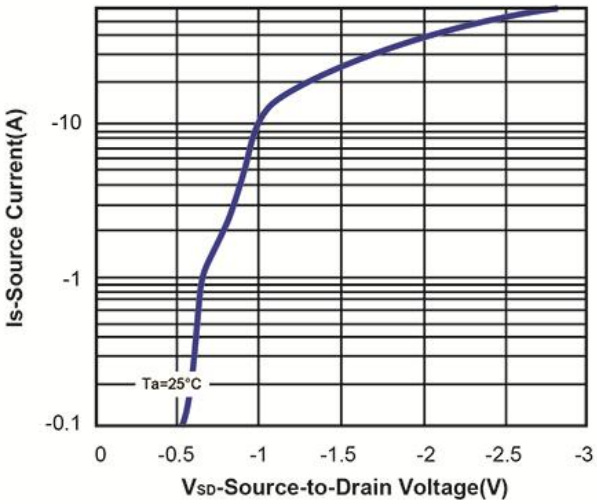
Typical Characteristics (T_J =25℃ Noted)

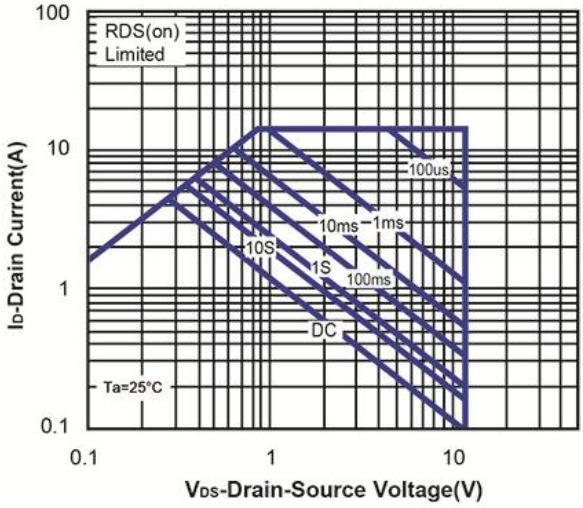
Gate Charge



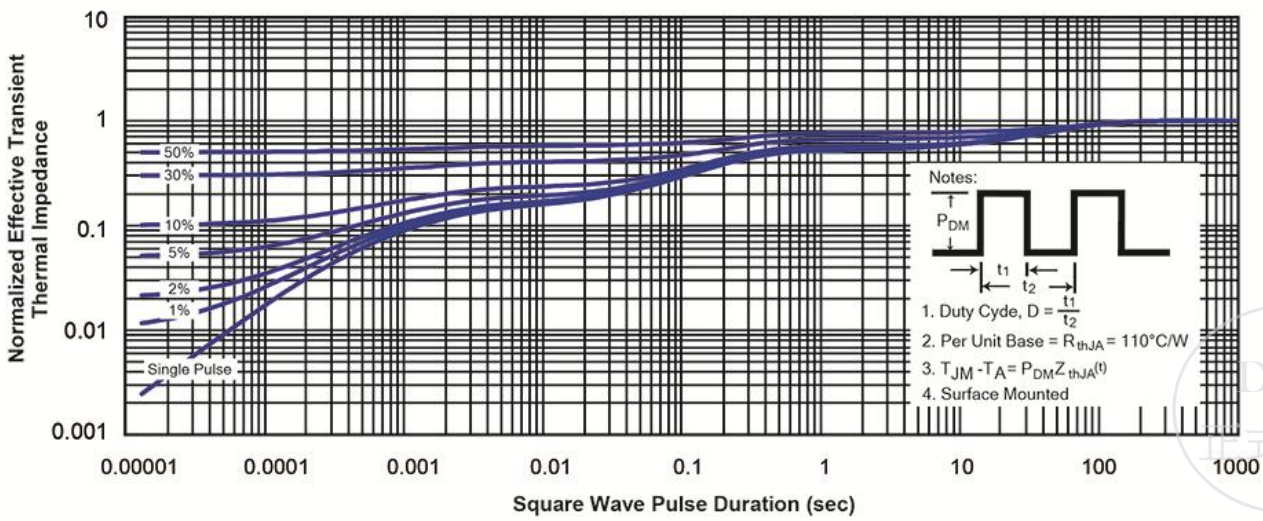
Body-diode characteristics



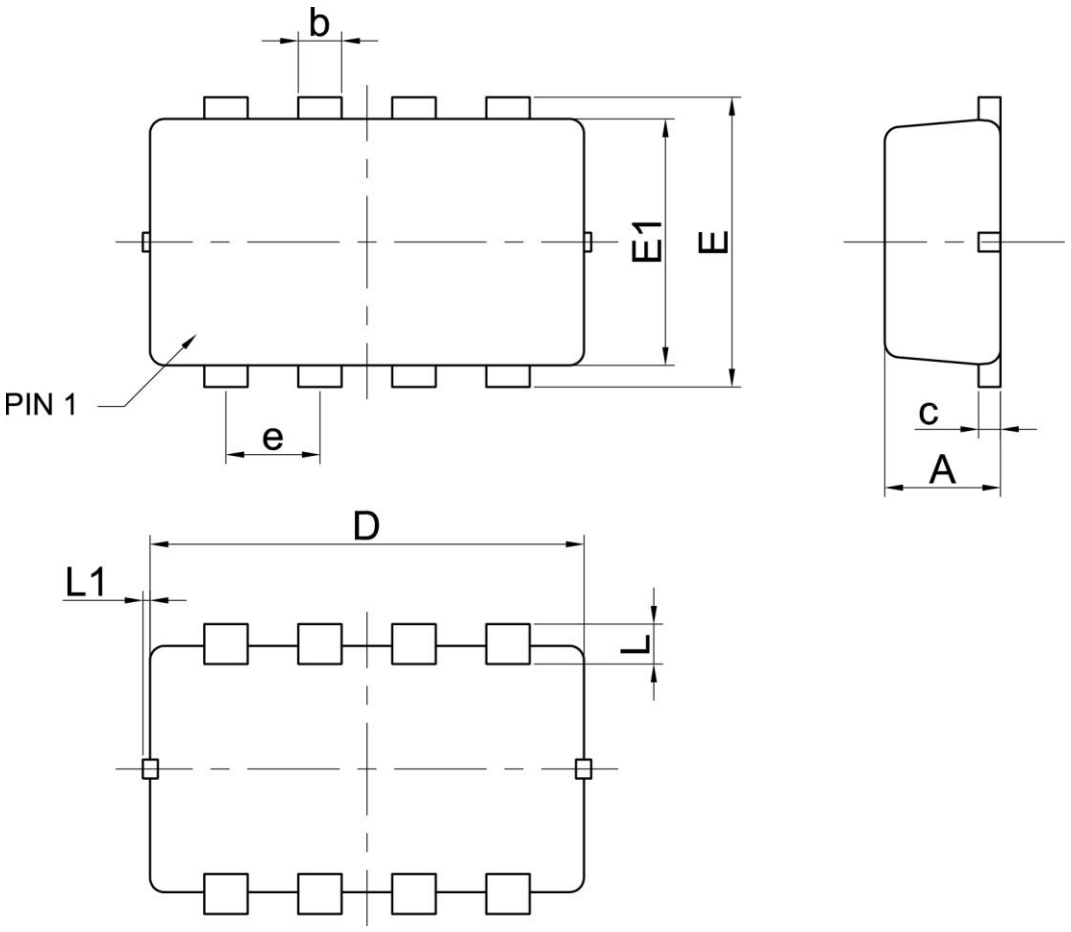
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



DFN 3x2 NEP Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.70	0.90
b	0.24	0.35
c	0.08	0.20
D	2.90	3.10
E	1.90	2.10
E1	1.60	1.75
e	0.65 BCS	
L	0.20	0.45
L1	0	0.10