

30V N-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The ME60N03 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as LCD inverter, computer power management and DC to DC converter circuits which need low in-line power loss.

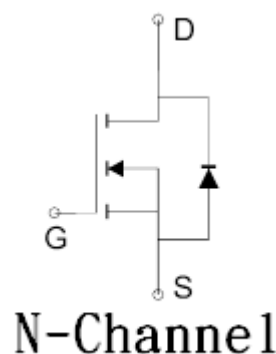
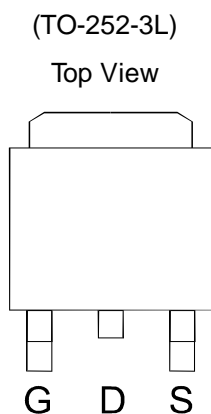
FEATURES

- $R_{DS(ON)} \leq 8.5m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 13m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- Secondary Synchronous Rectification

PIN CONFIGURATION



Ordering Information: ME60N03 (Pb-free)

ME60N03-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	30	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	$T_c=25^\circ C$	I_D	48.5	A
	$T_c=70^\circ C$			
Pulsed Drain Current		I_{DM}	60.6	A
Maximum Power Dissipation	$T_c=25^\circ C$	P_D	50	W
	$T_c=70^\circ C$		32	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Thermal Resistance-Junction to Case		$R_{\theta JC}$	2.5	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1	1.6	3	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =10V, I _D =30A		6.5	8.5	mΩ
		V _{GS} =4.5V, I _D =20A		10	13	
V _{SD}	Diode Forward Voltage	I _S =20A, V _{GS} =0V		0.87	1.5	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =35A		22		nC
Q _{gs}	Gate-Source Charge			4.5		
Q _{gd}	Gate-Drain Charge			4		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		1219		pF
C _{oss}	Output Capacitance			182		
C _{rss}	Reverse Transfer Capacitance			88		
t _{d(on)}	Turn-On Delay Time	V _{DS} =15V, V _{GS} =10V R _G =24Ω, R _L =15Ω, I _D =1A		13		ns
t _r	Turn-On Rise Time			10		
t _{d(off)}	Turn-Off Delay Time			46		
t _f	Turn-Off Fall Time			7		

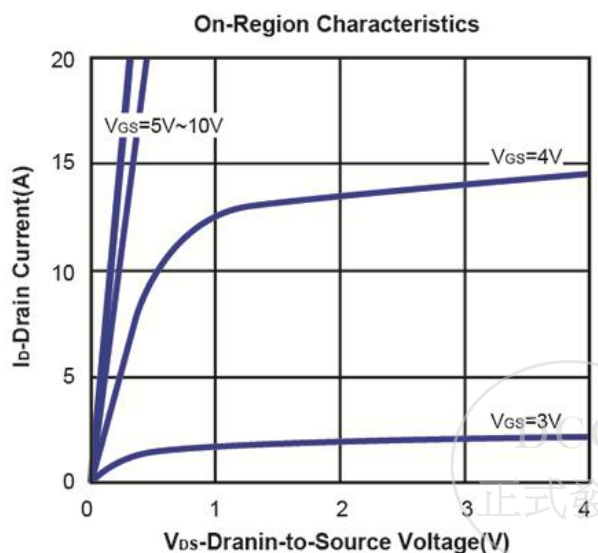
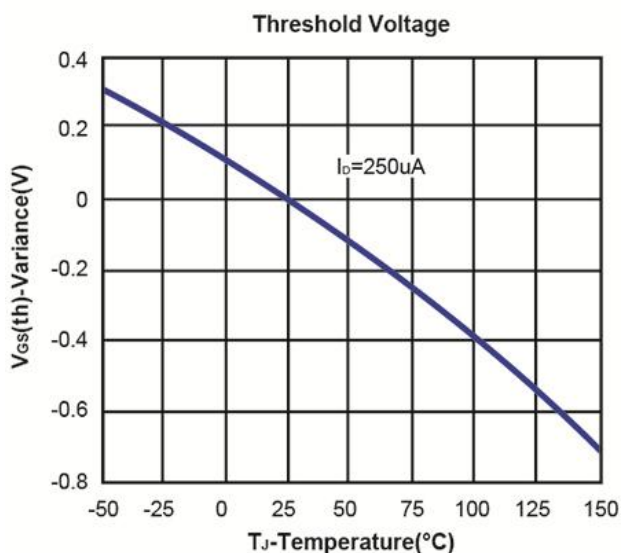
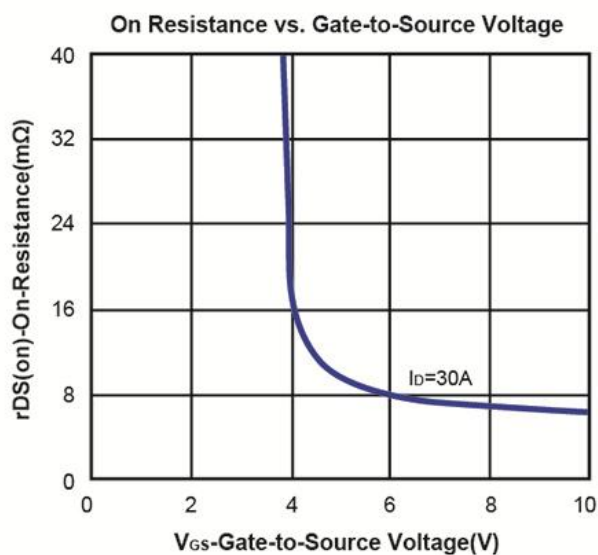
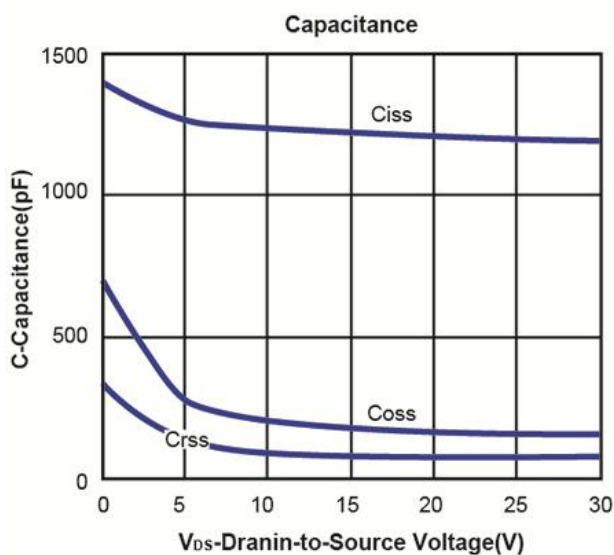
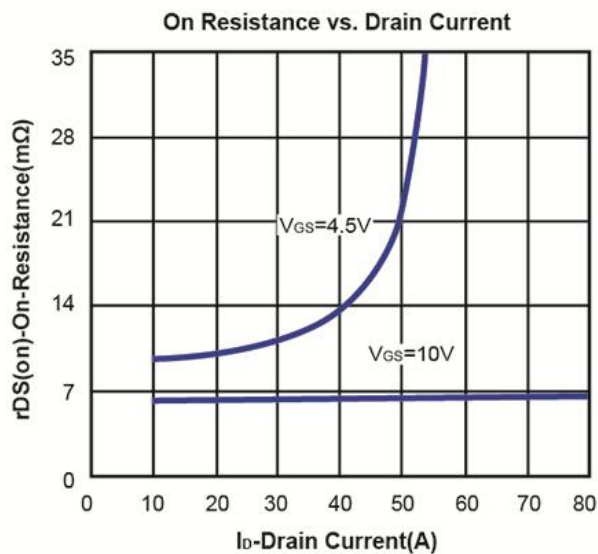
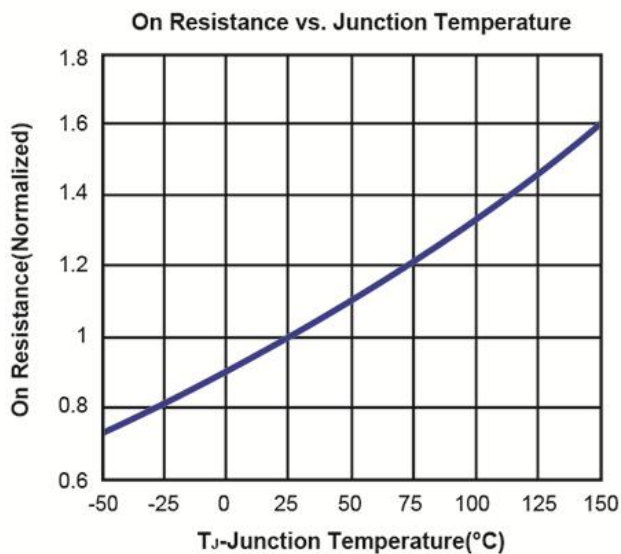
Note: a. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



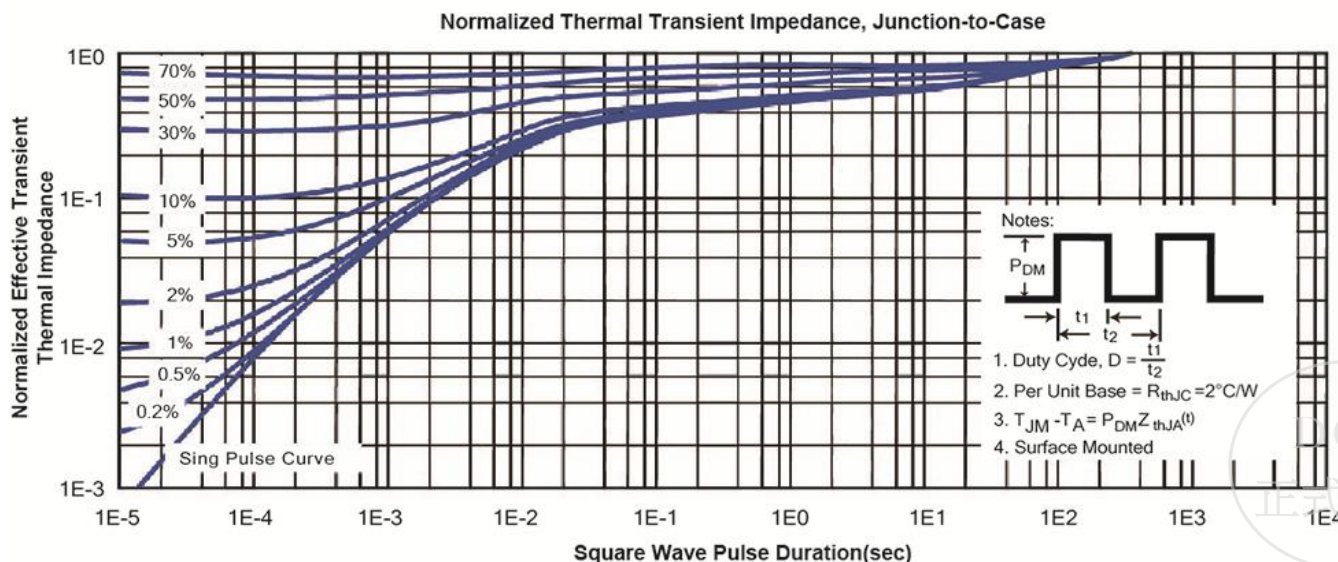
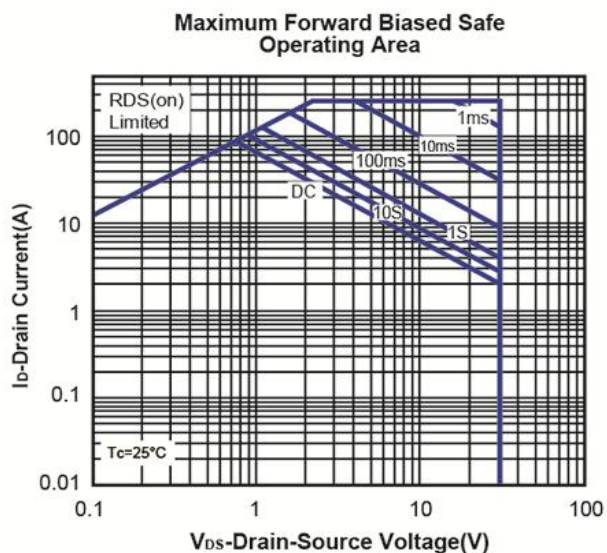
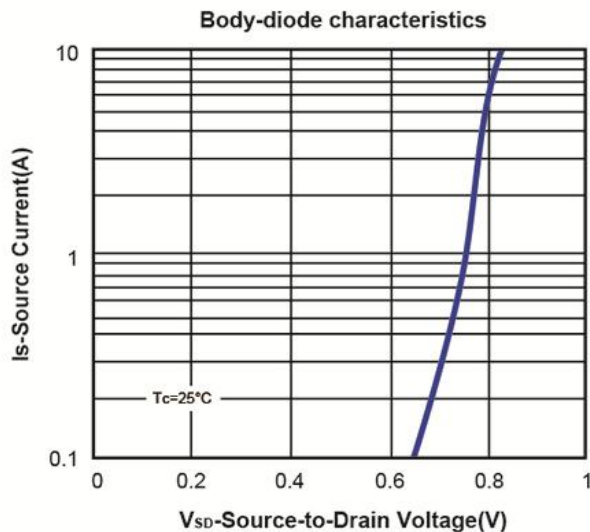
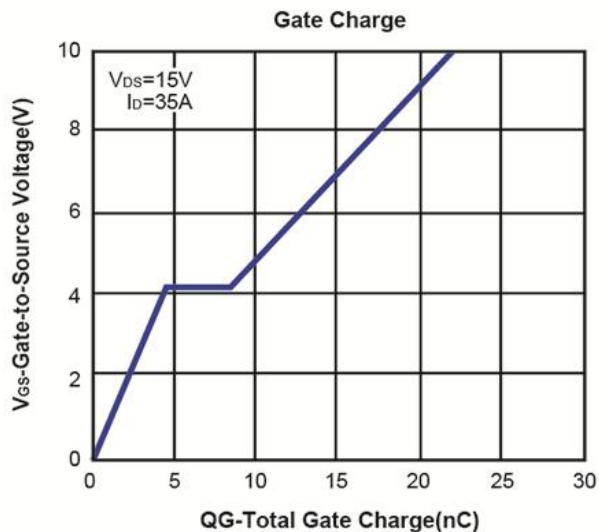
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Typical Characteristics (T_J = 25°C Noted)

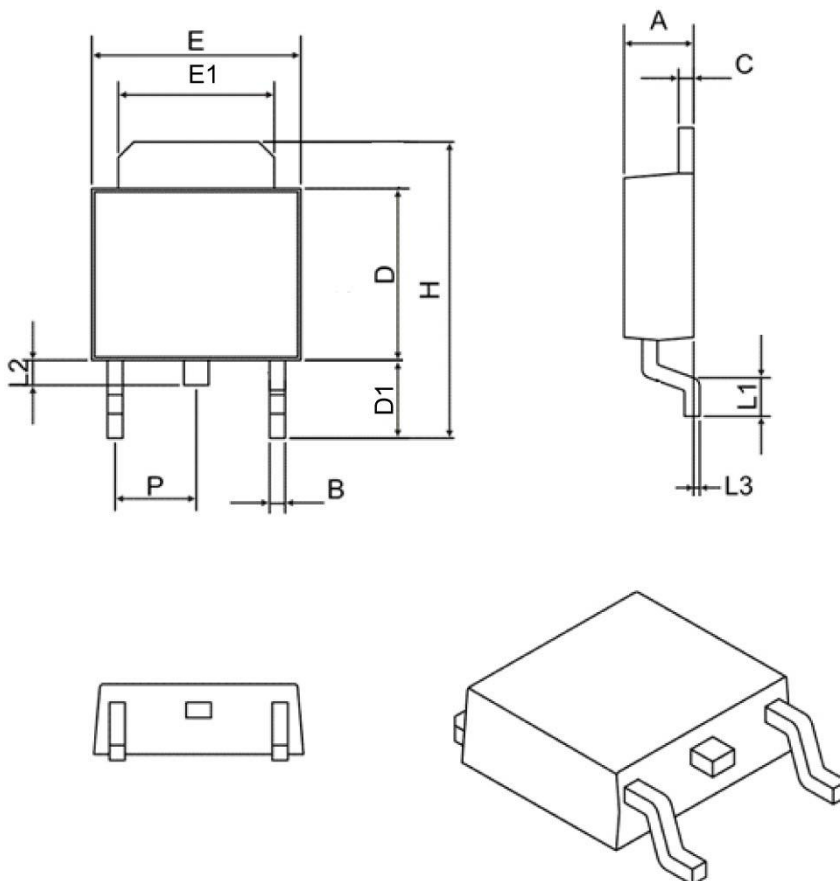


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Typical Characteristics (T_J =25°C Noted)



TO-252-3L Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

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