

## N-Channel 40-V (D-S) MOSFET

### GENERAL DESCRIPTION

The ME60N04 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as LCD inverter, computer power management and DC to DC converter circuits which need low in-line power loss.

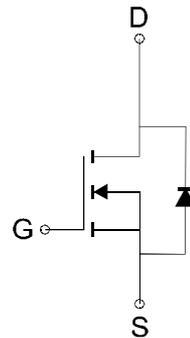
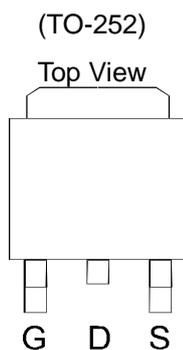
### FEATURES

- $R_{DS(ON)} \leq 12m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 17m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

### APPLICATIONS

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- Secondary Synchronous Rectification

### PIN CONFIGURATION



N-Channel MOSFET

### Absolute Maximum Ratings ( $T_A=25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	Steady	Unit
Drain-Source Voltage	$V_{DSS}$	40	V
Gate-Source Voltage	$V_{GSS}$	$\pm 20$	V
Continuous Drain Current ( $T_j=150^\circ C$ , limited by package)	$I_D$	$T_C=25^\circ C$	20
		$T_A=25^\circ C$	12
Pulsed Drain Current	$I_{DM}$	50	A
Avalanche Energy with Single Pulse( $L=1mH$ )	EAS	40	mJ
Maximum Power Dissipation (Note A)	$P_D$	$T_C=25^\circ C$	30
		$T_A=25^\circ C$	3
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient(Note A)	$R_{\theta JA}$	42	$^\circ C/W$
Thermal Resistance-Junction to Case(Note A)	$R_{\theta JC}$	4.3	$^\circ C/W$

Note A: The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper

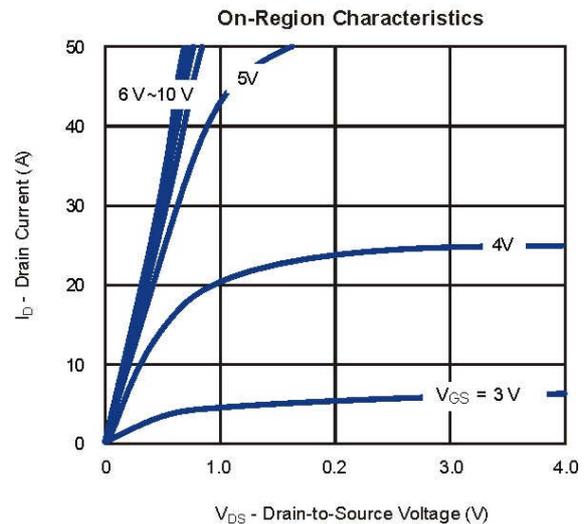
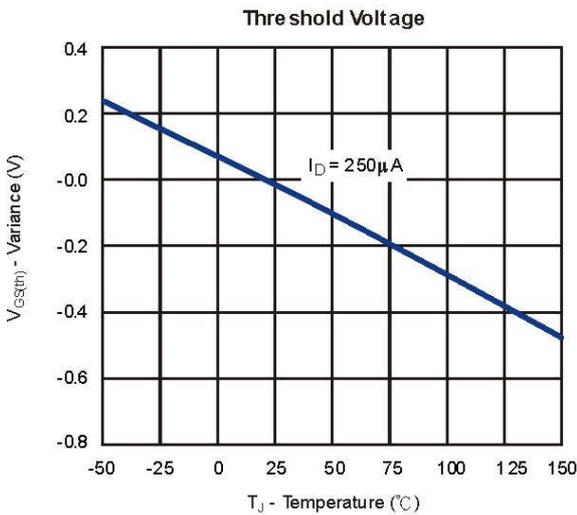
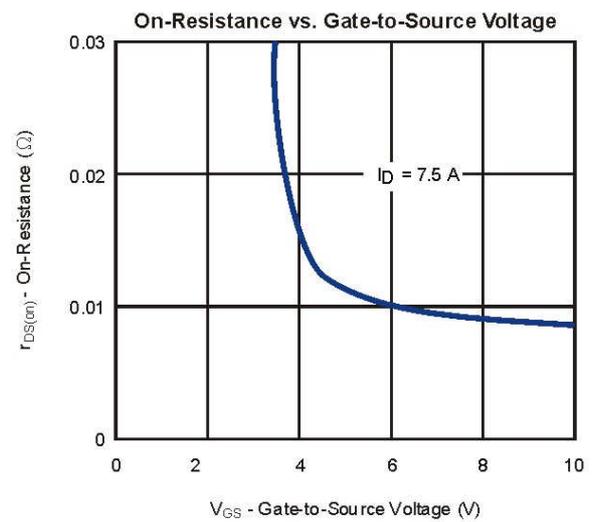
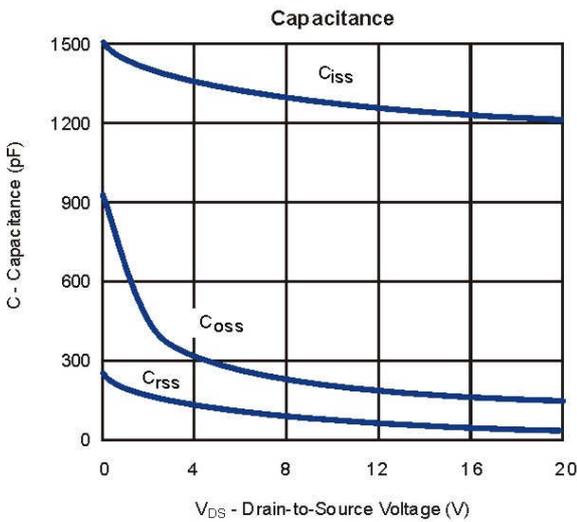
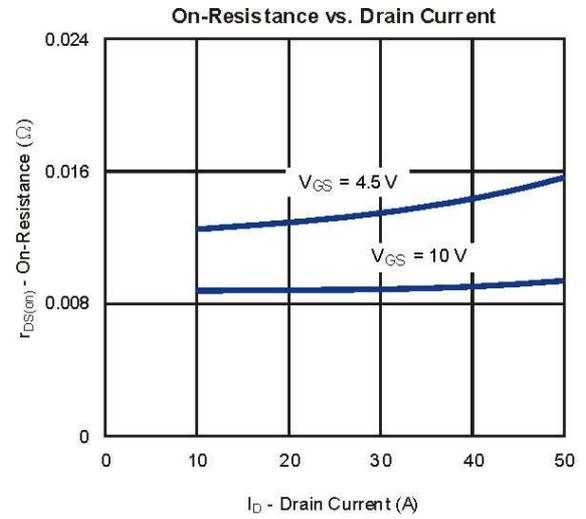
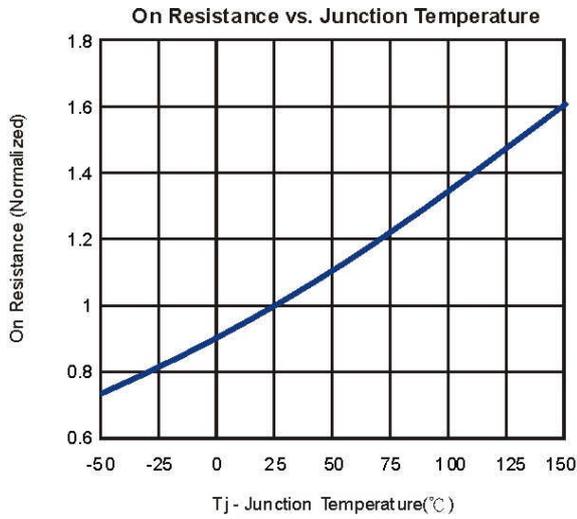
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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

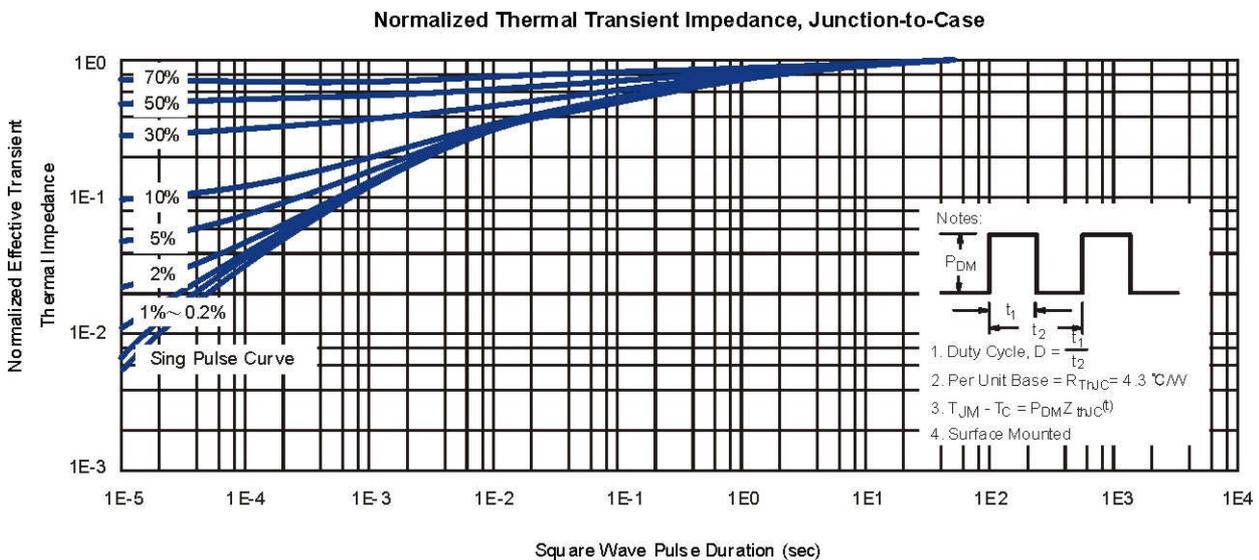
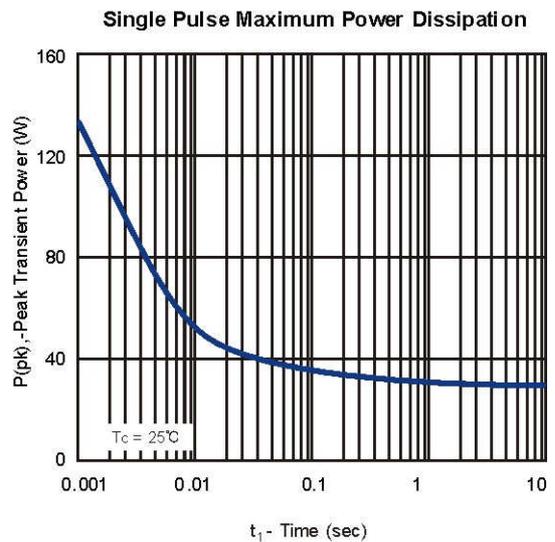
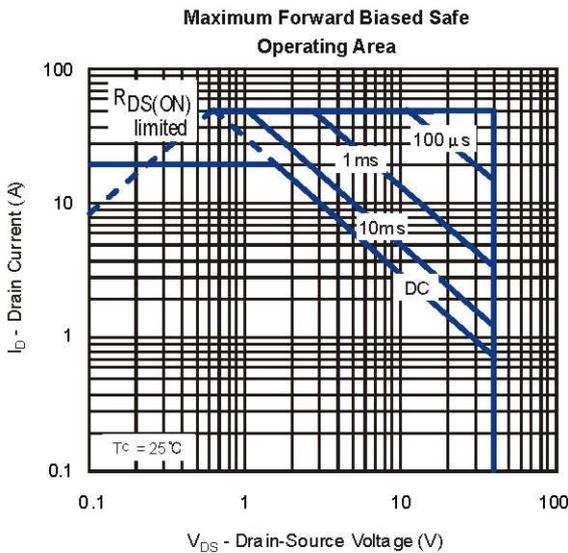
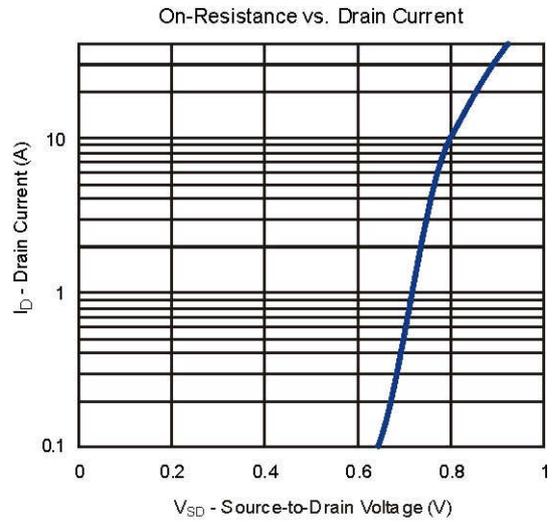
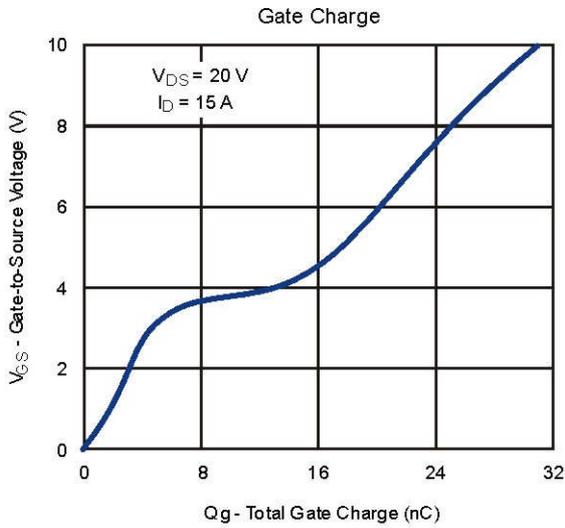
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>STATIC</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	40			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	1	1.9	3	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V			1	μA
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance <sup>a</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =15A		9	12	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =13A		13	17	
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =15A, V <sub>GS</sub> =0V		0.8	1.2	V
<b>DYNAMIC</b>						
Q <sub>g</sub> (TOT)	Total Gate Charge, V <sub>GS</sub> =10V	V <sub>DS</sub> =20V, I <sub>D</sub> =15A		31	36	nC
Q <sub>g</sub>	Total Gate Charge, V <sub>GS</sub> =4.5V			16	18	
Q <sub>gs</sub>	Gate-Source Charge			6.5		
Q <sub>gd</sub>	Gate-Drain Charge			8.3		
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> =V <sub>DS</sub> =0V, f=1MHz		1.6		Ω
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V, f=1MHz		1240	1500	pF
C <sub>oss</sub>	Output Capacitance			170		
C <sub>rss</sub>	Reverse Transfer Capacitance			60		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =20V, I <sub>D</sub> =1A V <sub>GS</sub> =10V, R <sub>GEN</sub> =6Ω		16	20	ns
t <sub>r</sub>	Turn-On Rise Time			13	17	
t <sub>d(off)</sub>	Turn-Off Delay Time			60	75	
t <sub>f</sub>	Turn-On Fall Time			7	10	

Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

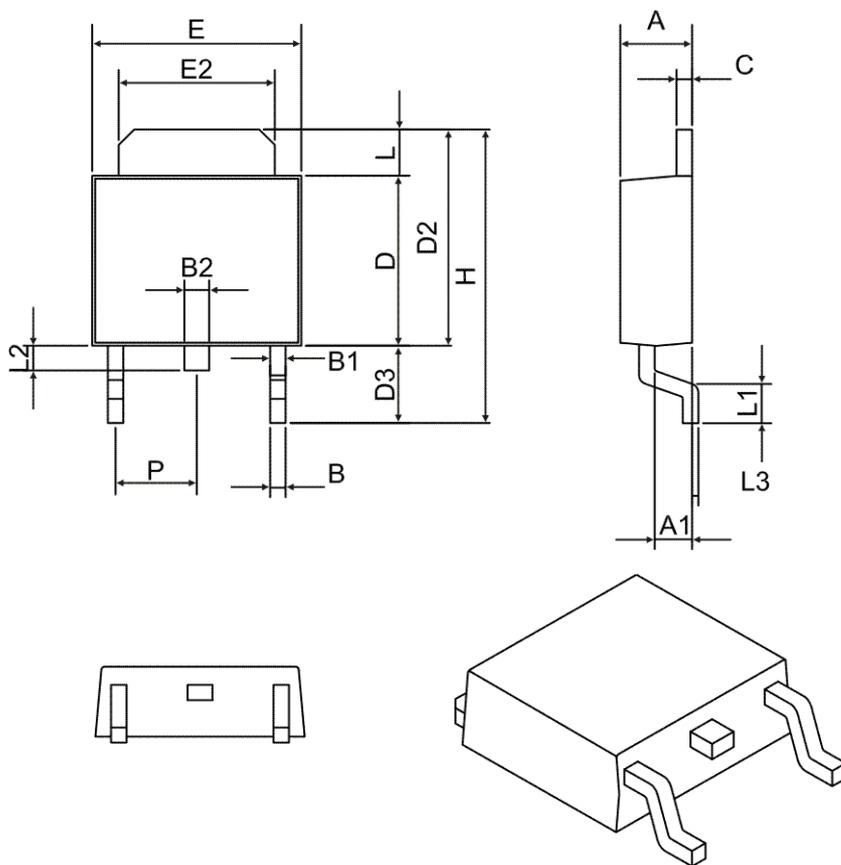
### Typical Characteristics (T<sub>J</sub> = 25°C Noted)



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### TO-252 Package Outline



SYMBOL	MILLIMETERS	
	MIN	MAX
A	2.00	2.50
A1	1.1	1.3
B	0.30	0.70
B1	0.40	0.80
B2	0.60	1.00
C	0.40	0.60
D	5.30	5.70
D2	6.70	7.30
D3	2.20	3.00
H	9.20	9.80
E	6.30	6.70
E2	4.80	5.20
L	1.30	1.70
L1	0.90	1.50
L3	0	0.30
P	2.40	2.80