

P- Channel 60-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME60P06T is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

- $R_{DS(ON)} \leq 16.5m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 20.5m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

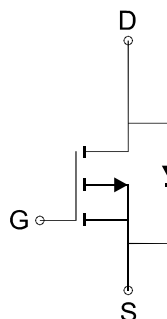
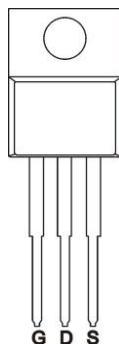
APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-220)

Top View



P-Channel MOSFET

Ordering Information: ME60P06T (Pb-free)

ME60P06T-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current*	Tc=25°C	I_D	-55.3	A
	Tc=70°C		-46.3	
Pulsed Drain Current		I_{DM}	-221	A
Maximum Power Dissipation*	Tc=25°C	P_D	90.9	W
	Tc=70°C		63.6	
Operating Junction Temperature		T_J	-55 to 175	°C
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	1.65	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (T_c =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1		-3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-60V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =-10V, I _D = -30A		13	16.5	mΩ
		V _{GS} =-4.5V, I _D = -20A		15	20.5	
V _{SD}	Diode Forward Voltage	I _S =-30A, V _{GS} =0V		-1.0	-1.5	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-30V, V _{GS} =-10V, I _D =-50A		98.6		nC
Q _g	Total Gate Charge	V _{DS} =-30V, V _{GS} =-4.5V, I _D =-50A		50.1		
Q _{gs}	Gate-Source Charge			15.9		
Q _{gd}	Gate-Drain Charge			25.2		
C _{iss}	Input capacitance	V _{DS} =-15V, V _{GS} =0V, F=1MHz		4480		pF
C _{oss}	Output Capacitance			427		
C _{rss}	Reverse Transfer Capacitance			355		
t _{d(on)}	Turn-On Delay Time	V _{DS} =-30V, R _L =30Ω V _{GEN} =-10V, R _G =6Ω		50.7		ns
t _r	Turn-On Rise Time			18.1		
t _{d(off)}	Turn-Off Delay Time			221		
t _f	Turn-Off Fall Time			60.1		

Notes:a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%

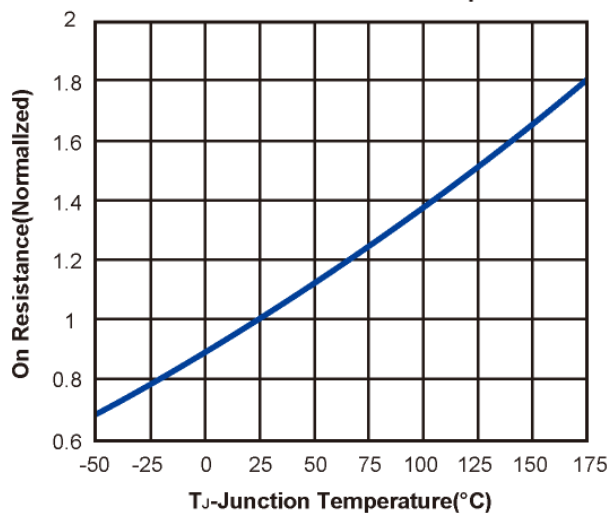
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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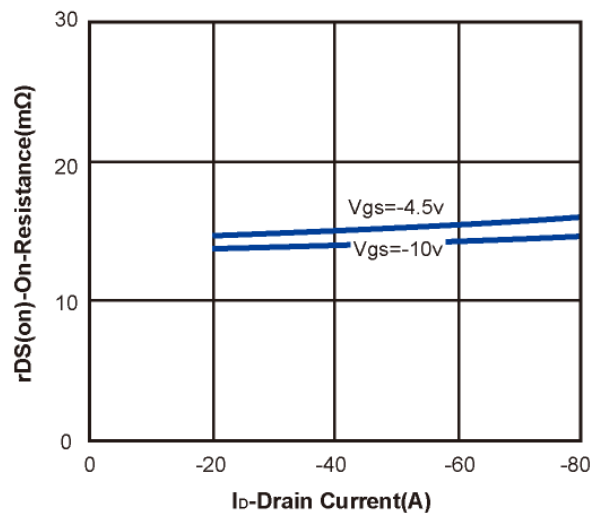
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Typical Characteristics (T_J =25°C Noted)

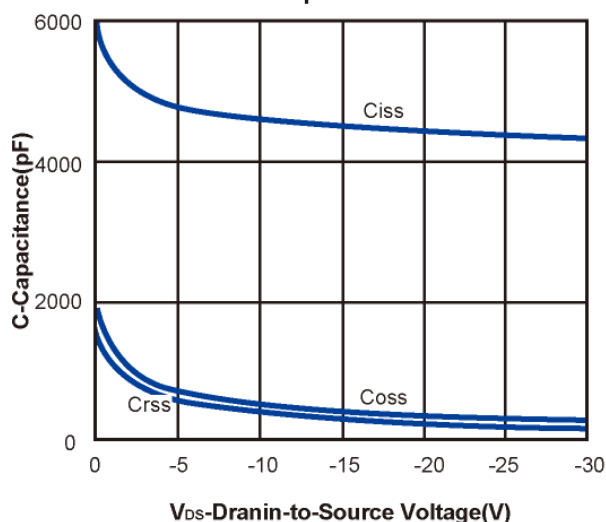
On Resistance vs. Junction Temperature



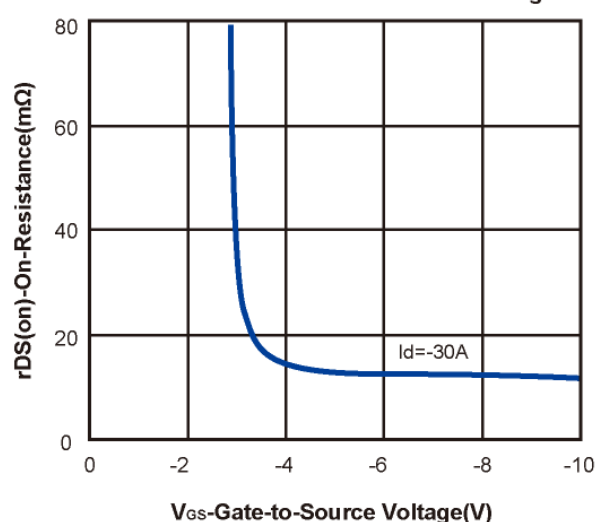
On Resistance vs. Drain Current



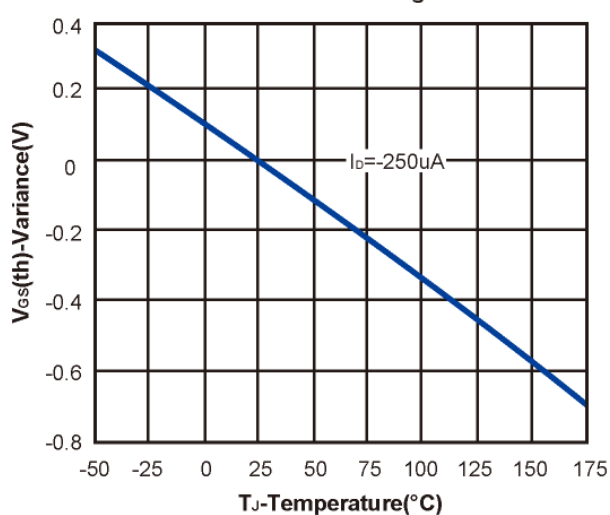
Capacitance



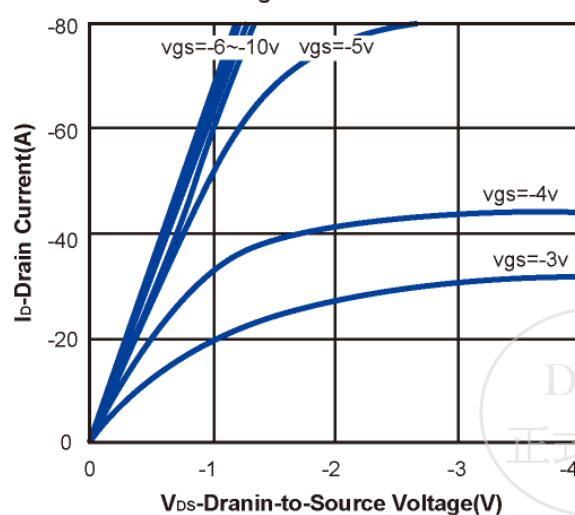
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage

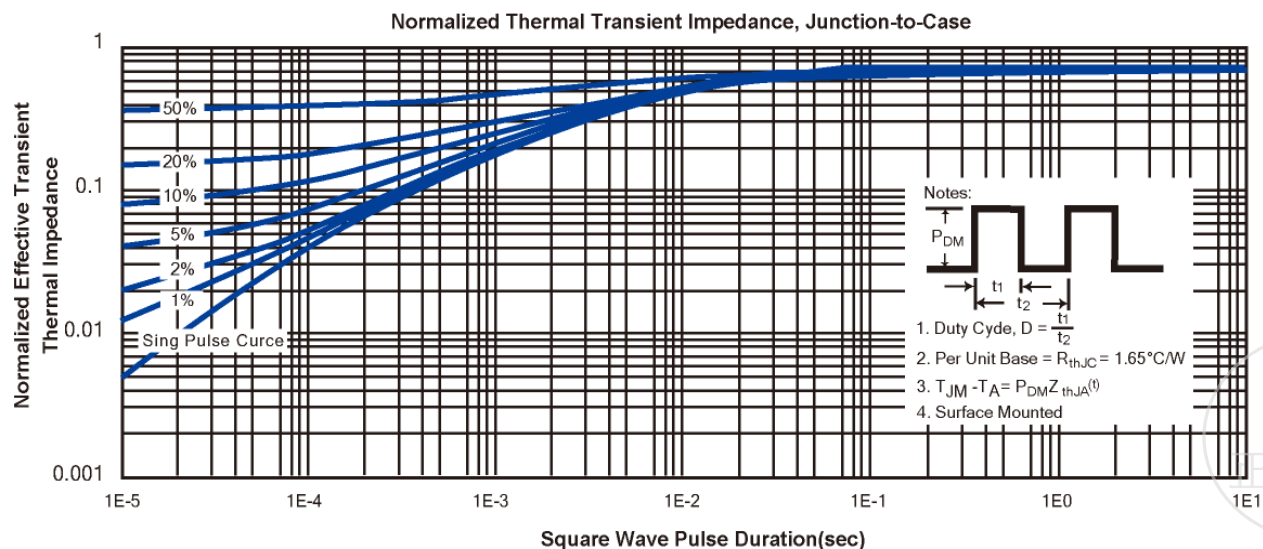
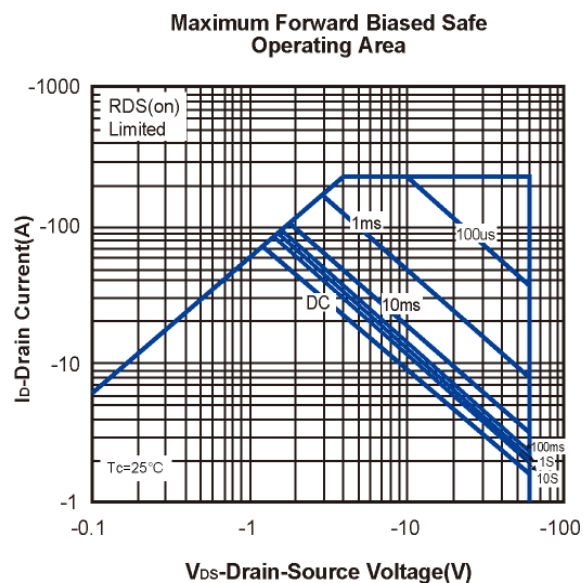
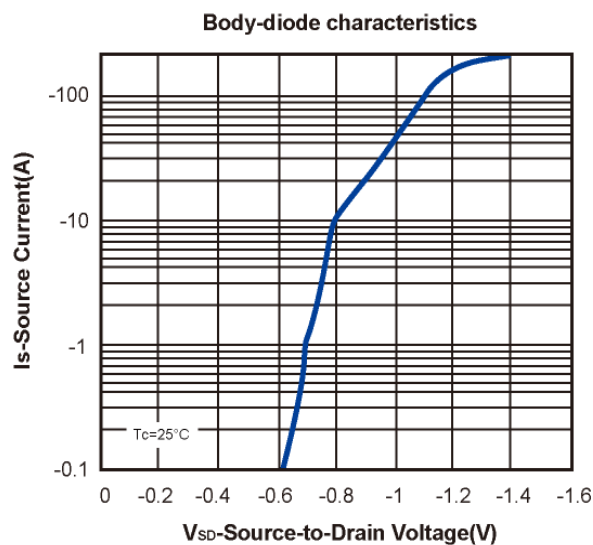
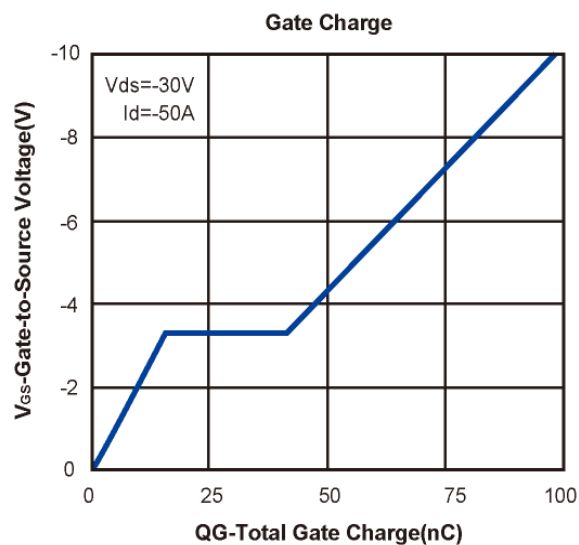


On-Region Characteristics

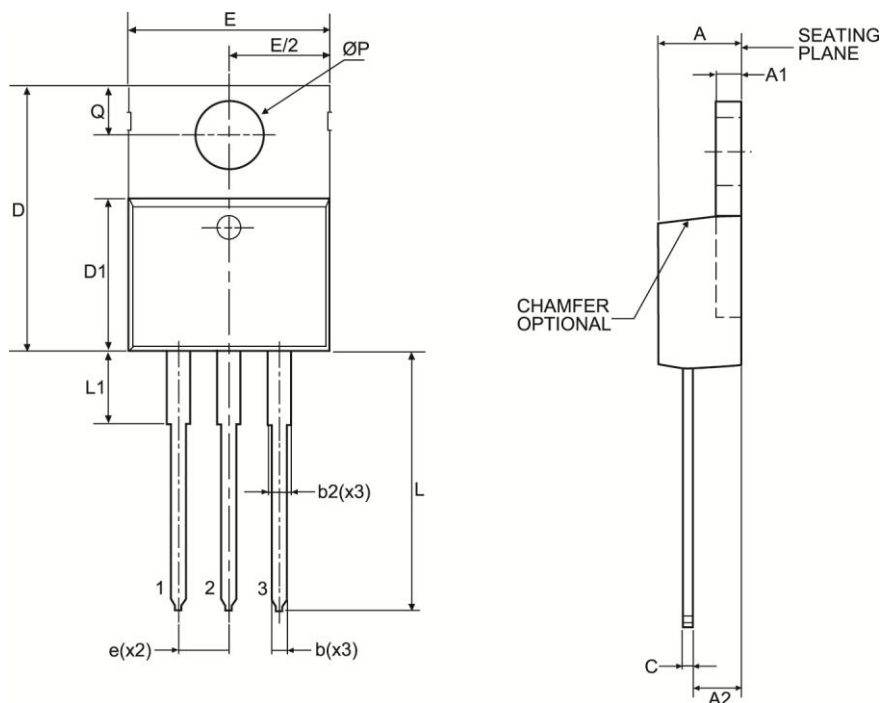


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TO-220 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	3.50	4.90
A1	1.00	1.40
A2	2.00	3.00
b	0.70	1.40
c	0.35	0.65
D	14.00	16.50
D1	8.30	9.50
E	9.60	10.70
e	2.54 BSC	
L	12.50	15.00
ØP	3.60 TYP	
Q	2.50	3.10
b2	1.10	1.80
L1	2.40	3.20

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