ME6874/ME6874-G

Dual N-Channel 20-V (G-S) MOSFET

GENERAL DESCRIPTION

The ME6874 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- 20V/6.0A,$R_{DS(ON)}$=25mΩ@V_{GS}=4.5V
- 20V/5.2A,$R_{DS(ON)}$=32mΩ@V_{GS}=2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

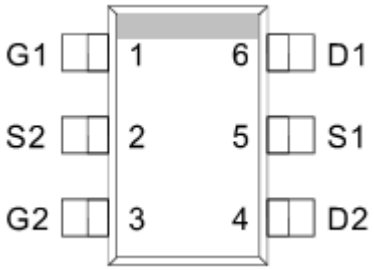
APPLICATIONS

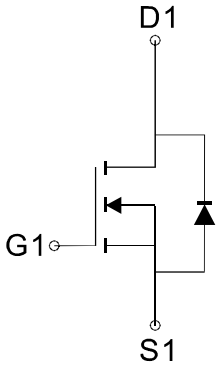
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

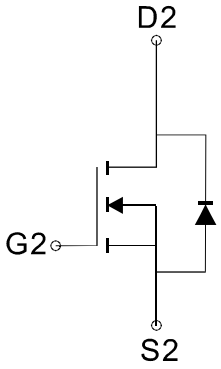
(TSOP-6)

Top View





N-Channel MOSFET



N-Channel MOSFET

Ordering Information: ME6874 (Pb-free)

ME6874-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DSS}	20		V
Gate-Source Voltage		V_{GSS}	±12		V
Continuous Drain Current		I_D	5.3		A
Pulsed Drain Current		I_{DM}	21		A
Maximum Power Dissipation	T_A=25℃	P_D	1.14		W
	T_A=70℃		0.68		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	T≦10 sec	87	℃/W
			Steady State	110	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	62		℃/W

Dual N-Channel 20-V (G-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0, I_D=250μA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.4		0.9	V
I_{GSS}	Gate Body Leakage	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=4.5V, I_D= 6.0A		20	25	mΩ
		V_{GS}=2.5V, I_D= 5.2A		25	32	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.74	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=6.0A		9.5		nC
Qgs	Gate-Source Charge			2.1		
Qgd	Gate-Drain Charge			2.6		
Rg	Gate resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		0.8		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=10V,I_D=1.0A, V_{GEN}=4.5V R_G=6Ω		9.5		ns
t_r	Turn-On Rise Time			22		
$t_{d(off)}$	Turn-Off Delay Time			47		
t_f	Turn-Off Fall Time			2.6		
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1.0MHz		550		pF
Coss	Output Capacitance			76		
Crss	Reverse Transfer Capacitance			20		

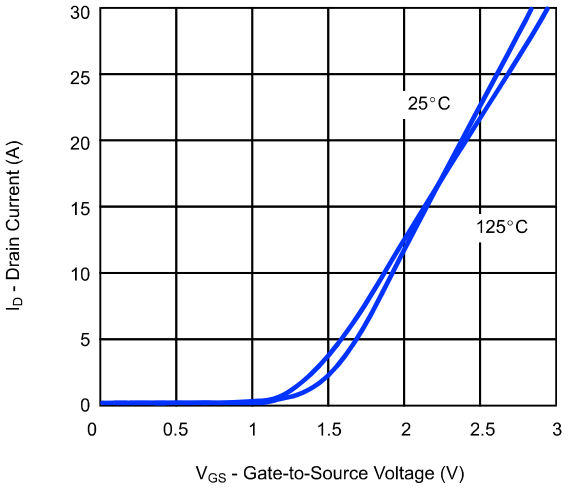
Notes: a. pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

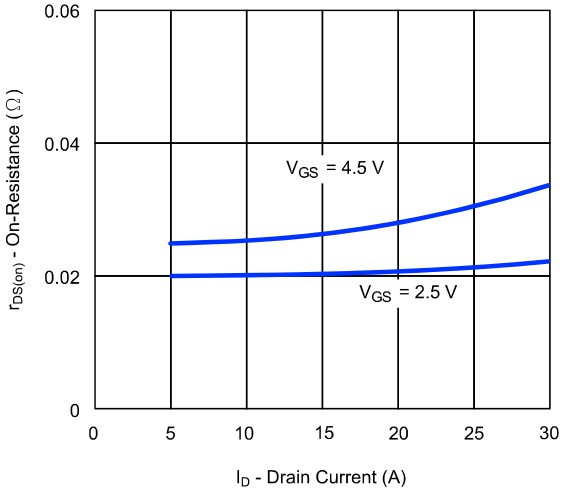
Dual N-Channel 20-V (G-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

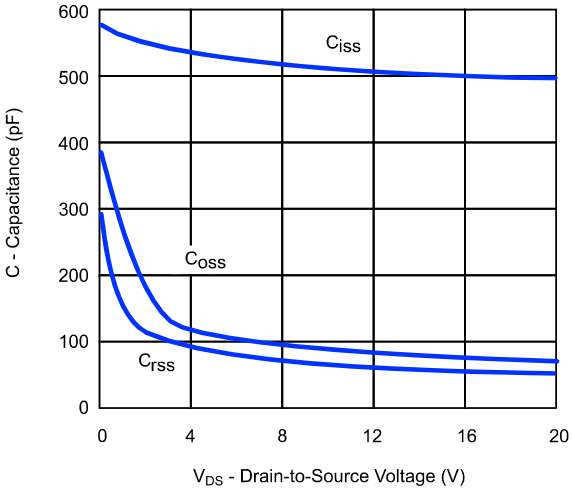
Transfer Characteristics



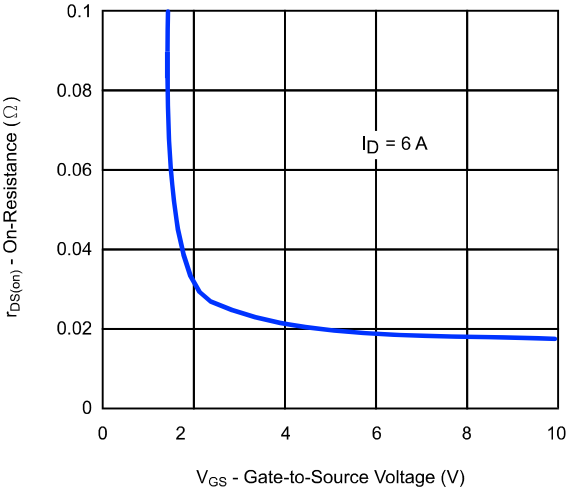
On-Resistance vs. Drain Current



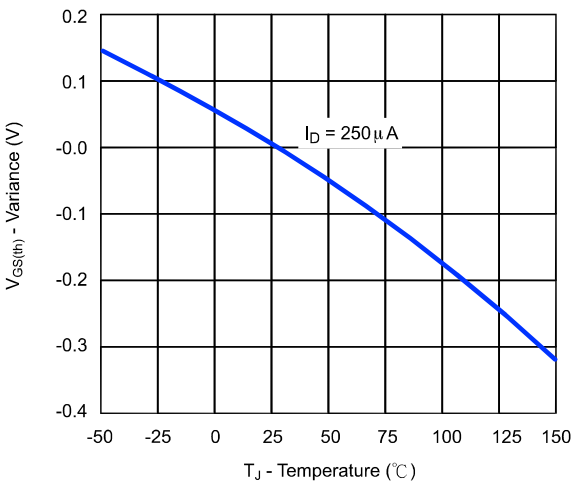
Capacitance



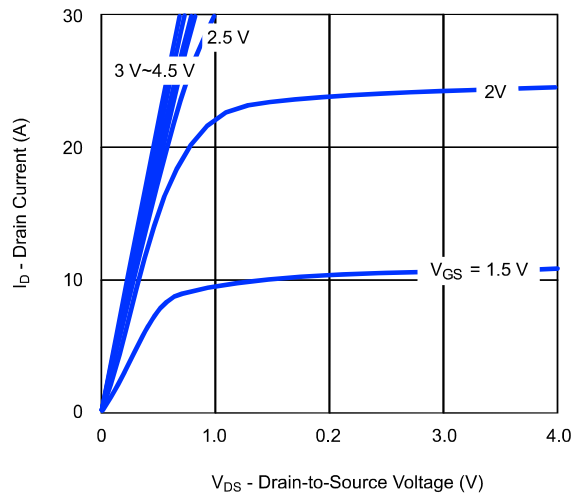
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



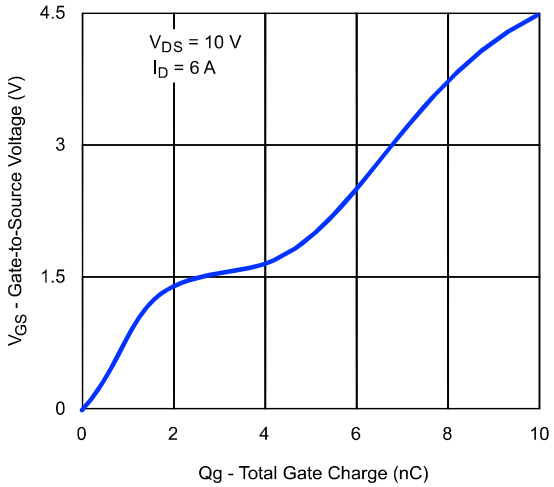
On-Region Characteristics



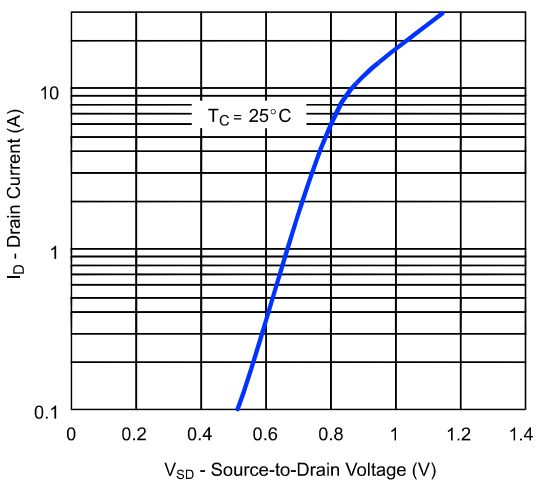
Dual N-Channel 20-V (G-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

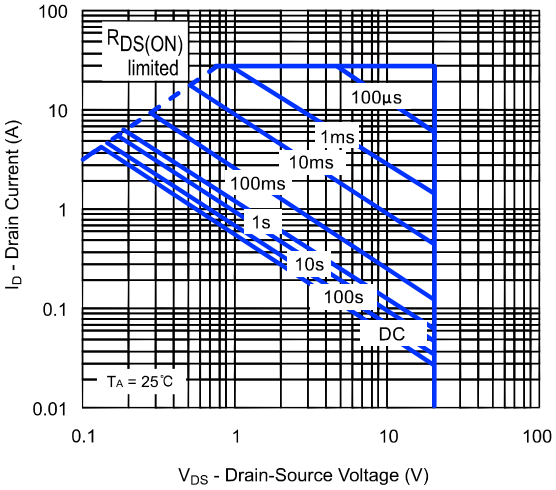
Gate Charge



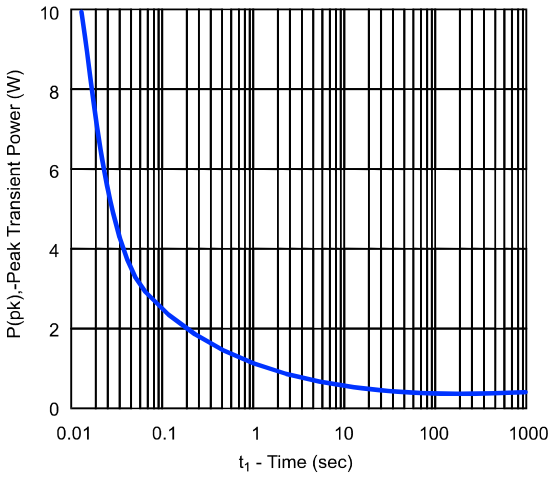
On-Resistance vs. Drain Current



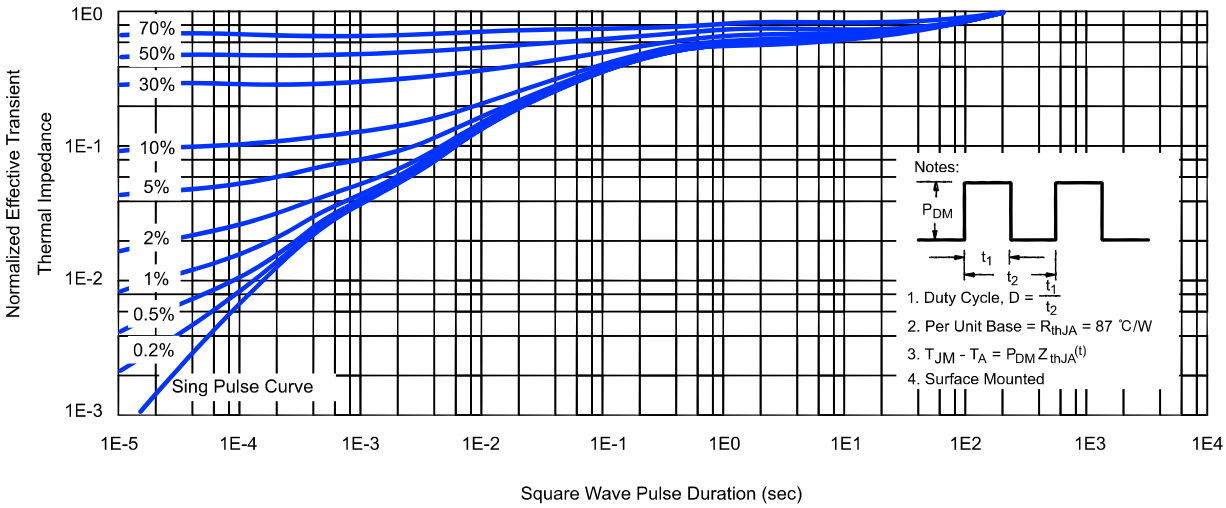
Maximum Forward Biased Safe Operating Area



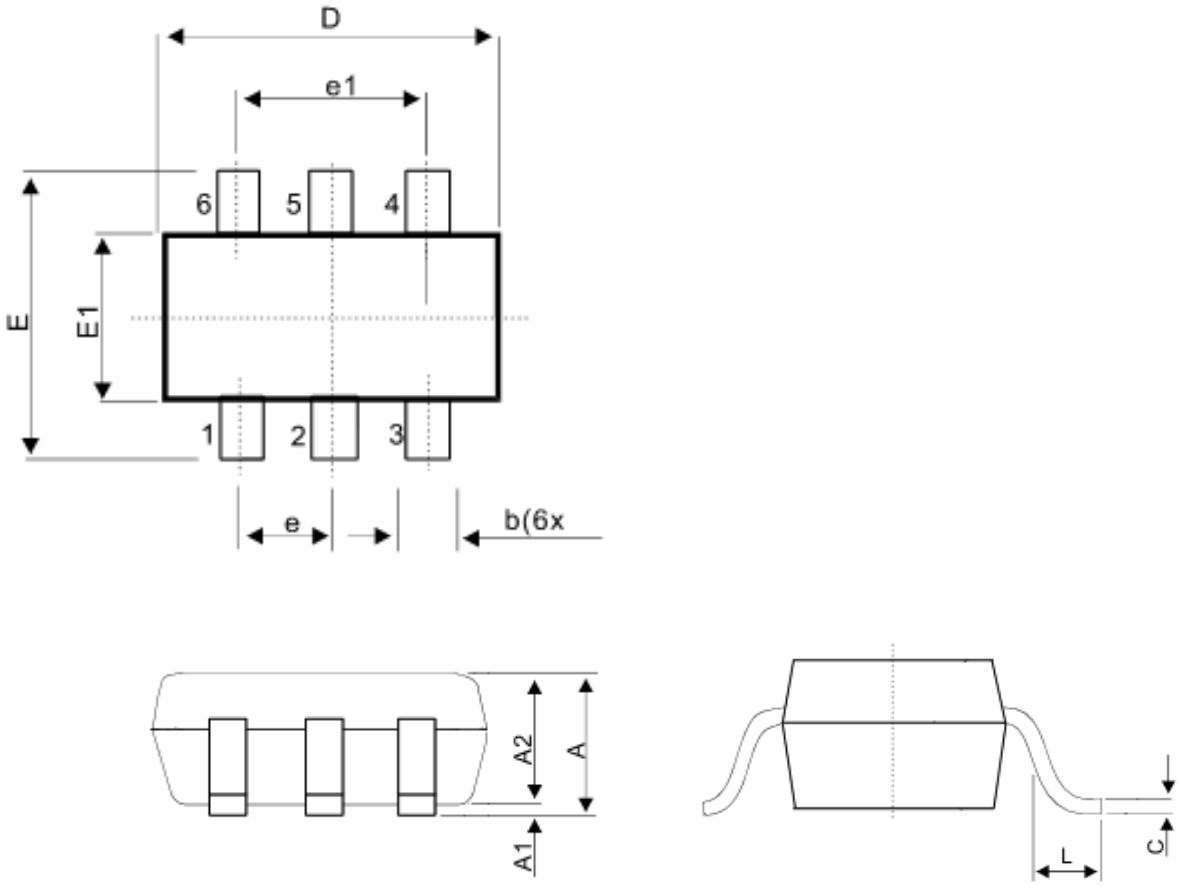
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



TSOP-6 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.20
A1	0.01	0.10
A2	0.90	1.15
b	0.25	0.50
C	0.10	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60