

Dual N-Channel 20-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME6972 Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

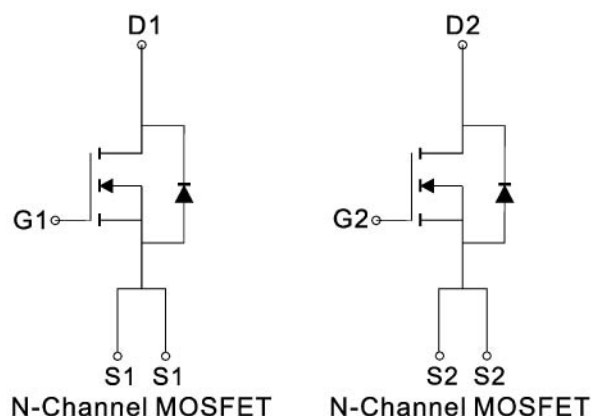
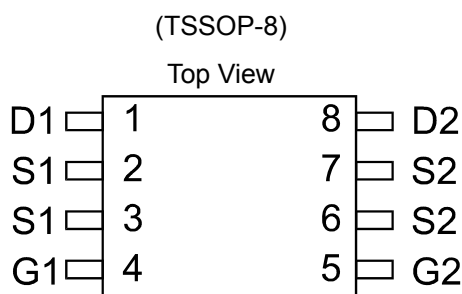
FEATURES

- $R_{DS(ON)} \leq 26m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leq 36m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION



Ordering Information: ME6972 (Pb-free)

ME6972-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current ($T_J=150^\circ\text{C}$)	$T_A=25^\circ\text{C}$	I_D	5.5	A
	$T_A=70^\circ\text{C}$		4.4	
Pulsed Drain Current		I_{DM}	22	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	1.3	W
	$T_A=70^\circ\text{C}$		0.8	
Operating Junction Temperature		T_J	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	100	$^\circ\text{C/W}$

* The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μ A	0.4		0.9	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} = $\pm$ 12V			$\pm$ 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V			1	μ A
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =4.5V, I _D = 6.0A		20	26	m Ω
		V _{GS} =2.5V, I _D = 5.2A		28	36	
V _{SD}	Diode Forward Voltage	I _S =1.7A, V _{GS} =0V		0.7	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =10V, V _{GS} =4.5V, I _D =6.0A		8		
Q _{gs}	Gate-Source Charge			2.1		
Q _{gd}	Gate-Drain Charge			2.3		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		530		pF
C _{oss}	Output Capacitance			73		
C _{rss}	Reverse Transfer Capacitance			23		
t _{d(on)}	Turn-On Delay Time	V _{DD} =10V, R _L =10 Ω I _D =1A, V _{GEN} =4.5V R _G =6 Ω		14		ns
t _r	Turn-On Rise Time			17		
t _{d(off)}	Turn-Off Delay Time			43		
t _f	Turn-Off Fall Time			5		

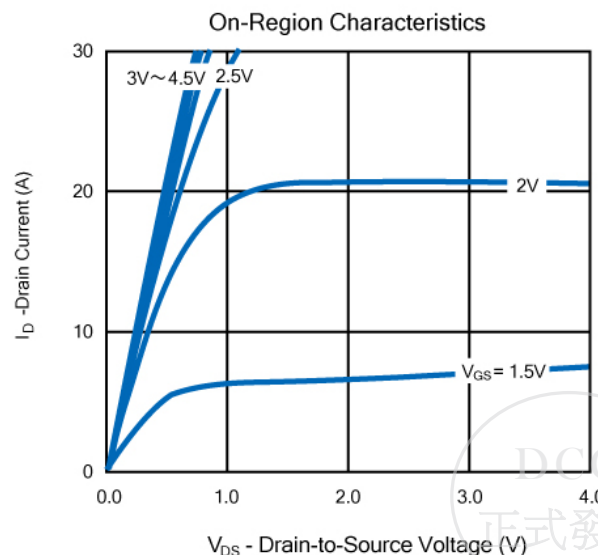
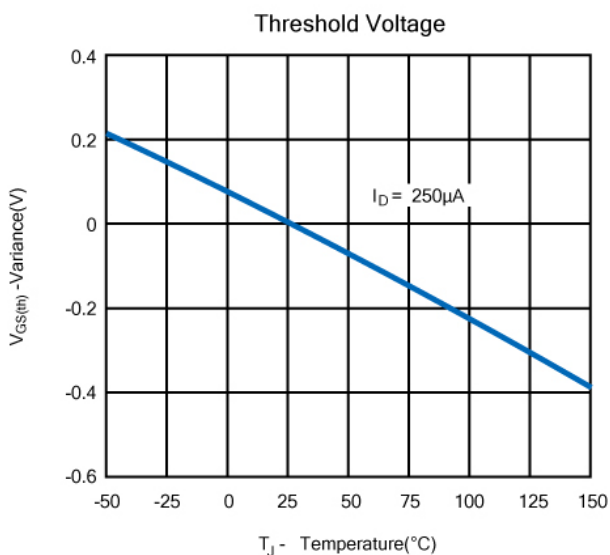
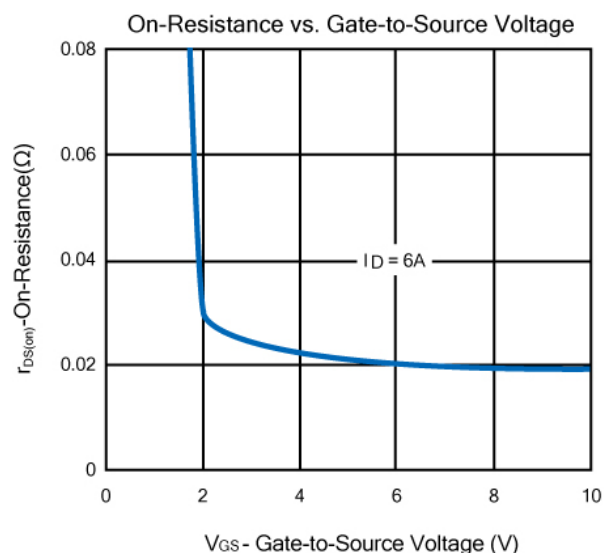
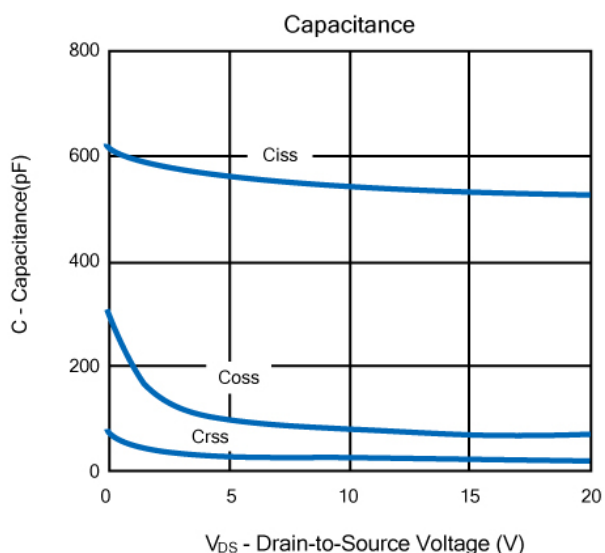
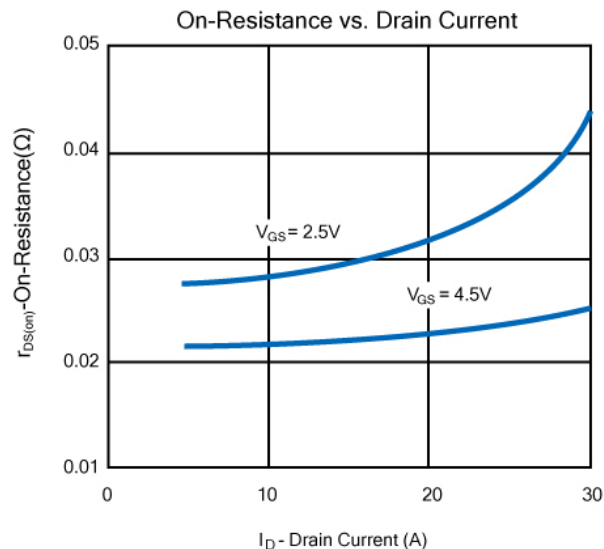
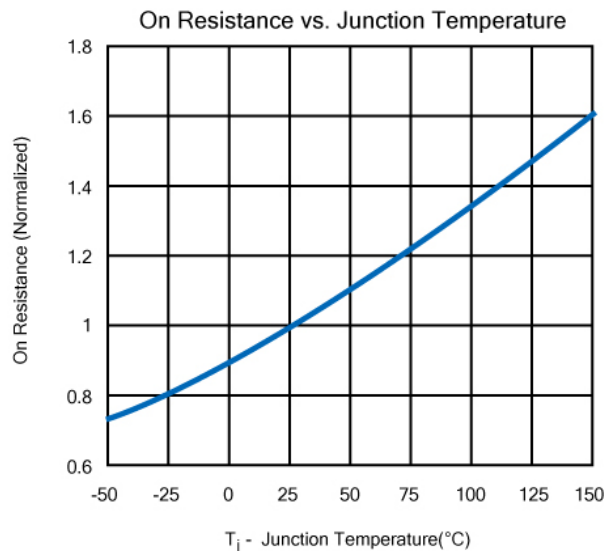
Notes: a. pulse test: pulse width $\leq$ 300 μ s, duty cycle $\leq$ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.



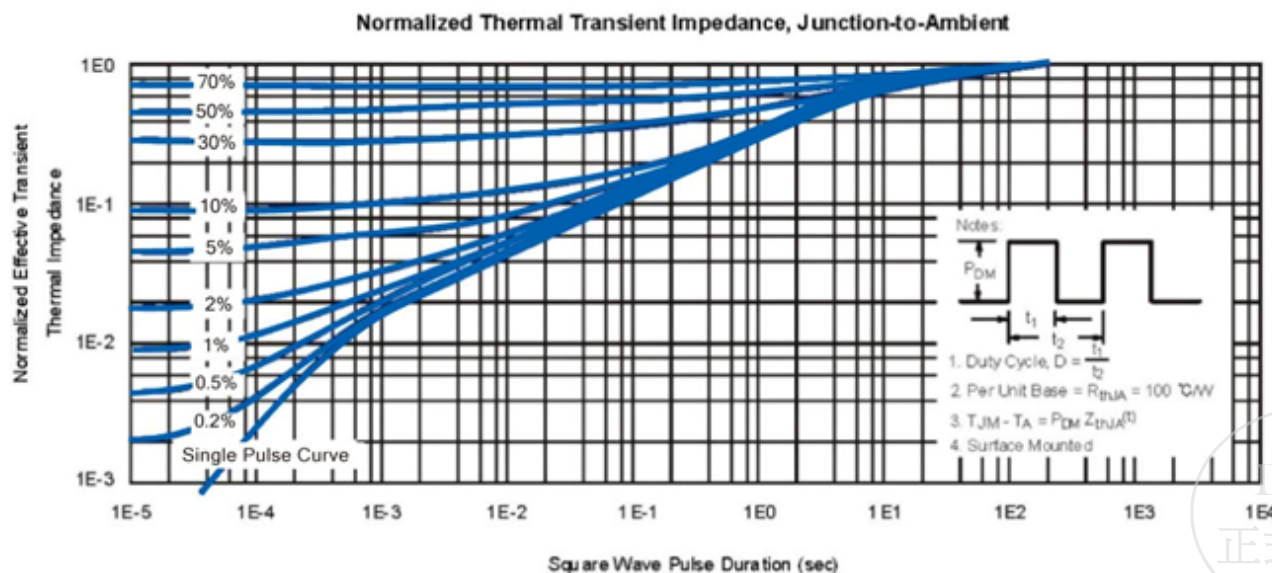
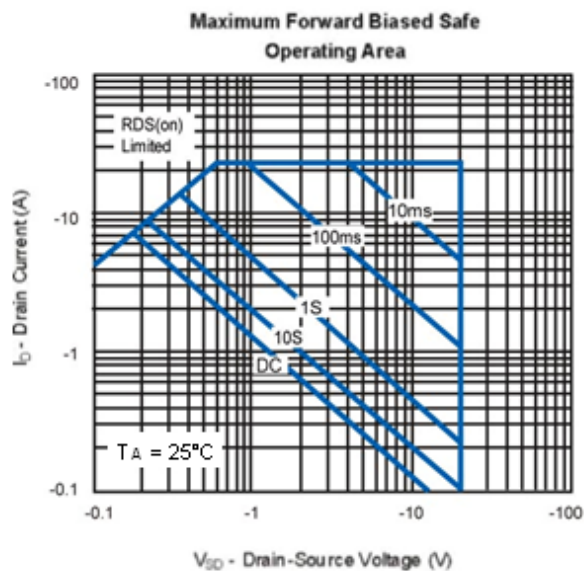
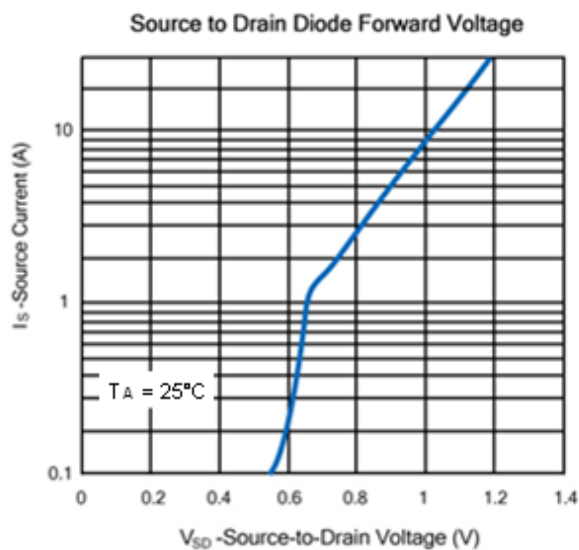
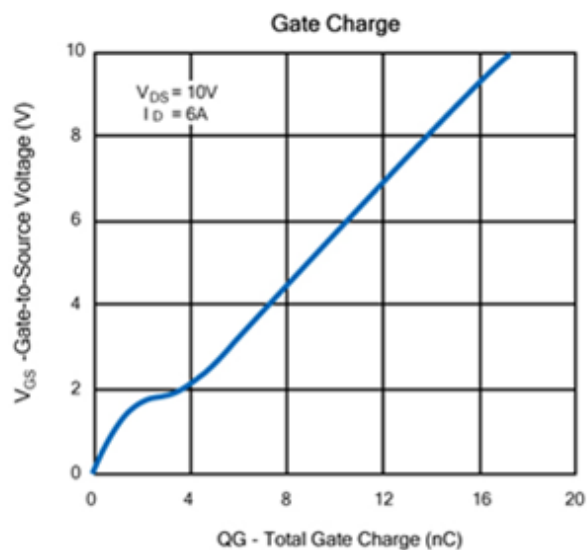
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Typical Characteristics (T_J = 25°C Noted)

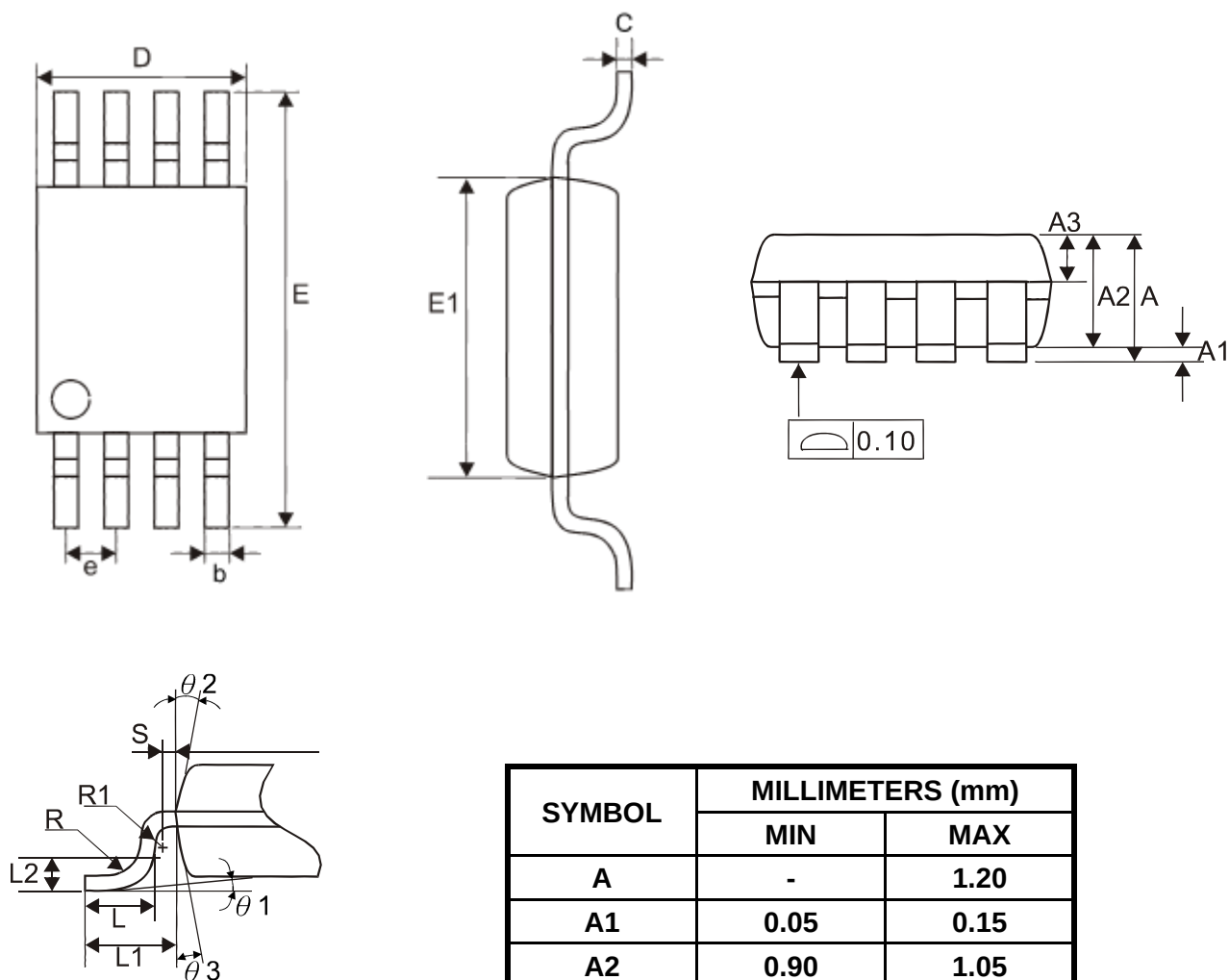


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TSSOP-8 Package



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	-	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.34	0.54
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L1	1.00REF	
L2	0.25BSC	
R	0.09	-

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