ME6982ED/ME6982ED-G

Dual N-Channel 20V(D-S) Enhancement Mode Mosfet

GENERAL DESCRIPTION

The ME6982ED Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 19m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 24m\Omega @ V_{GS}=2.5V$
- $R_{DS(ON)} \leqq 39m\Omega @ V_{GS}=1.8V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

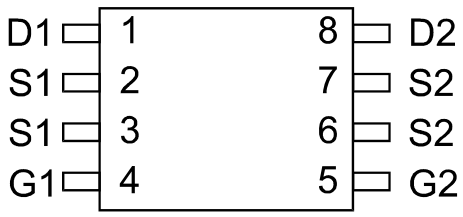
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

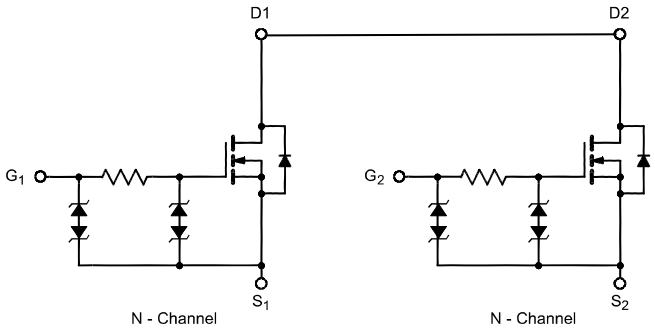
(TSSOP-8)

Top View



Ordering Information: ME6982ED (Pb-free)

ME6982ED-G (Green product-Halogen free)



*Typical value by design

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A=25℃	I_D	6.6	A
	T_A=70℃		5.3	
Pulsed Drain Current		I_{DM}	26	A
Maximum Power Dissipation	T_A=25℃	P_D	1.3	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	100	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.4		1.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V			±10	uA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=4.5V, I_D= 7A		15	19	mΩ
		V_{GS}=2.5V, I_D= 5.5A		18	24	
		V_{GS}=1.8V, I_D= 5A		29	39	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.76	1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=7A		12.6		nc
Qgs	Gate-Source Charge			3.2		
Qgd	Gate-Drain Charge			3.2		
Ciss	Input Capacitance	V_{DS}=10V, V_{GS}=0V,f=1MHz		1050		pF
Coss	Output Capacitance			143		
Crss	Reverse Transfer Capacitance			45.3		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=10V, R_L =1.5Ω V_{GEN}=5V,R_G=3.5Ω		48.2		ns
t_r	Turn-On Rise Time			338		
$t_{d(off)}$	Turn-Off Delay Time			203		
t_f	Turn-Off Fall Time			239		

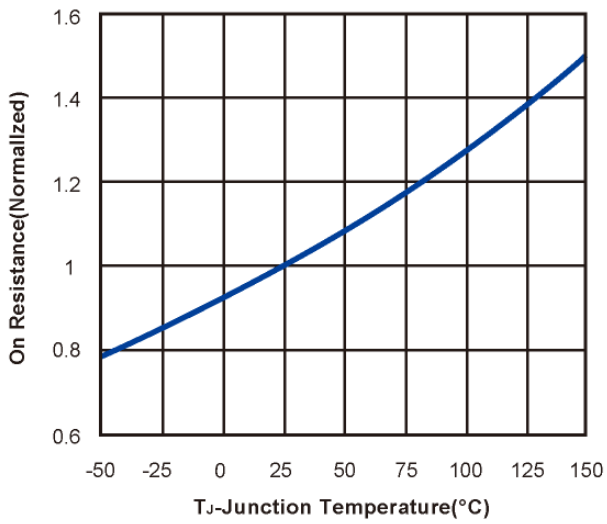
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

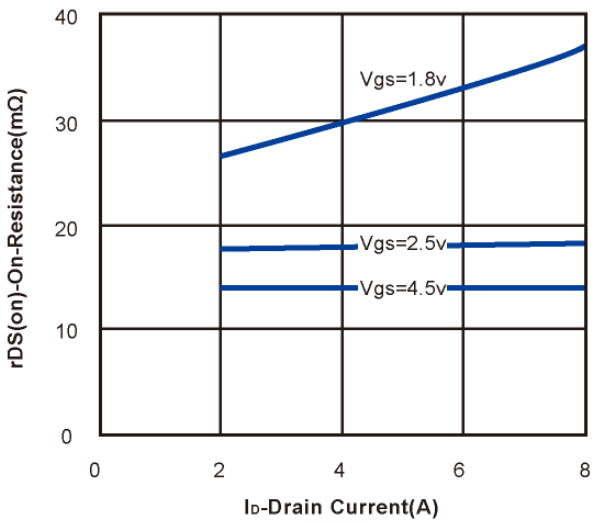
Dual N-Channel 20V(D-S) Enhancement Mode Mosfet

Typical Characteristics (T_J =25℃ Noted)

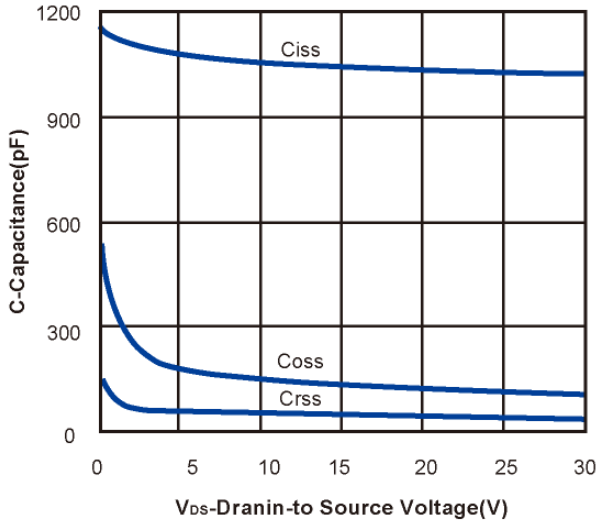
On Resistance vs. Junction Temperature



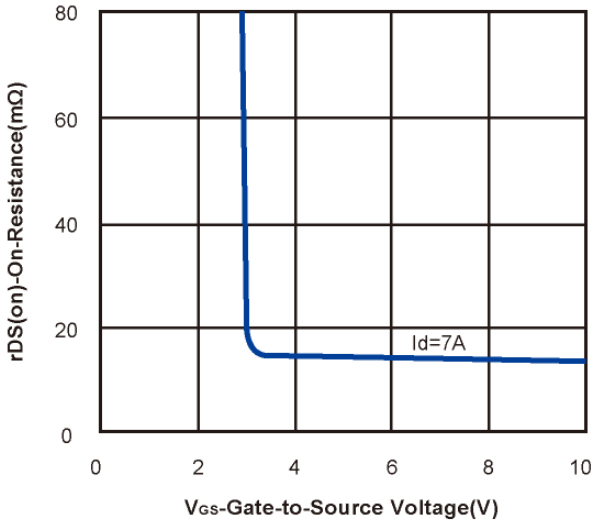
On Resistance vs. Drain Current



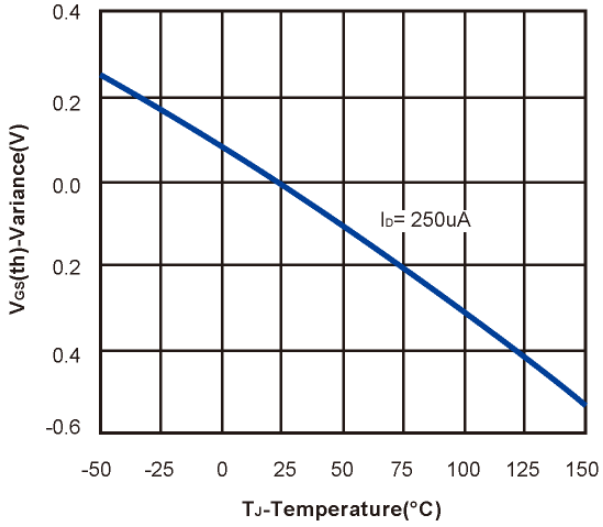
Capacitance



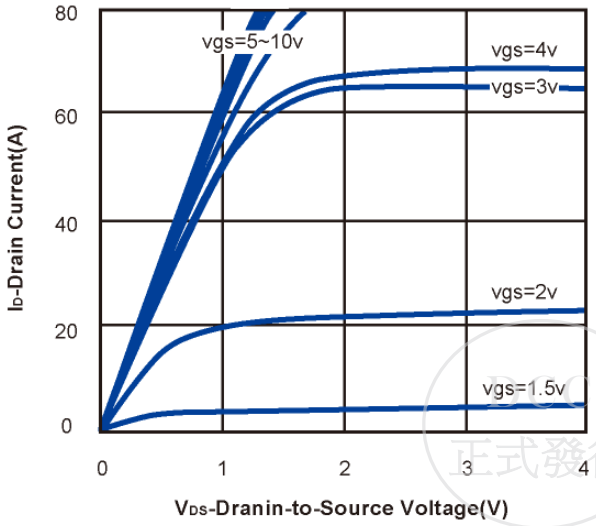
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



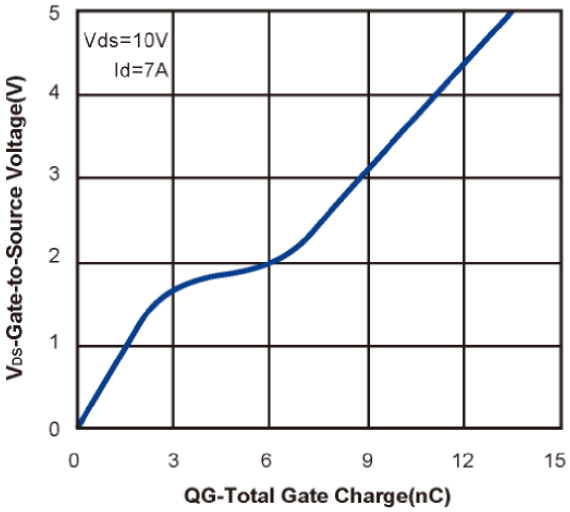
On-Region Characteristics



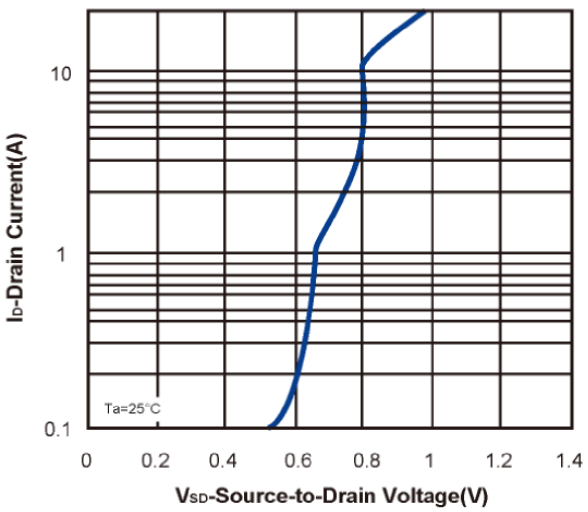
Dual N-Channel 20V(D-S) Enhancement Mode Mosfet

Typical Characteristics (T_J =25℃ Noted)

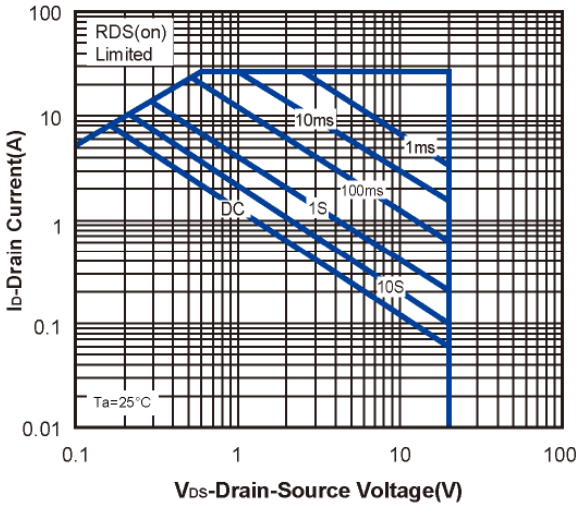
Gate Charge



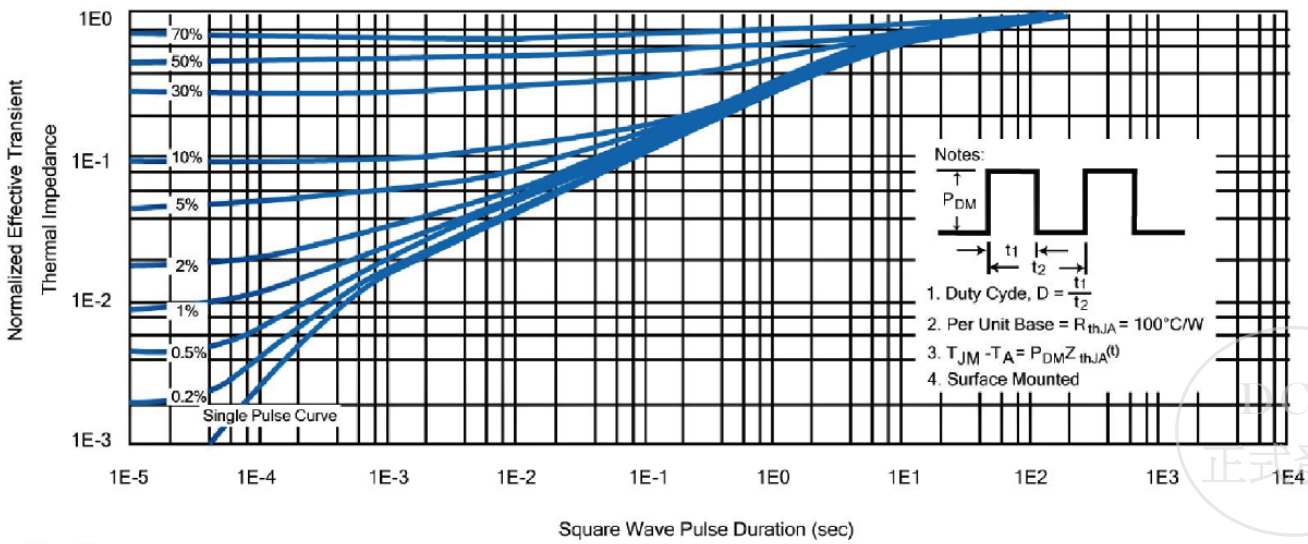
Body-diode characteristics



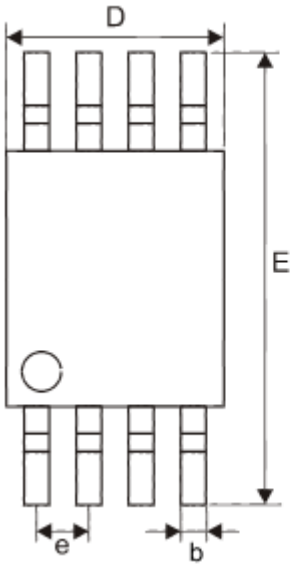
Maximum Forward Biased Safe Operating Area

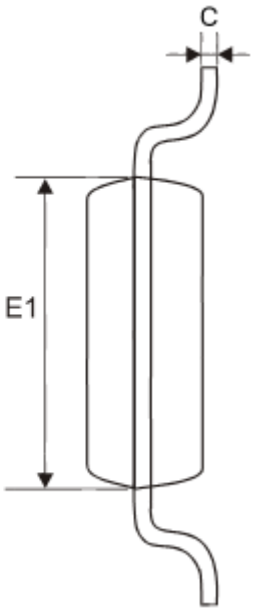


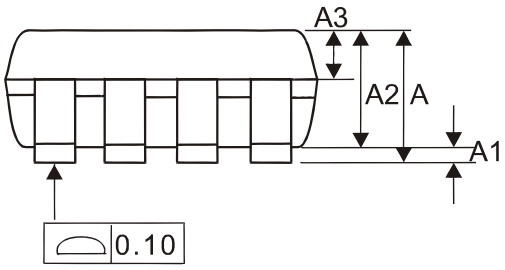
Normalized Thermal Transient Impedance, Junction-to-Ambient

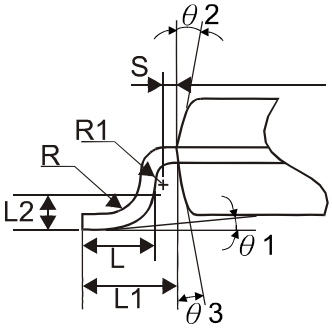


TSSOP-8 Package









SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	-	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.34	0.54
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.20	6.60
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L1	1.00REF	
L2	0.25BSC	
R	0.09	-

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.