# Dual P-Channel 20V (D-S) MOSFET

## GENERAL DESCRIPTION

The ME6987-G is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

## FEATURES

- $R_{DS(ON)} \leqq 31m\Omega @ V_{GS}$=-4.5V
- $R_{DS(ON)} \leqq 43m\Omega @ V_{GS}$=-2.5V
- $R_{DS(ON)} \leqq 63m\Omega @ V_{GS}$=-1.8V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

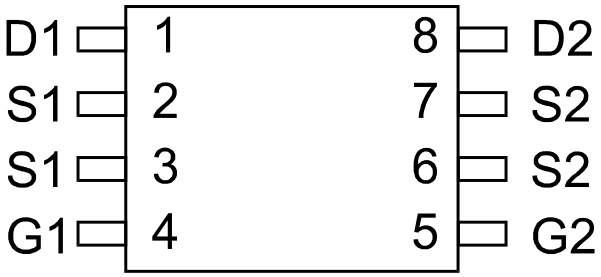
## APPLICATIONS

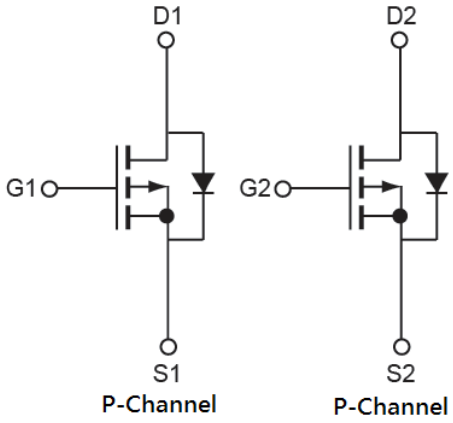
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

## PIN CONFIGURATION

(TSSOP-8)

Top View




**Ordering Information**: ME6987 -G (Green product-Halogen free)

## Absolute Maximum Ratings ($T_A$=25℃ Unless Otherwise Noted)

| Parameter | | Symbol | Maximum Ratings | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±12 | V |
| Continuous Drain Current | $T_A$=25℃ | $I_D$ | -5 | A |
| | $T_A$=70℃ | | -4 | |
| Pulsed Drain Current | | $I_{DM}$ | -20 | A |
| Maximum Power Dissipation | $T_A$=25℃ | $P_D$ | 1.3 | W |
| | $T_A$=70℃ | | 0.8 | |
| Junction and Storage Temperature Range | | TJ, Tstg | -55 to 150 | ℃ |
| Thermal Resistance-Junction to Ambient* | | $R_{\theta JA}$ | 100 | ℃/W |

*The device mounted on 1in$^2$ FR4 board with 2 oz copper

## Dual P-Channel 20V (D-S) MOSFET

**Electrical Characteristics** ($T_J$=25℃ Unless Otherwise Specified)

| Symbol | Parameter | Limit | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **STATIC** | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_D$=-250μA | -20 | | | V |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=-250μA | -0.3 | | -1 | V |
| $I_{GSS}$ | Gate Leakage Current | $V_{DS}$=0V, $V_{GS}$=±12V | | | ±100 | nA |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=-20V, $V_{GS}$=0V | | | -1 | μA |
| $R_{DS(ON)}$ | Drain-Source On-Resistance | $V_{GS}$=-4.5V, $I_D$= -4.5A | | 24 | 31 | mΩ |
| | | $V_{GS}$=-2.5V, $I_D$= -3A | | 31 | 43 | |
| | | $V_{GS}$=-1.8V, $I_D$= -2A | | 45 | 63 | |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=-0.5A, $V_{GS}$=0V | | -0.62 | -1 | V |
| **DYNAMIC** | | | | | | |
| Qg | Total Gate Charge | $V_{DS}$=-10V, $V_{GS}$=-4.5V, $I_D$=-4.5A | | 14.8 | | nC |
| Qgs | Gate-Source Charge | | | 2.3 | | |
| Qgd | Gate-Drain Charge | | | 4.3 | | |
| Ciss | Input Capacitance | $V_{DS}$=-10V, $V_{GS}$=0V,f=1MHz | | 1107 | | pF |
| Coss | Output Capacitance | | | 139 | | |
| Crss | Reverse Transfer Capacitance | | | 136 | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DS}$=-10V, $R_L$=10Ω<br>$R_G$=6Ω,$V_{GS}$=-4.5V<br>$I_D$=-1A | | 61.5 | | ns |
| $t_r$ | Turn-On Rise Time | | | 37 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 113 | | |
| $t_f$ | Turn-Off Fall Time | | | 41 | | |

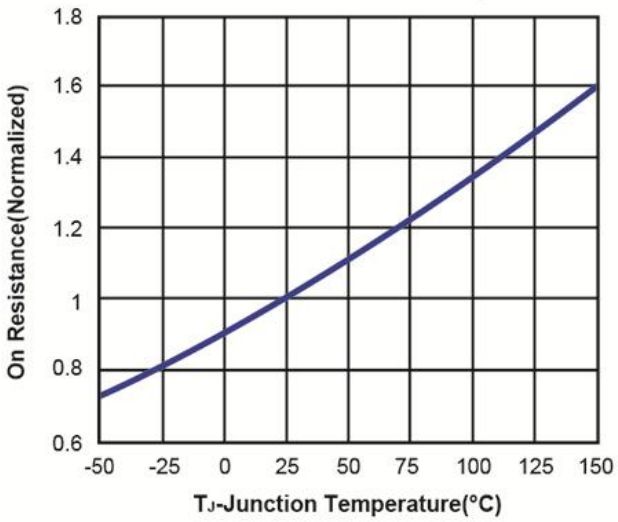
Notes: a. Pulse test; pulse width ≦ 300us, duty cycle ≦ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

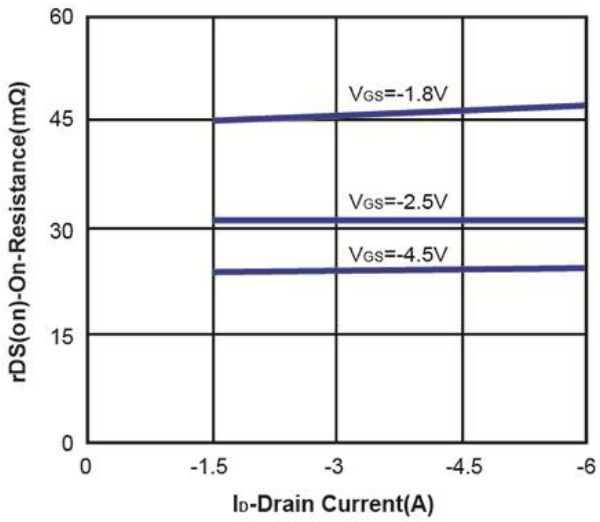
## Dual P-Channel 20V (D-S) MOSFET

### Typical Characteristics ($T_J$ =25℃ Noted)

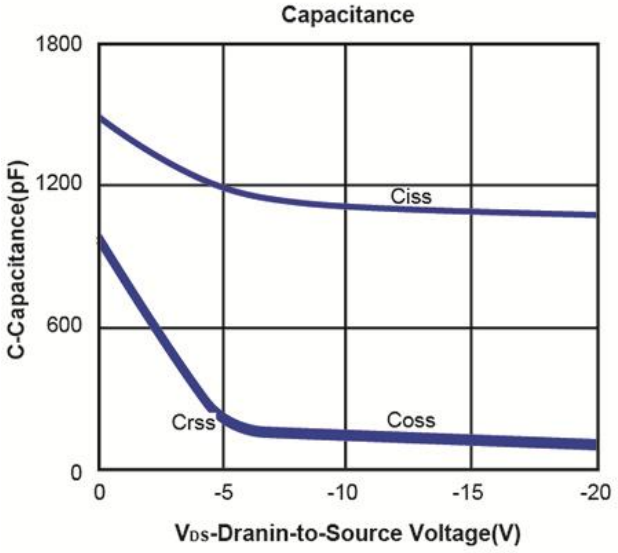
On Resistance vs. Junction Temperature



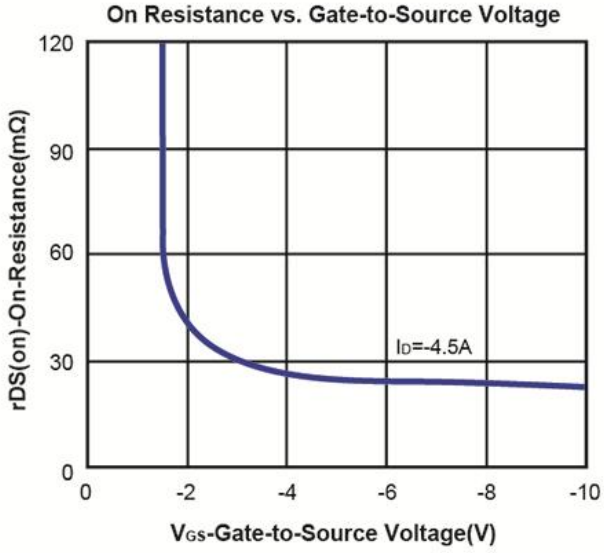

On Resistance vs. Drain Current



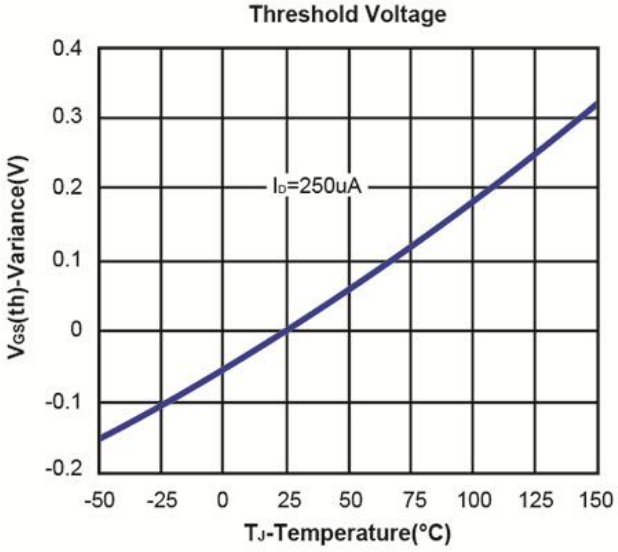

Capacitance



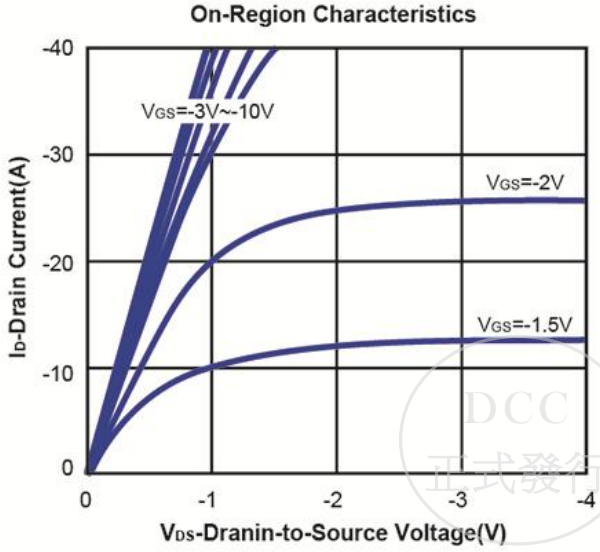

On Resistance vs. Gate-to-Source Voltage




Threshold Voltage



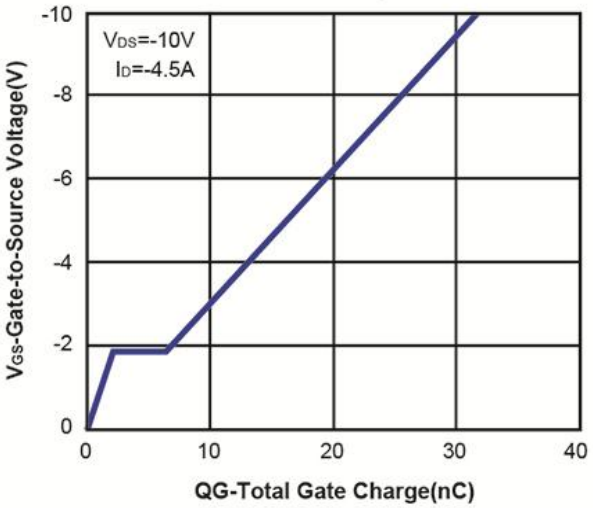

On-Region Characteristics



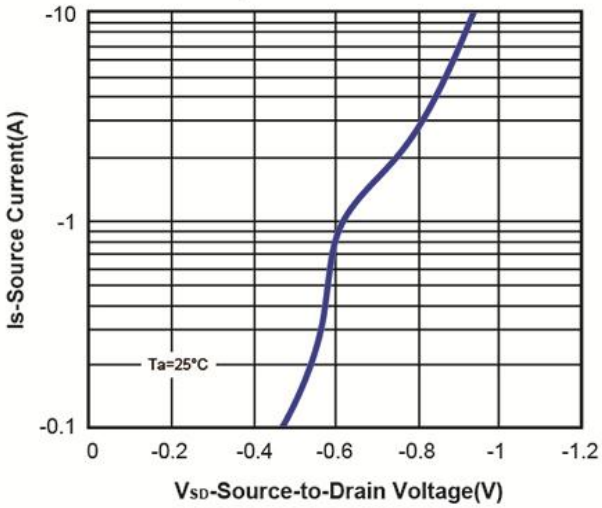
## Dual P-Channel 20V (D-S) MOSFET

### Typical Characteristics ($T_J$ =25℃ Noted)

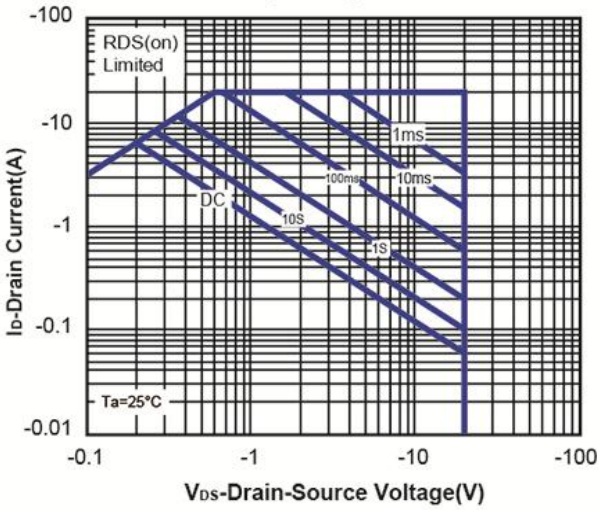
Gate Charge



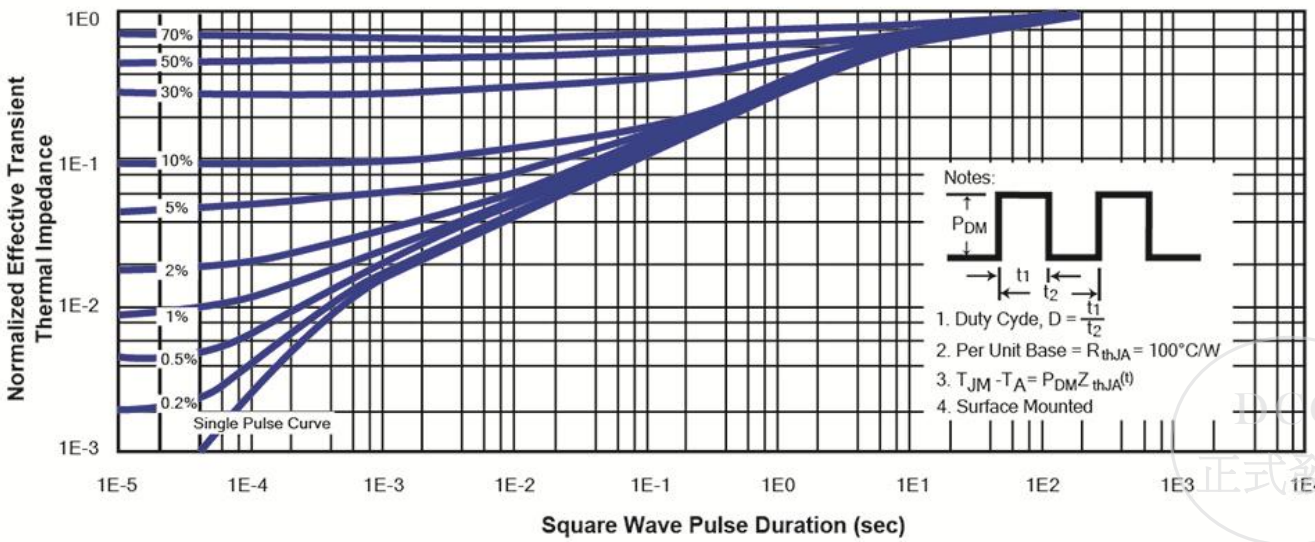

Body-diode characteristics



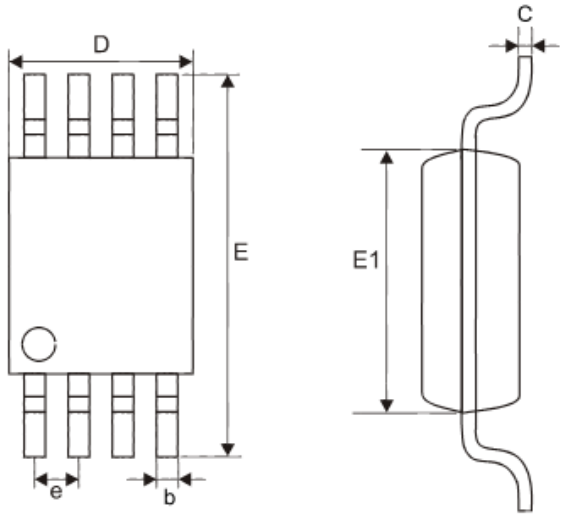

Maximum Forward Biased Safe Operating Area

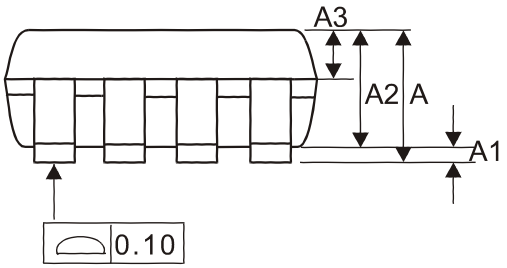


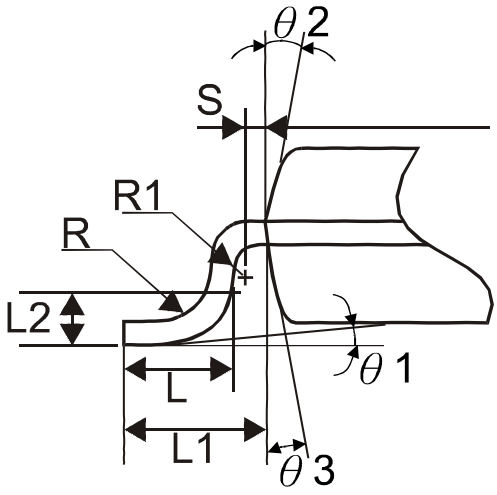

Normalized Thermal Transient Impedance, Junction-to-Ambient



# TSSOP-8 Package Outline




| SYMBOL | MILLIMETERS (mm) | |
|---|---|---|
| | MIN | MAX |
| A | - | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.90 | 1.05 |
| A3 | 0.34 | 0.54 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 2.90 | 3.10 |
| E | 6.20 | 6.60 |
| E1 | 4.30 | 4.50 |
| e | 0.65BSC | |
| L | 0.45 | 0.75 |
| L1 | 1.00REF | |
| L2 | 0.25BSC | |
| R | 0.09 | - |