ME7114-G

N-Channel 30V(D-S) Enhancement MOSFET

GENERAL DESCRIPTION

The ME7114-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 7m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 10.5m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

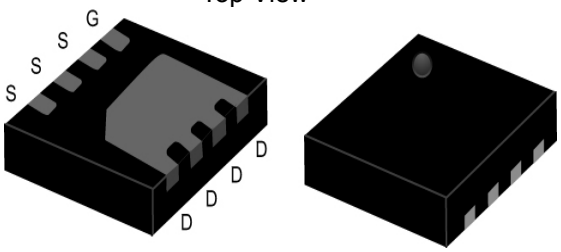
APPLICATIONS

- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

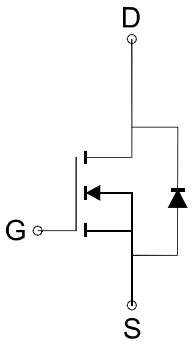
PIN CONFIGURATION

(DFN 3.3x3.3)

Top View



Bottom View



N-Channel MOSFET

Ordering Information: ME7114-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Steady State				Unit
Drain-Source Voltage		V_{DSS}	30				V
Gate-Source Voltage		V_{GSS}	±20				V
Continuous Drain Current(Tj=150℃)*	T_C=25℃	I_D	71				A
	T_C=70℃		57				
	T_A=25℃		18.4				
	T_A=70℃		14.7				
Pulsed Drain Current		I_{DM}	74				A
Maximum Power Dissipation*	T_C=25℃	P_D	52				W
	T_C=70℃		33				
	T_A=25℃		3.8				
	T_A=70℃		2.4				
Operating Junction Temperature		T_J	-55 to 150				℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	Typ	26	Max	33	℃/W
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	Typ	1.9	Max	2.4	

*The device mounted on 1in^2 FR4 board with 2 oz copper

N-Channel 30V(D-S) Enhancement MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0		3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D=13A		5.8	7	mΩ
		V_{GS}=4.5V, I_D=10A		8.5	10.5	
V_{SD}	Diode Forward Voltage	I_S=2.8A, V_{GS}=0V		0.75	1.1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=13A		37		nC
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=13A		18		
Qgs	Gate-Source Charge			7.7		
Qgd	Gate-Drain Charge			8.8		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, F=1MHz		1690		pF
Coss	Output Capacitance			260		
Crss	Reverse Transfer Capacitance			84		
Rg	Gate-Resistance	V_{DS}=0V, V_{GS}=0V, F=1MHz		0.9		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L=15Ω, I_D=1A, V_{GEN}=10V, R_G=6Ω		20		ns
t_r	Turn-On Rise Time			16		
$t_{d(off)}$	Turn-Off Delay Time			63		
t_f	Turn-Off Fall Time			11		

Note: a.Pulse test: pulse width≦300us, duty cycle≦2%

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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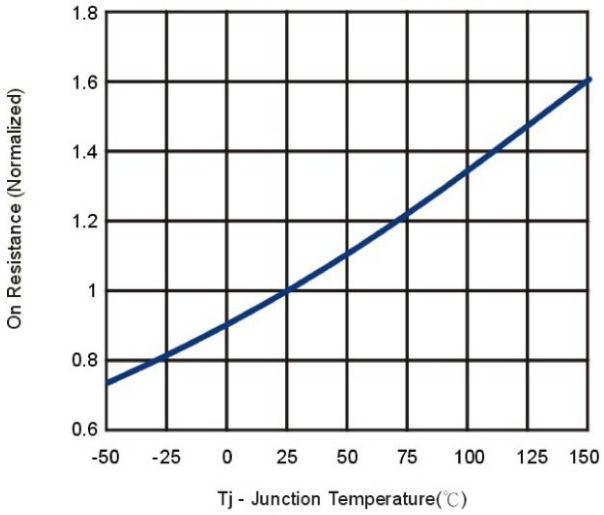
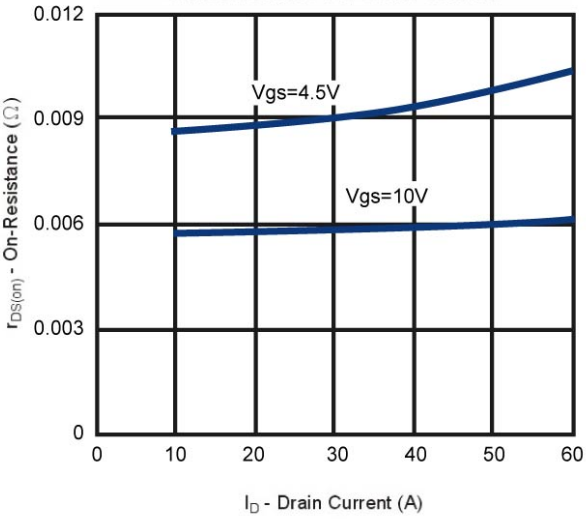
Typical Characteristics (T_J =25℃ Noted)

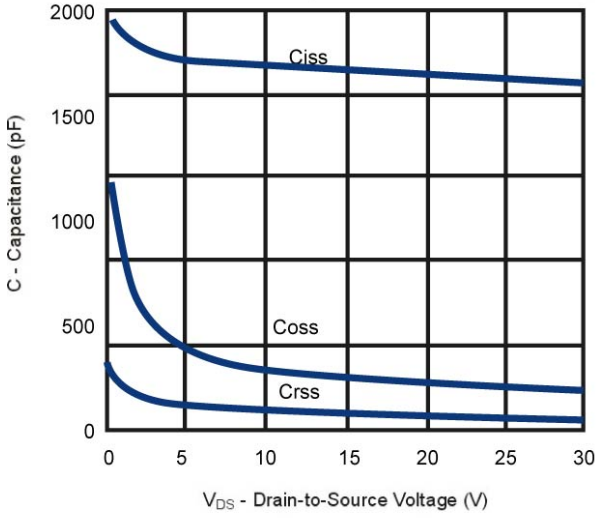
On Resistance vs. Junction Temperature



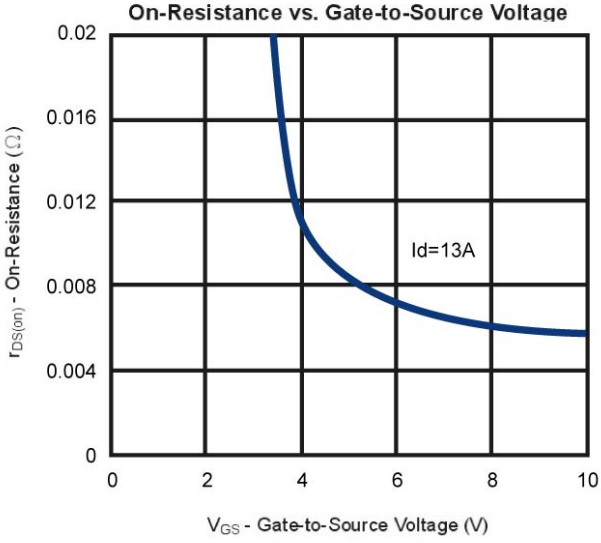
On-Resistance vs. Drain Current



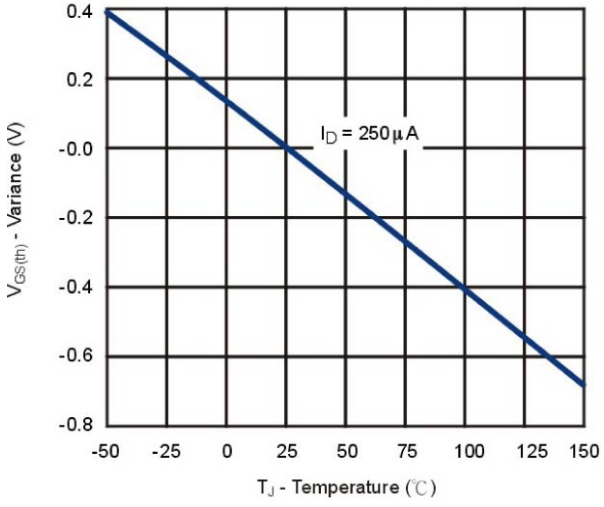
Capacitance



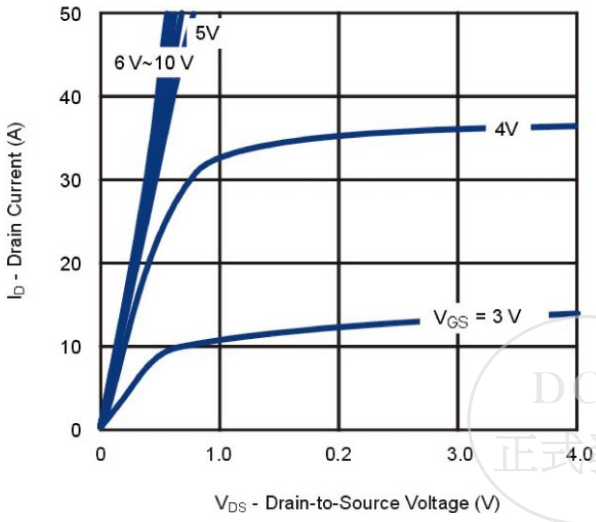
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



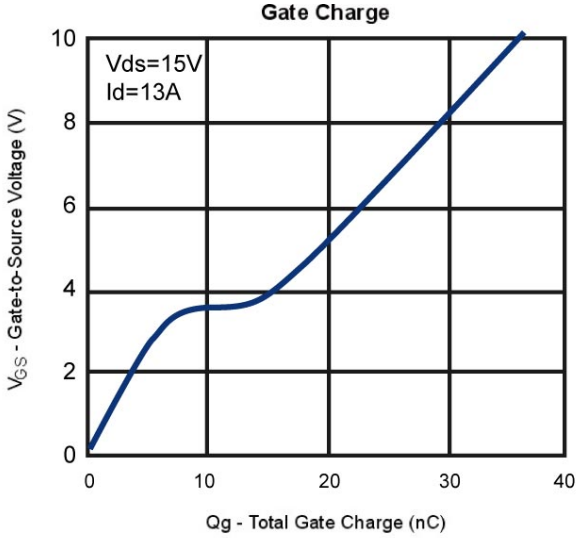
On-Region Characteristics



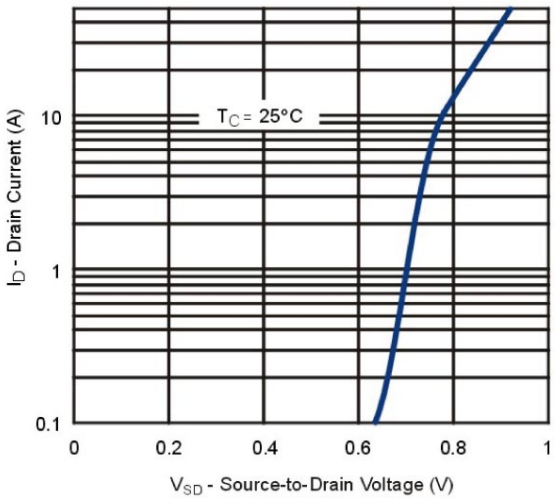
N-Channel 30V(D-S) Enhancement MOSFET

Typical Characteristics (T_J =25℃ Noted)

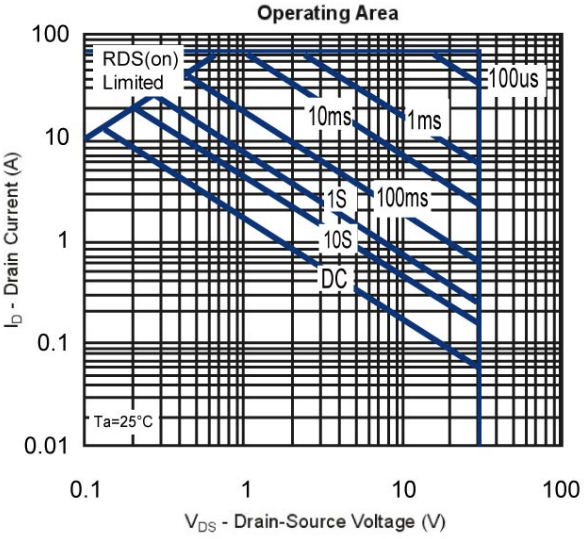
Gate Charge



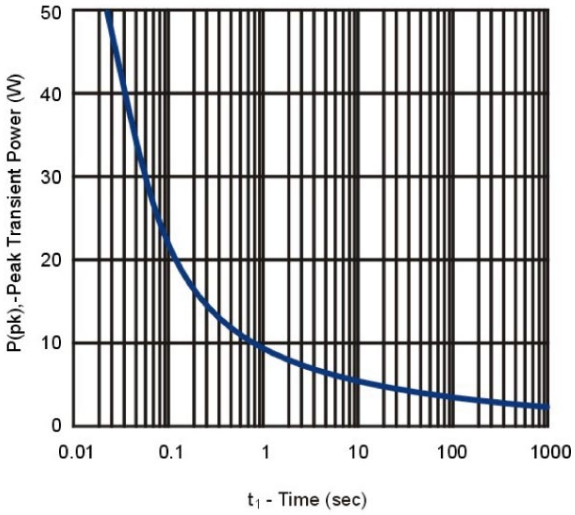
Body - Diode Characteristics



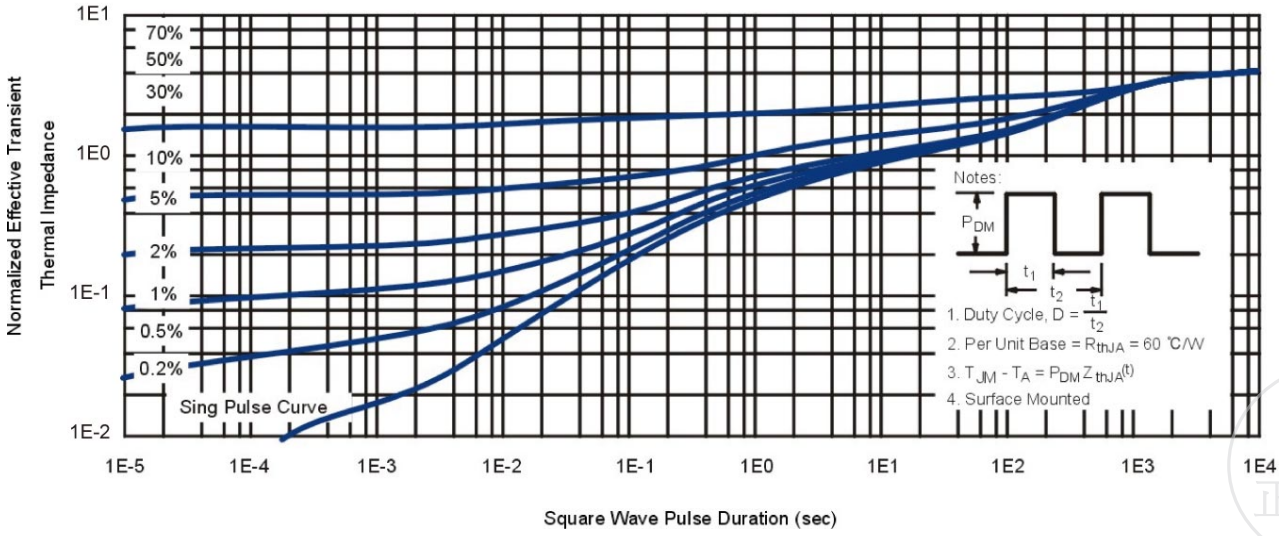
Maximum Forward Biased Safe Operating Area



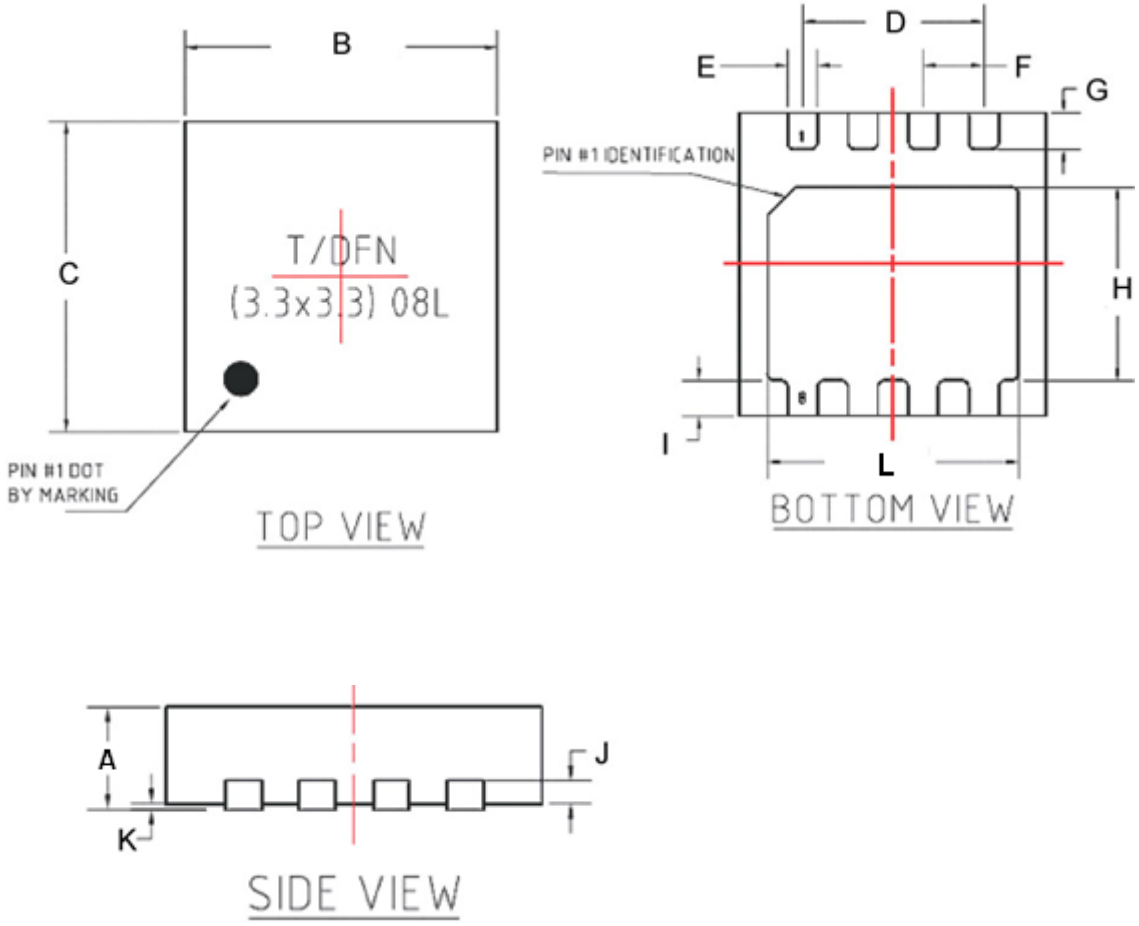
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



PowerDFN 3.3x3.3 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.700	1.000
B	3.250	3.350
C	3.250	3.350
D	1.95REF.	
E	0.270	0.370
F	0.65BSC	
G	0.350	0.450
H	2.050	2.150
I	0.340	0.440
J	0.195	0.211
K	0.000	0.050
L	2.650	2.750