Dual N- and P-Channel 12-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME7202 is the dual N-Channel + P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦ 31 mΩ@V_{GS}=4.5V (N-Ch)
- $R_{DS(ON)}$ ≦ 43 mΩ@V_{GS}=2.5V(N-Ch)
- $R_{DS(ON)}$ ≦ 74 mΩ@V_{GS}=1.8V(N-Ch)
- $R_{DS(ON)}$ ≦ 73mΩ@V_{GS}=-4.5V(P-Ch)
- $R_{DS(ON)}$ ≦ 120 mΩ@V_{GS}=-2.5V(P-Ch)
- $R_{DS(ON)}$ ≦ 240 mΩ@V_{GS}=-1.8V(P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

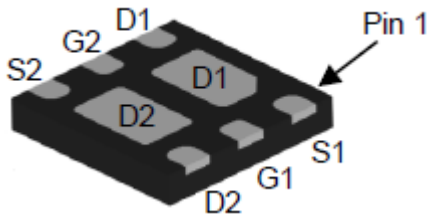
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

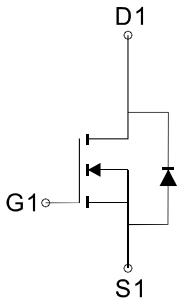
(DFN 2X2)

Bottom View

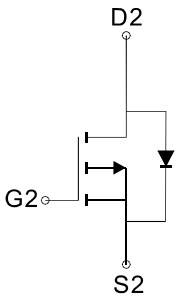


Ordering Information: ME7202 (Pb-free)

ME7202-G (Green product-Halogen free)



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	N-Channel Maximum Ratings	P-Channel Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	12	-12	V
Gate-Source Voltage		V_{GS}	±8	±8	V
Continuous Drain Current*	T_A=25℃	I_D	7.4	-4.8	A
	T_A=70℃		5.9	-3.9	
Pulsed Drain Current		I_{DM}	30	-19	A
Maximum Power Dissipation*	T_A=25℃	P_D	2.7	2.7	W
	T_A=70℃		1.7	1.7	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	45		℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_J =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit		Min	Typ	Max	Unit
STATIC							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA V_{GS}=0V, I_D=-250μA	N-Ch P-Ch	12 -12			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA V_{DS}=V_{GS}, I_D=-250μA	N-Ch P-Ch	0.4 -0.4		1 -1	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V V_{DS}=0V, V_{GS}=±8V	N-Ch P-Ch			±100 ±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=12V, V_{GS}=0V V_{DS}=-12V, V_{GS}=0V	N-Ch P-Ch			1 -1	μA
$R_{DS(ON)}$	Drain-Source on-State Resistance[a]	V_{GS}=4.5V, I_D=5A V_{GS}=-4.5V, I_D= -3.6A	N-Ch P-Ch		26 61	31 73	mΩ
		V_{GS} =2.5V, I_D =4.6A V_{GS} =-2.5V, I_D =-3.2A	N-Ch P-Ch		33 92	43 120	
		V_{GS} =1.8V, I_D =4.1A V_{GS} =-1.8V, I_D =-1A	N-Ch P-Ch		49 136	74 240	
V_{SD}	Diode Forward Voltage	I_S=5.2A, V_{GS}=0V I_S=-3.4A, V_{GS}=0V	N-Ch P-Ch		0.85 -0.8	1.2 -1.2	V
DYNAMIC							
Qg	Total Gate Charge	N-Channel V_{DS}=6V,V_{GS}=4.5V,I_D=6.5A P-Channel V_{DS}=-6V,V_{GS}=-4.5V,I_D=-4.3A	N-Ch P-Ch		6.5 6.4		nC
Qgs	Gate-Source Charge		N-Ch P-Ch		2.1 2.0		
Qgd	Gate-Drain Charge		N-Ch P-Ch		1.5 1.9		
Ciss	Input Capacitance	N-Channel V_{DS}=6V, V_{GS}=0V, f=1MHz P-Channel V_{DS} =-6V, V_{GS} =0V, f=1MHz	N-Ch P-Ch		423 405		pF
Coss	Output Capacitance		N-Ch P-Ch		86 130		
Crss	Reverse Transfer Capacitance		N-Ch P-Ch		63 104		
$t_{d(on)}$	Turn-On Delay Time	N-Channel V_{DD}=10V, R_L =10Ω I_D=1A, V_{GEN}=4.5V, R_G=6Ω P-Channel V_{DD}=-6V, R_L =6Ω I_D=-1A, V_{GEN}=-10V, R_G=6Ω	N-Ch P-Ch		8.3 44.3		ns
t_r	Turn-On Rise Time		N-Ch P-Ch		19.6 28.6		
$t_{d(off)}$	Turn-Off Delay Time		N-Ch P-Ch		32 40.7		
t_f	Turn-Off Fall Time		N-Ch P-Ch		1.89 70.4		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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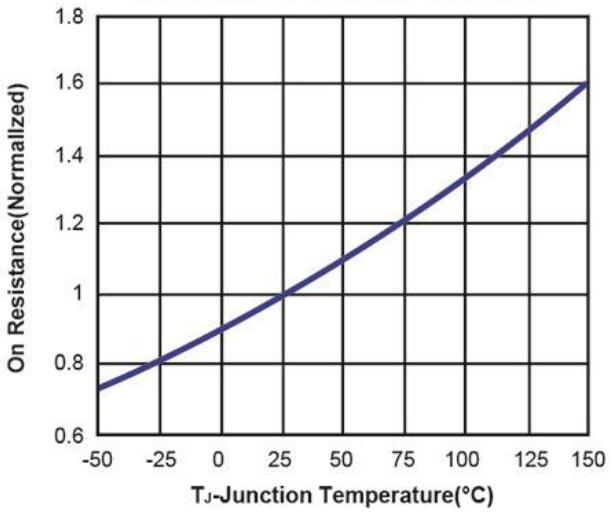
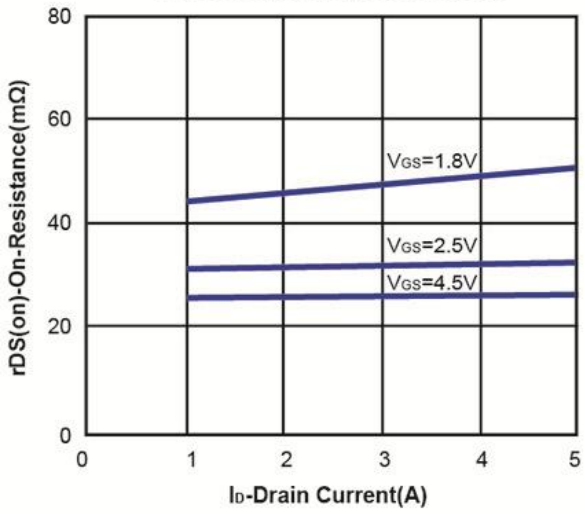
Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

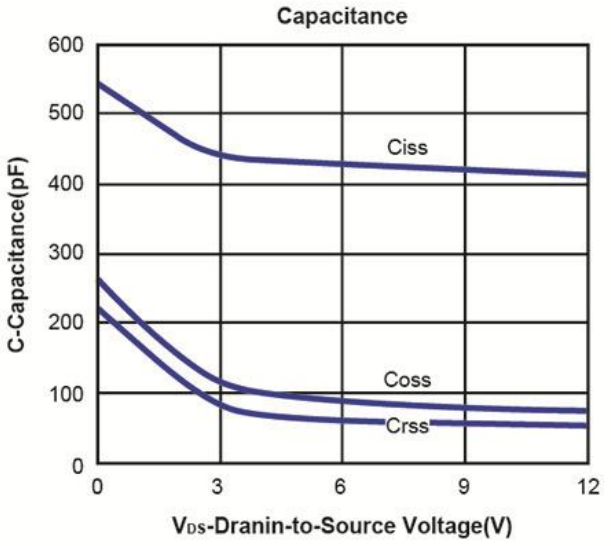
On Resistance vs. Junction Temperature



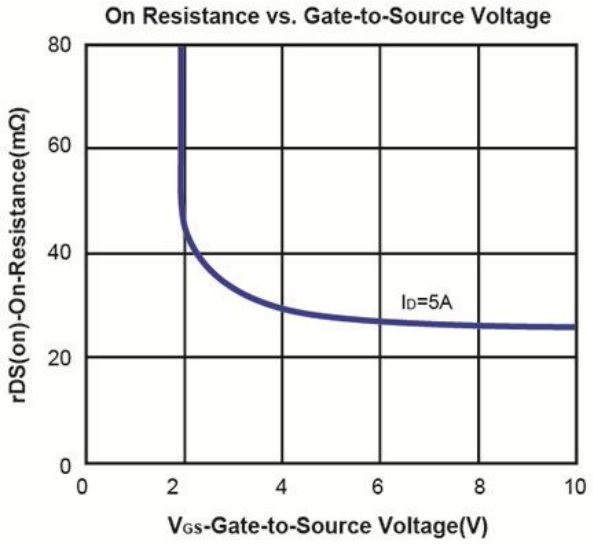
On Resistance vs. Drain Current



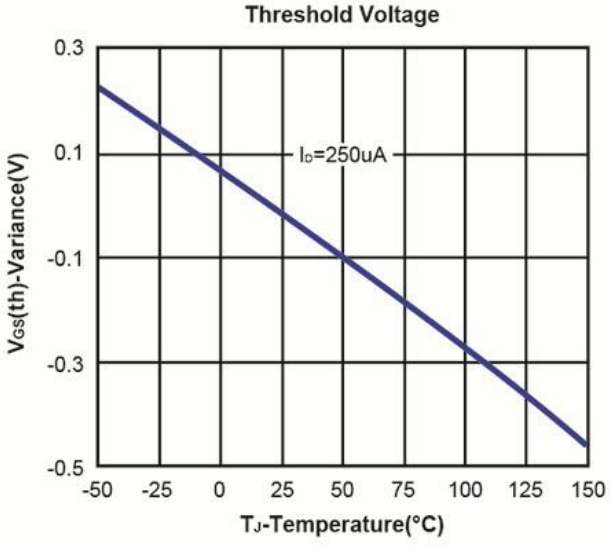
Capacitance



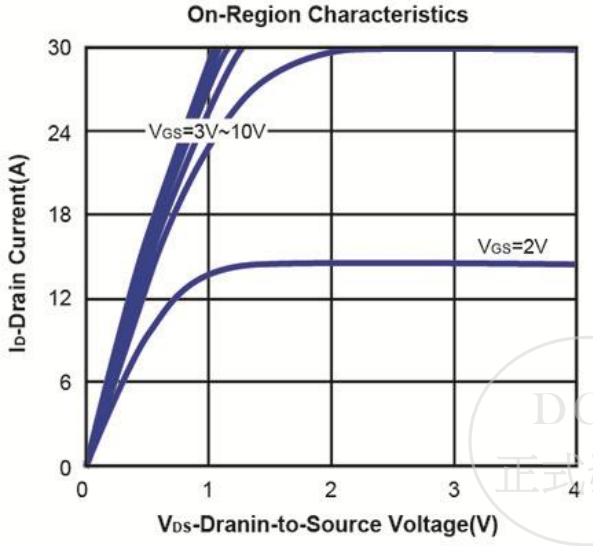
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



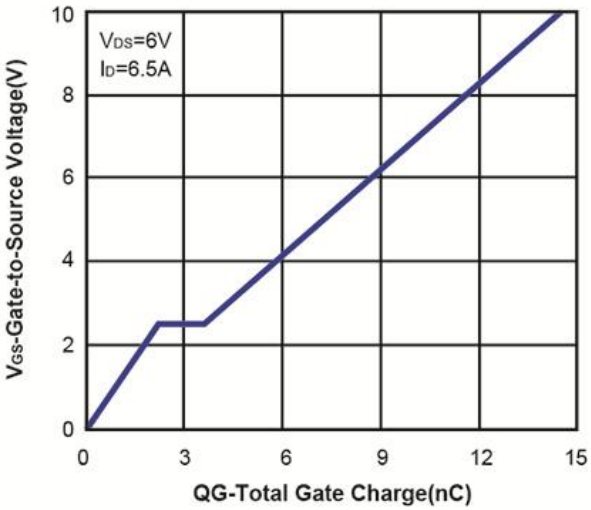
On-Region Characteristics



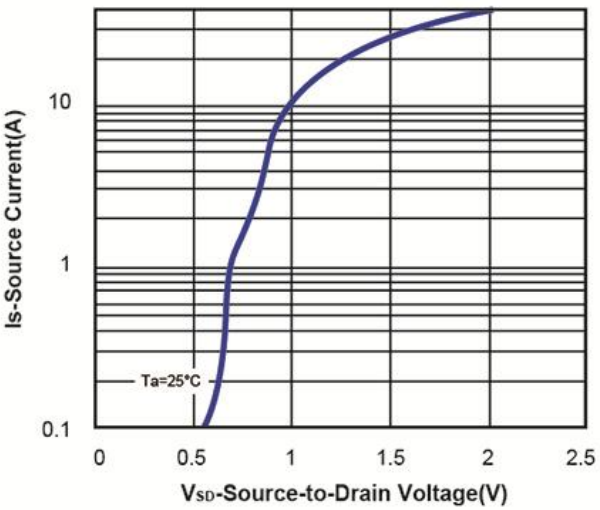
Dual N- and P-Channel 12-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) N-CHANNEL

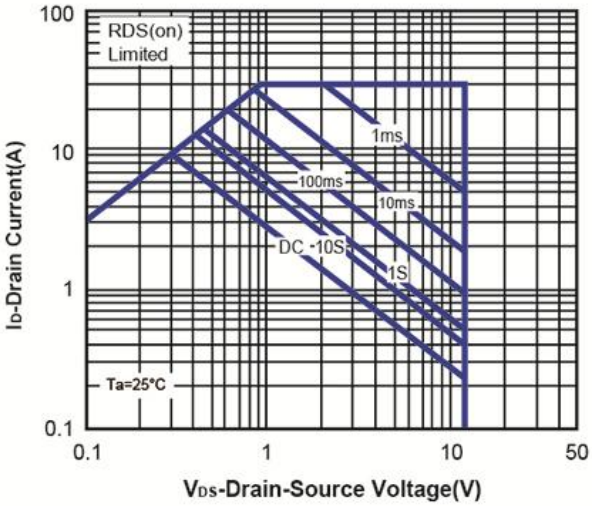
Gate Charge



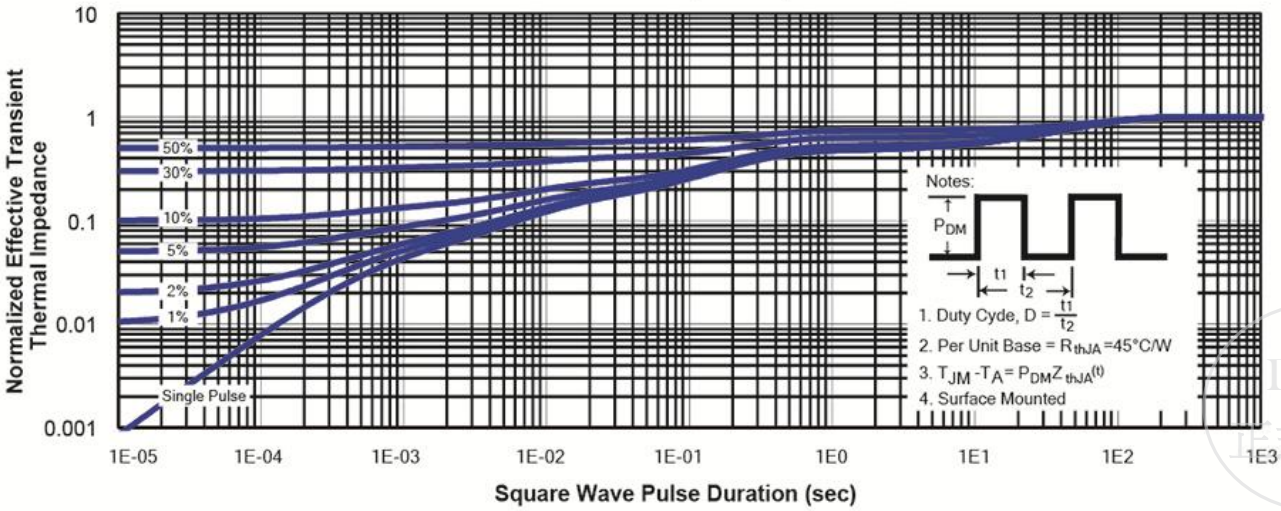
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



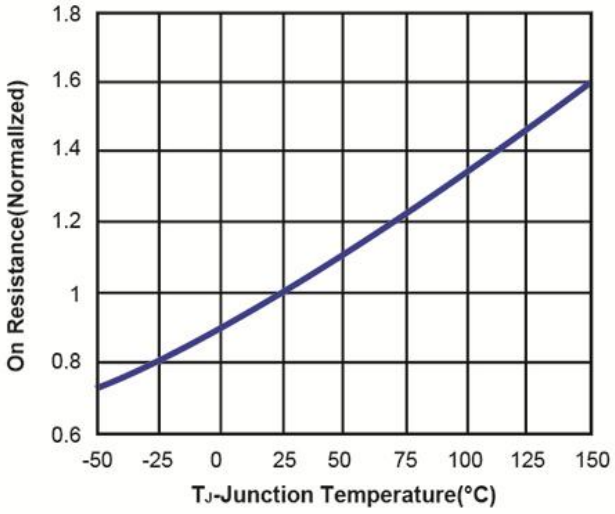
Normalized Thermal Transient Impedance, Junction-to-Ambient



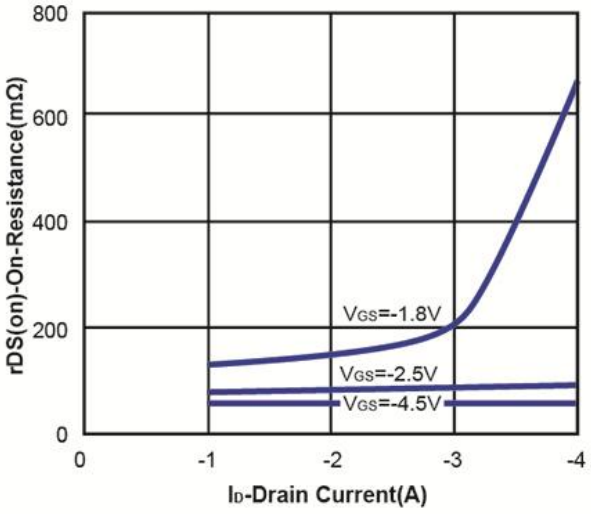
Dual N- and P-Channel 12-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

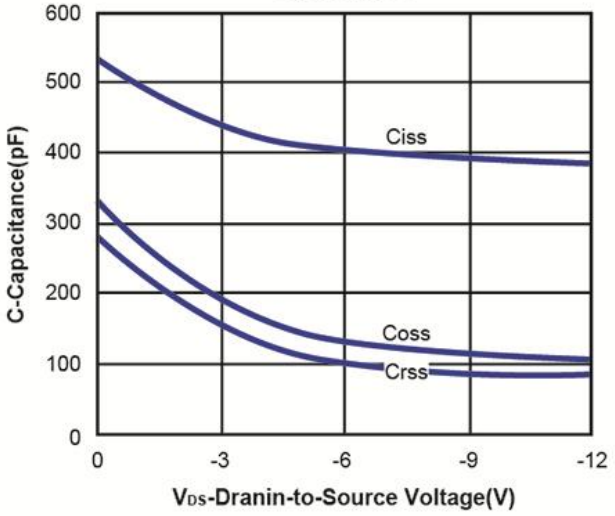
On Resistance vs. Junction Temperature



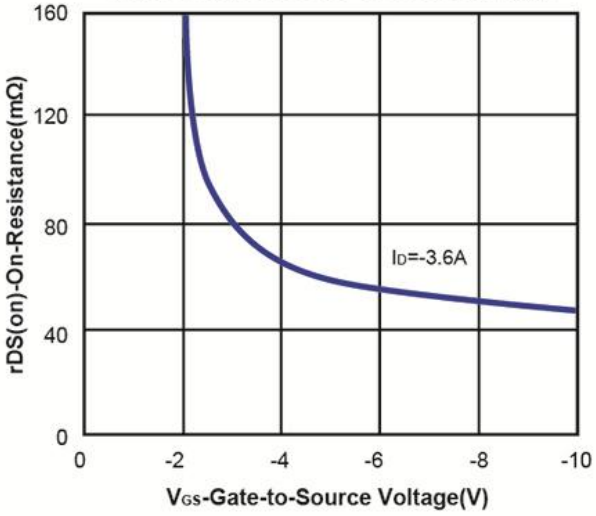
On Resistance vs. Drain Current



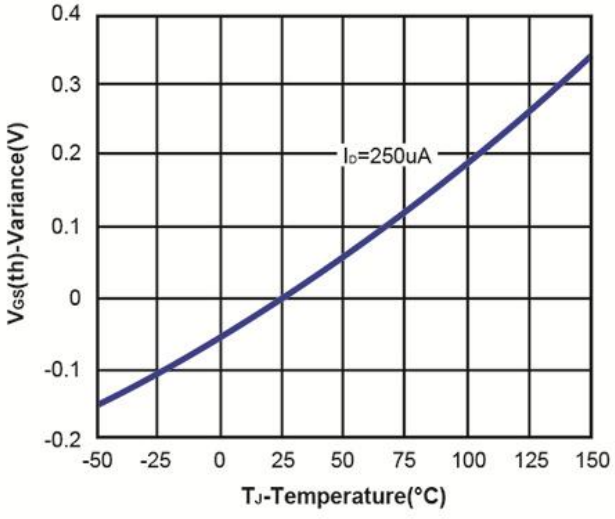
Capacitance



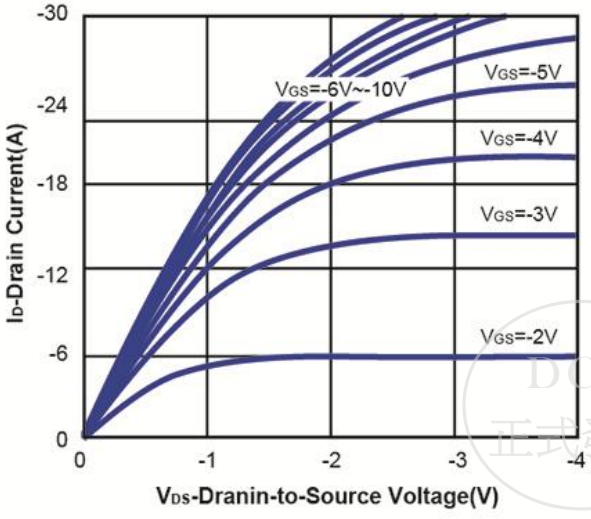
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



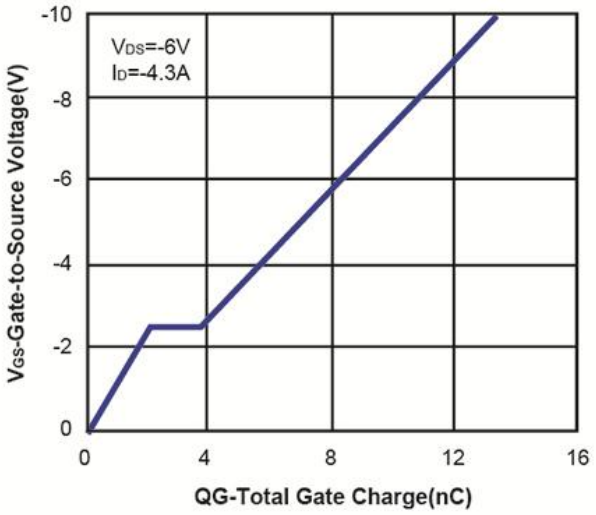
On-Region Characteristics



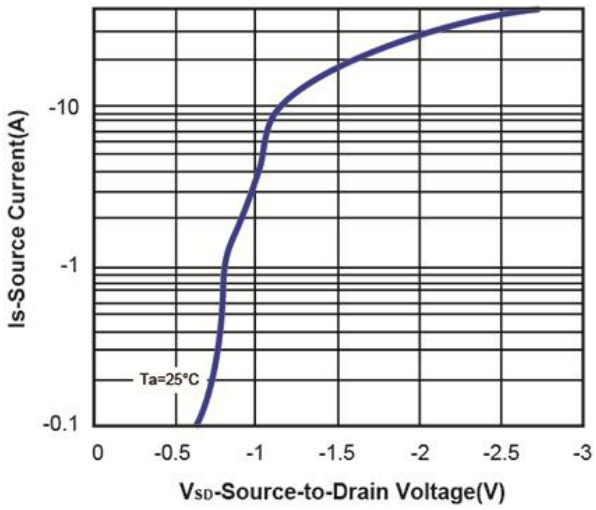
Dual N- and P-Channel 12-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted) P-CHANNEL

Gate Charge



Body-diode characteristics



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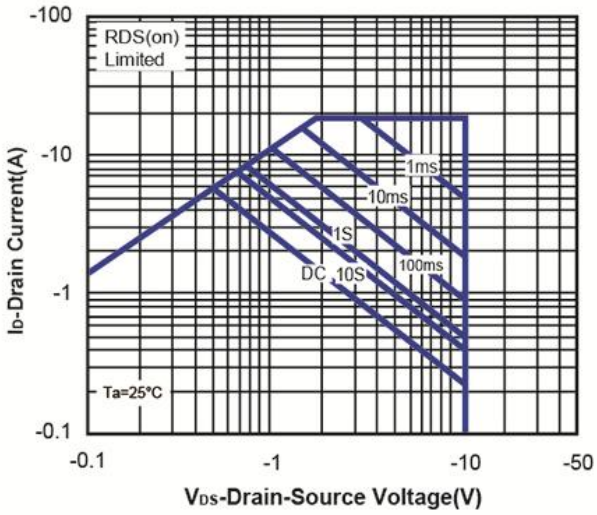
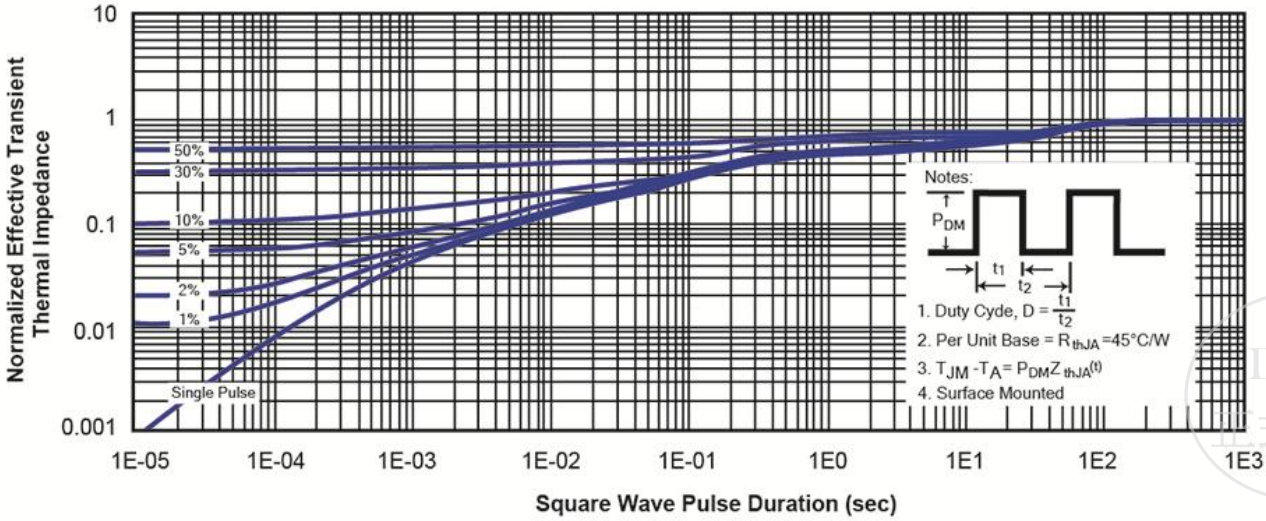
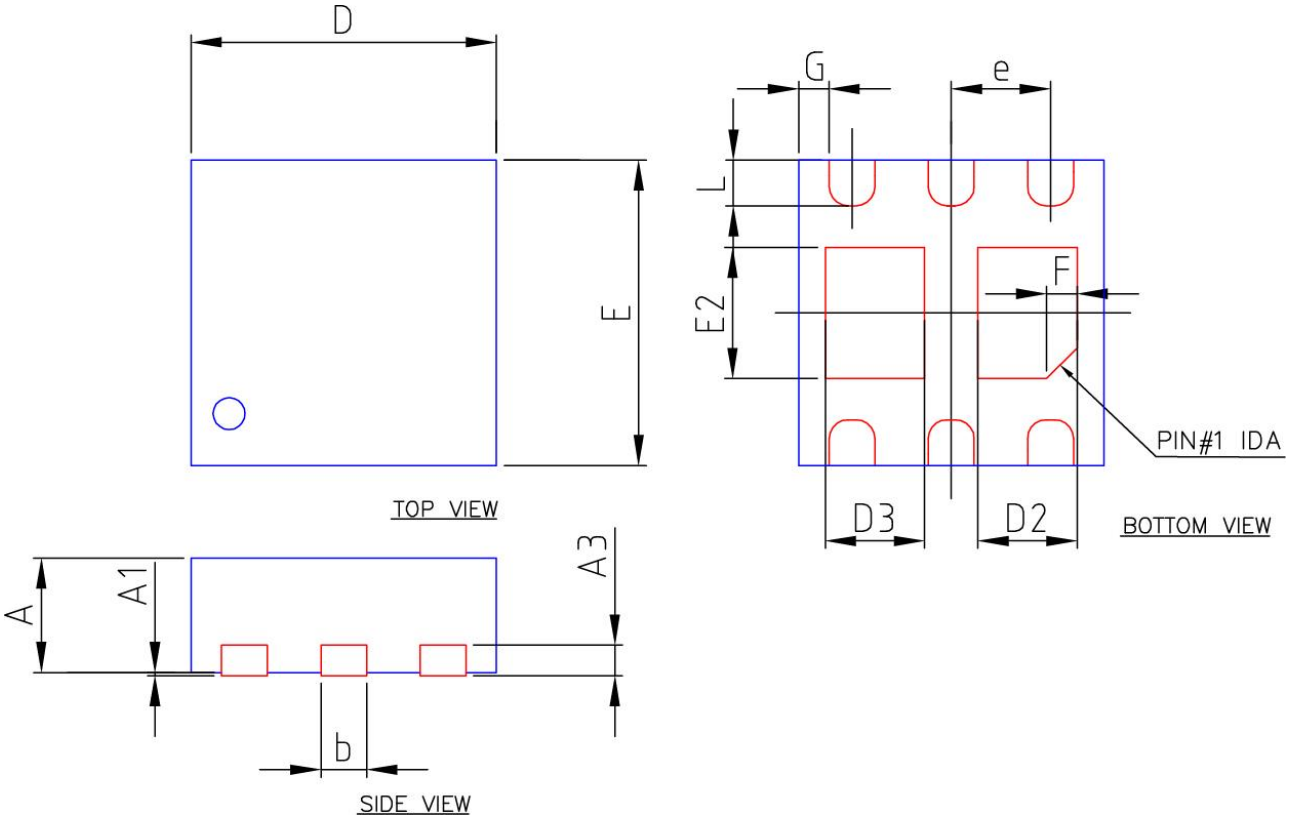


Normalized Thermal Transient Impedance, Junction-to-Ambient



DFN 2x2 6L Dual Package Outline



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.25	0.30	0.35
D		2.00 BSC	
D2	0.60	0.65	0.70
D3	0.60	0.65	0.70
E		2.00 BSC	
E2	0.81	0.86	0.91
e		0.65 BSC	
L	0.25	0.30	0.35
F		0.20 REF	
G	0.15	0.20	0.25