P- Channel 60-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME7345-G is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

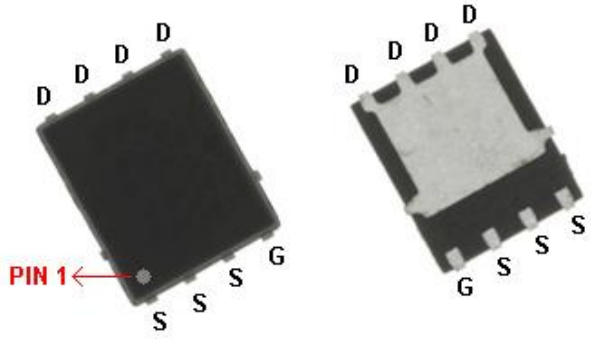
- $R_{DS(ON)} \leqq 15m\Omega @ V_{GS}=-10V$
- $R_{DS(ON)} \leqq 20m\Omega @ V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

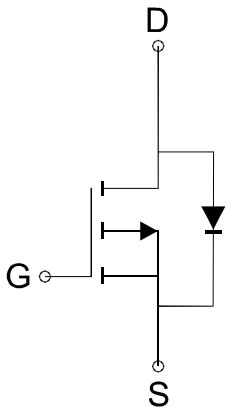
APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

PowerDFN 5x6





P-Channel MOSFET

Ordering Information: ME7345-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	T_C=25℃	I_D	-11	A
	T_C=70℃		-8.6	
Pulsed Drain Current		I_{DM}	-43	A
Maximum Power Dissipation*	T_C=25℃	P_D	2.8	W
	T_C=70℃		1.8	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	45	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_C =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1		-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-60V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=-10V, I_D= -17A		13	15	mΩ
		V_{GS}=-4.5V, I_D= -14A		15	20	
V_{SD}	Diode Forward Voltage	I_S=-17A, V_{GS}=0V		-0.8	-1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-30V, V_{GS}=-10V, I_D=-17A		92.6		nC
Qg	Total Gate Charge	V_{DS}=-30V, V_{GS}=-4.5V, I_D=-17A		44.6		
Qgs	Gate-Source Charge			15.9		
Qgd	Gate-Drain Charge			20.3		
Ciss	Input capacitance	V_{DS}=-30V, V_{GS}=0V, F=1MHz		4765		pF
Coss	Output Capacitance			270		
Crss	Reverse Transfer Capacitance			234		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-30V, R_L =1.8Ω V_{GS}=-10V, R_G=6Ω I_D=-17A		127		ns
t_r	Turn-On Rise Time			103		
$t_{d(off)}$	Turn-Off Delay Time			175		
t_f	Turn-Off Fall Time			57.1		

Notes:a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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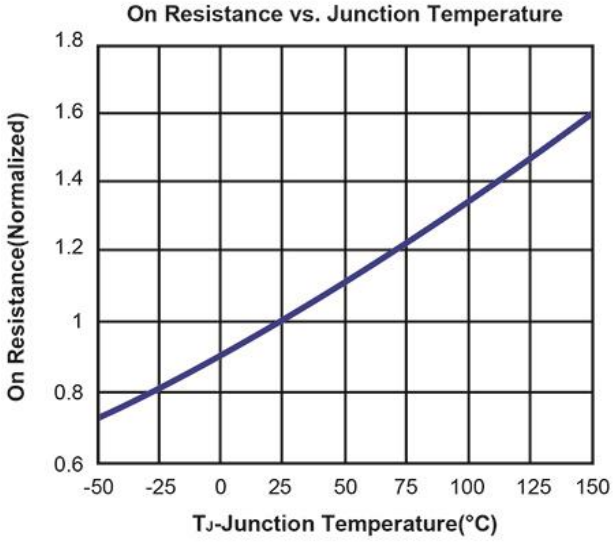
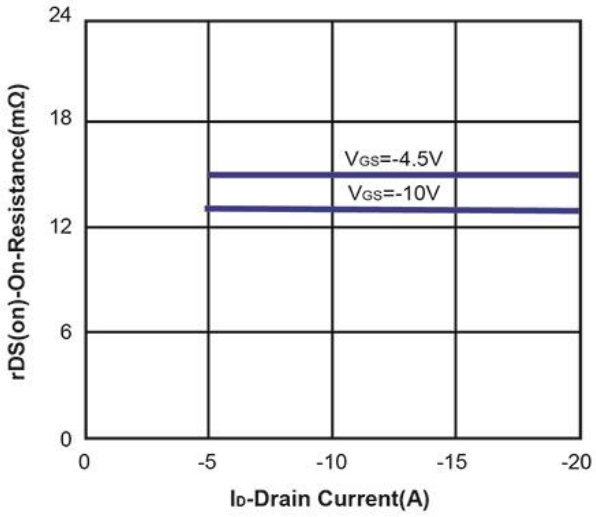
Typical Characteristics (T_J =25℃ Noted)

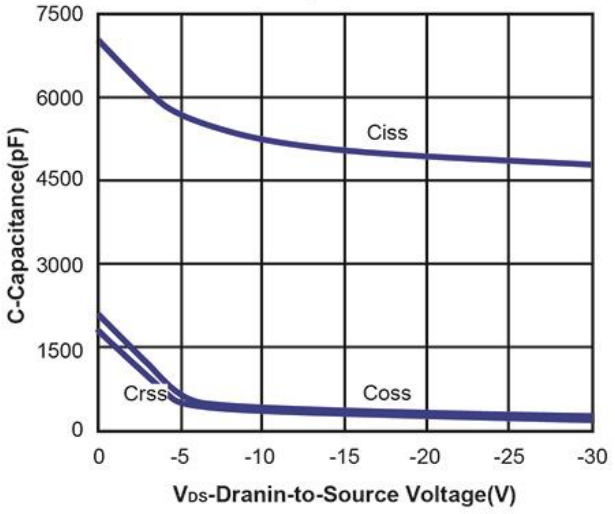
On Resistance vs. Junction Temperature



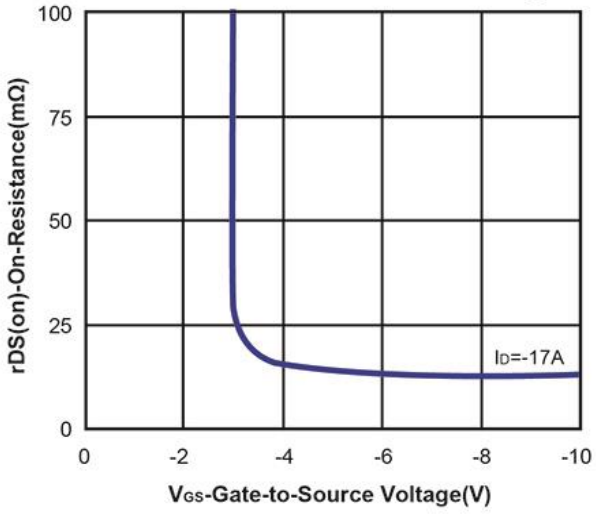
On Resistance vs. Drain Current



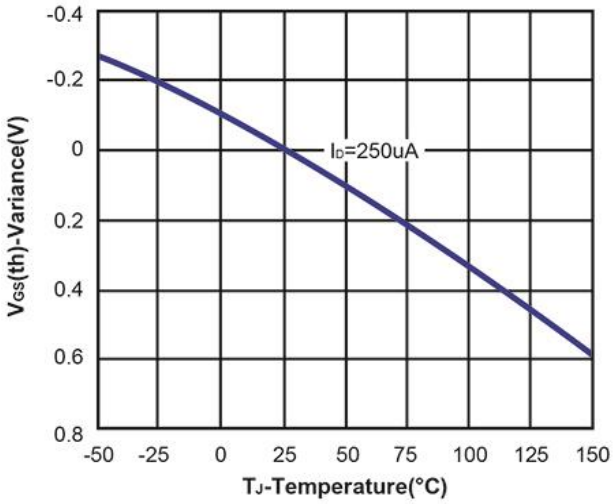
Capacitance



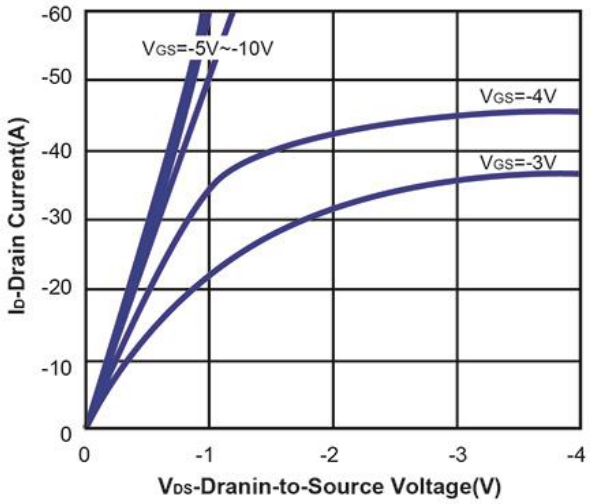
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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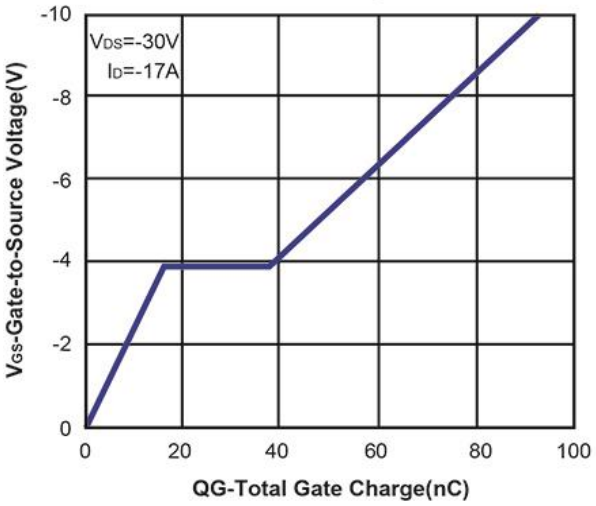
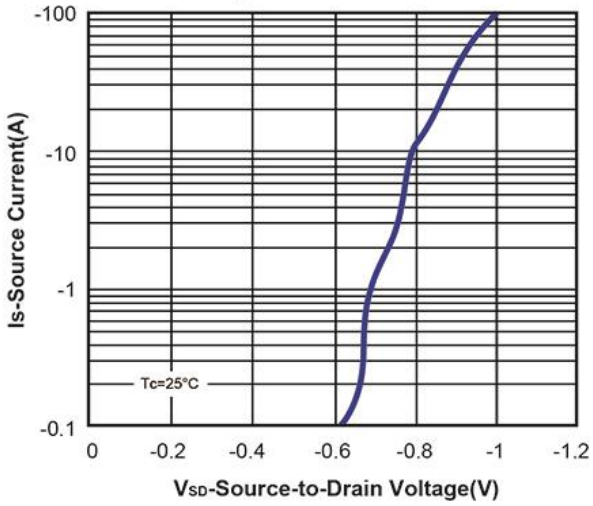
Typical Characteristics (T_J =25℃ Noted)

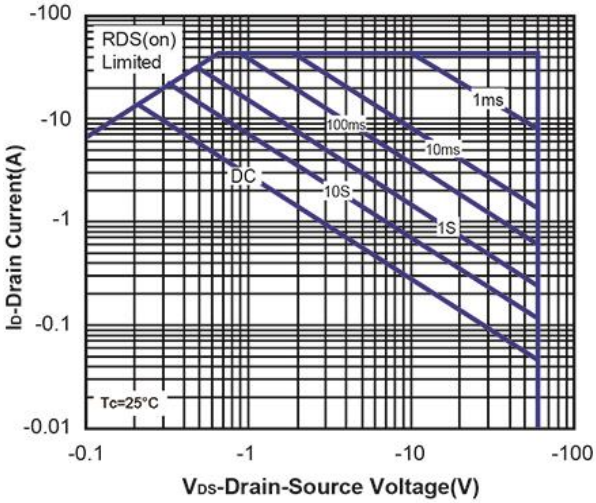
Gate Charge



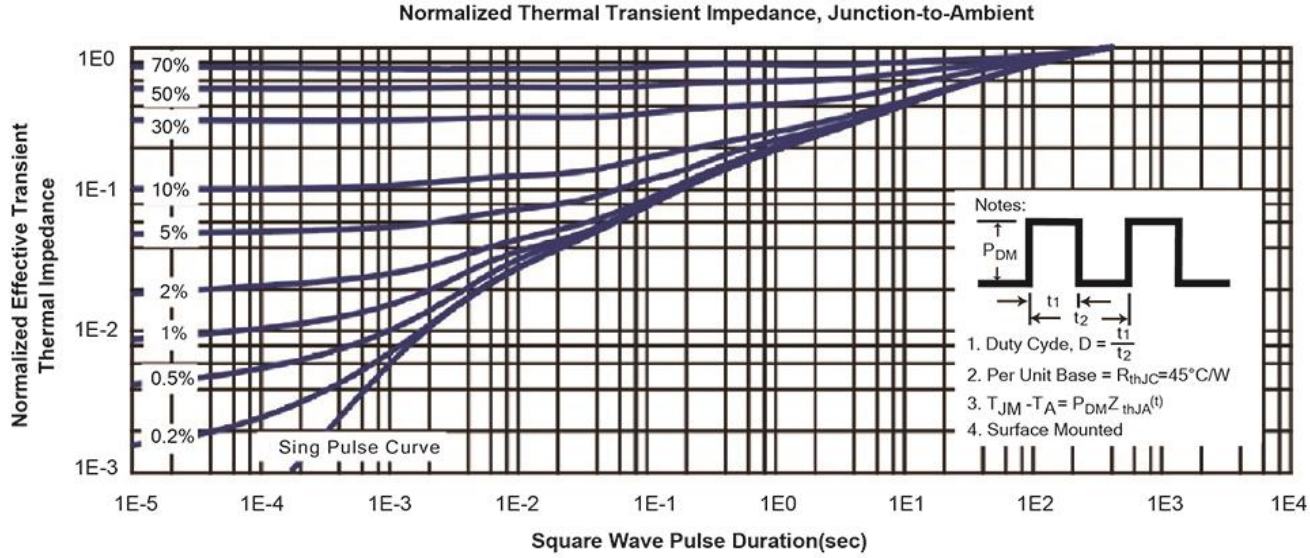
Body-diode characteristics



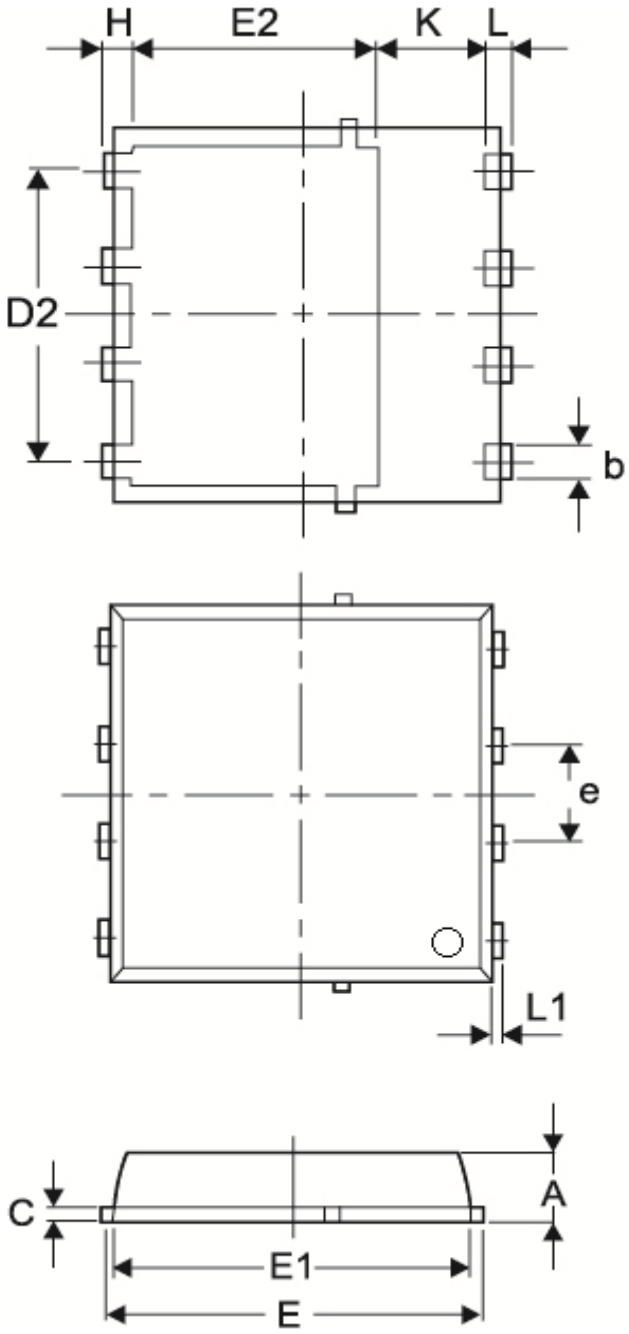
Maximum Forward Biased Safe Operating Area

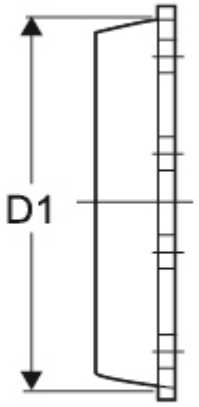


Normalized Thermal Transient Impedance, Junction-to-Ambient



DFN5X6 Package Outline





Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.25
b	0.33	0.51
C	0.155	0.30
D1	4.80	5.00
D2	3.61	3.96
E	5.8	6.20
E1	5.6	5.90
E2	3.35	4.31
e	1.27 BSC	
H	0.35	0.61
K	1.60	-
L	0.35	0.71
L1	0.05	0.20