P-Channel Enhancement Mosfet

GENERAL DESCRIPTION

The ME7423 P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦13mΩ@V_{GS}=-10V
- $R_{DS(ON)}$ ≦17mΩ@ V_{GS}=-4.5V

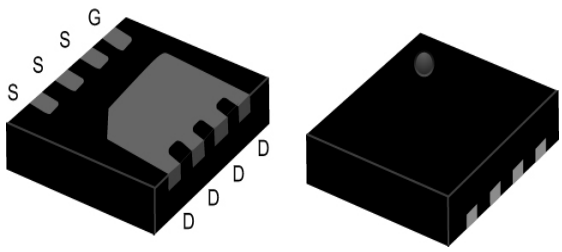
APPLICATIONS

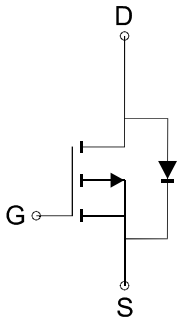
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

(DFN 3.3x3.3)

Top View





P-Channel MOSFET

Ordering Information: ME7423 (Pb-free)

ME7423-G (Green product-Halogen free)

Absolute Maximum Ratings (T_j=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(tJ=150℃)	T_A=25℃	I_D	-17	A
	T_A=70℃		-13	
Pulsed Drain Current		I_{DM}	68	A
Maximum Power Dissipation	T_A=25℃	P_D	3.8	W
	T_A=70℃		2.4	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	33	℃/W

The device mounted on 1in^2 FR4 board with 2 oz copper

P-Channel Enhancement Mosfet

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1		-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=-10V, I_D=-11.7A		10	13	mΩ
		V_{GS}=-4.5V, I_D=-9A		13	17	
V_{SD}	Diode Forward Voltage	I_S=-9A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge (-10V)	V_{DS}=-15V,V_{GS}=-10V, I_D=-11.7A		70		nC
Qg	Total Gate Charge (-4.5V)			35		
Qgs	Gate-Source Charge			13		
Qgd	Gate-Drain Charge			17		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V,f=1MHz		3020		pF
Coss	Output Capacitance			400		
Crss	Reverse Transfer Capacitance			135		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-15V, R_L=15Ω R_{GEN}=6Ω, V_{GS}=-10V		47		ns
t_r	Turn-On Rise Time			20		
$t_{d(off)}$	Turn-Off Delay Time			212		
t_f	Turn-Off Fall Time			61		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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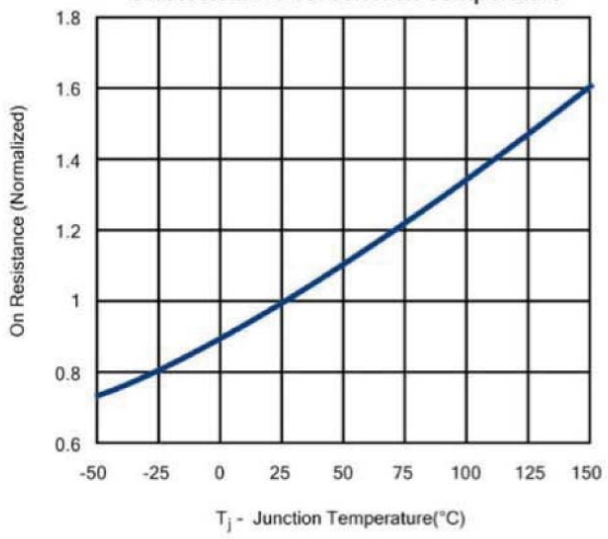
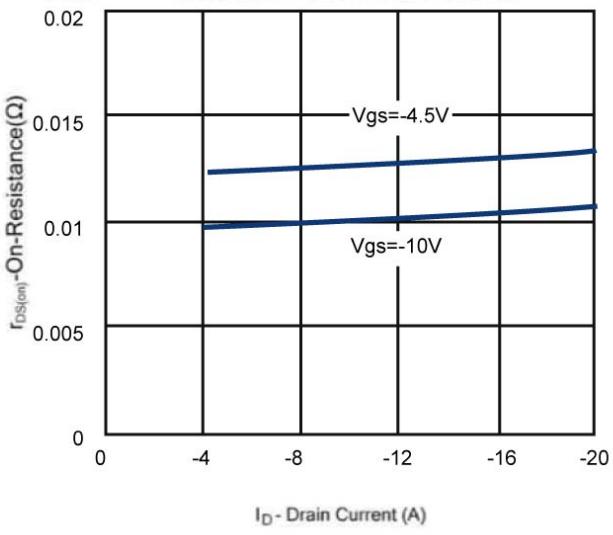
Typical Characteristics (T_J =25℃ Noted)

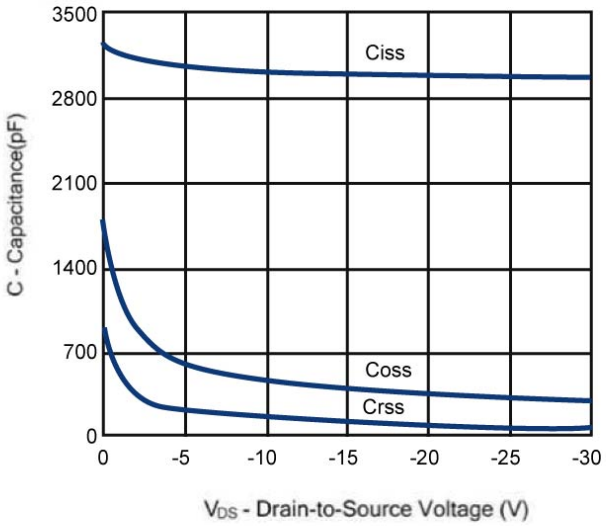
On Resistance vs. Junction Temperature



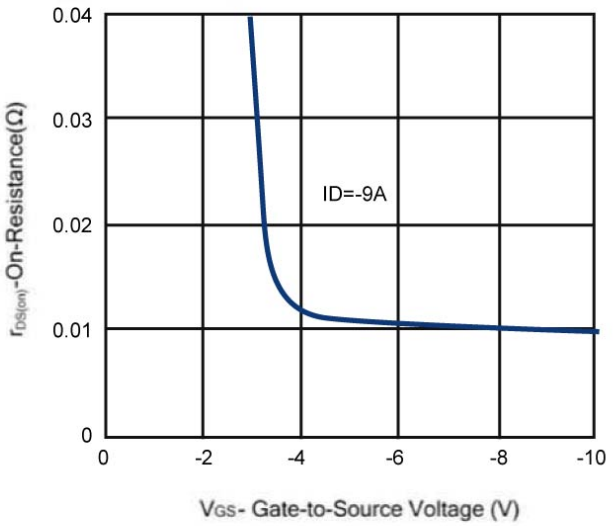
On-Resistance vs. Drain Current



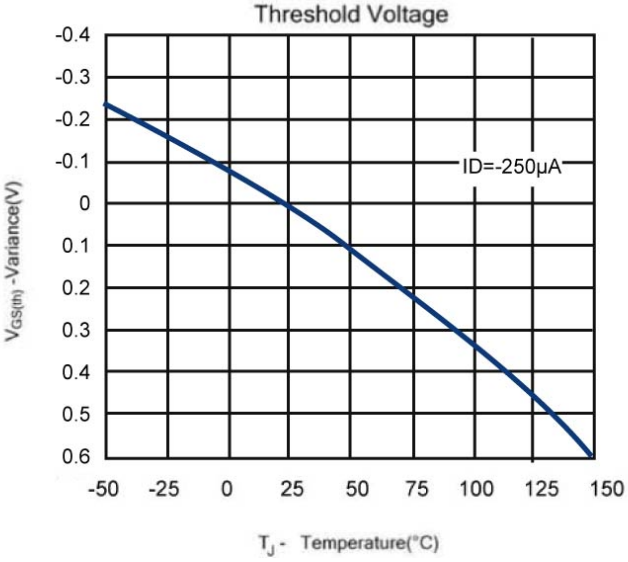
Capacitance



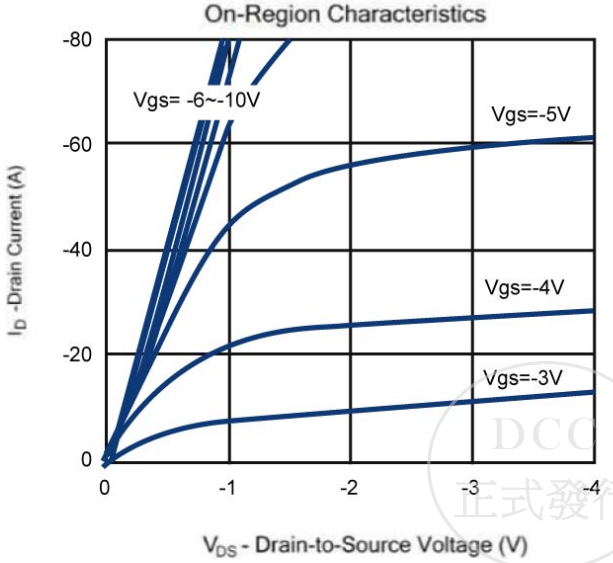
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



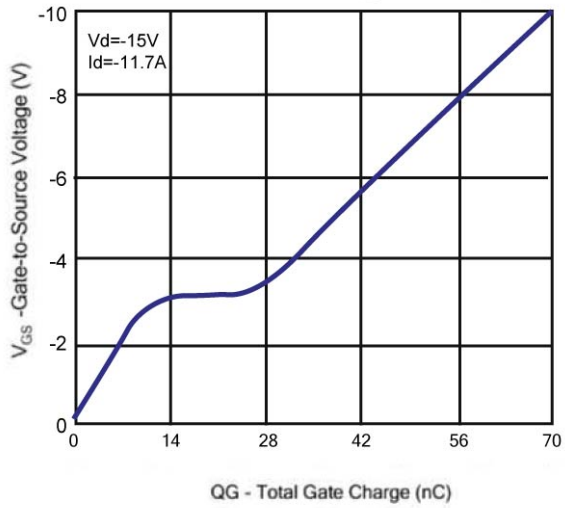
On-Region Characteristics



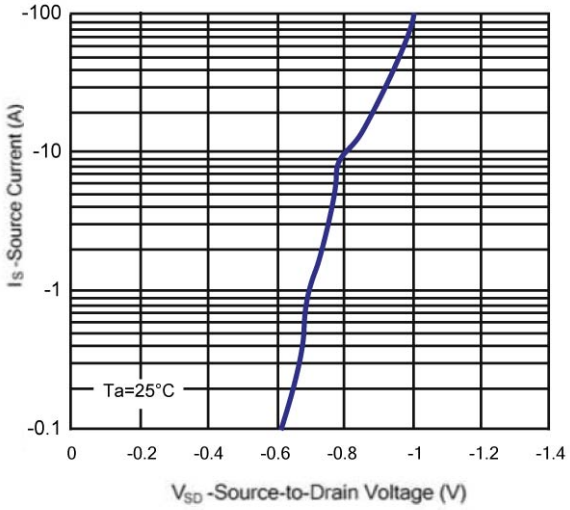
P-Channel Enhancement Mosfet

Typical Characteristics (T_J =25℃ Noted)

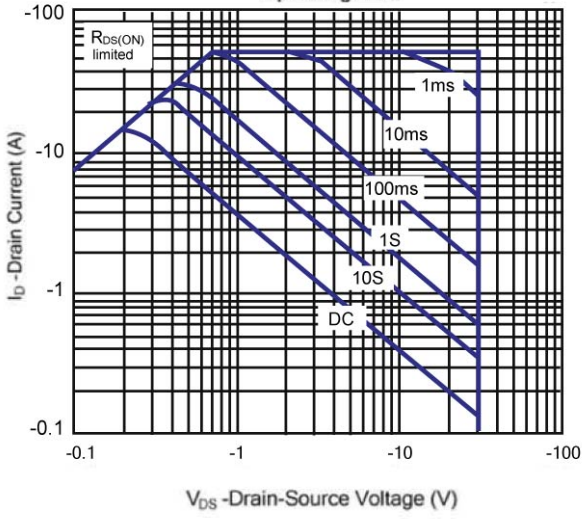
Gate Charge



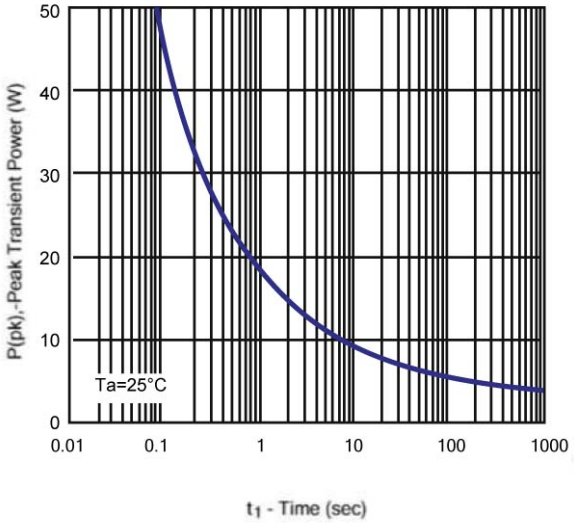
Source to Drain Diode Forward Voltage



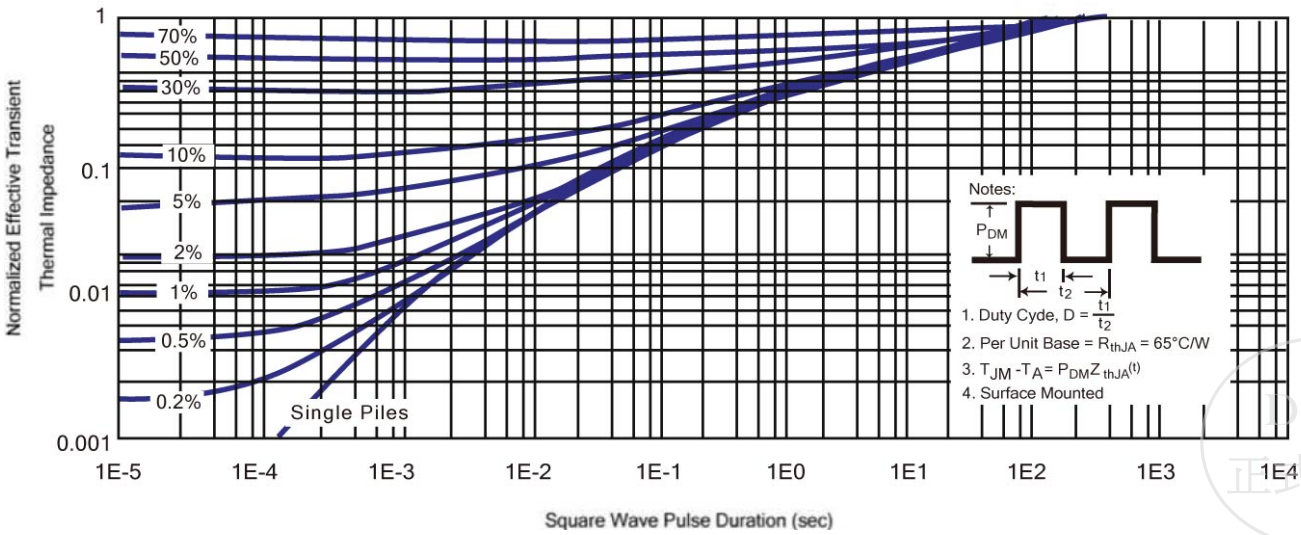
Maximum Forward Biased Safe Operating Area



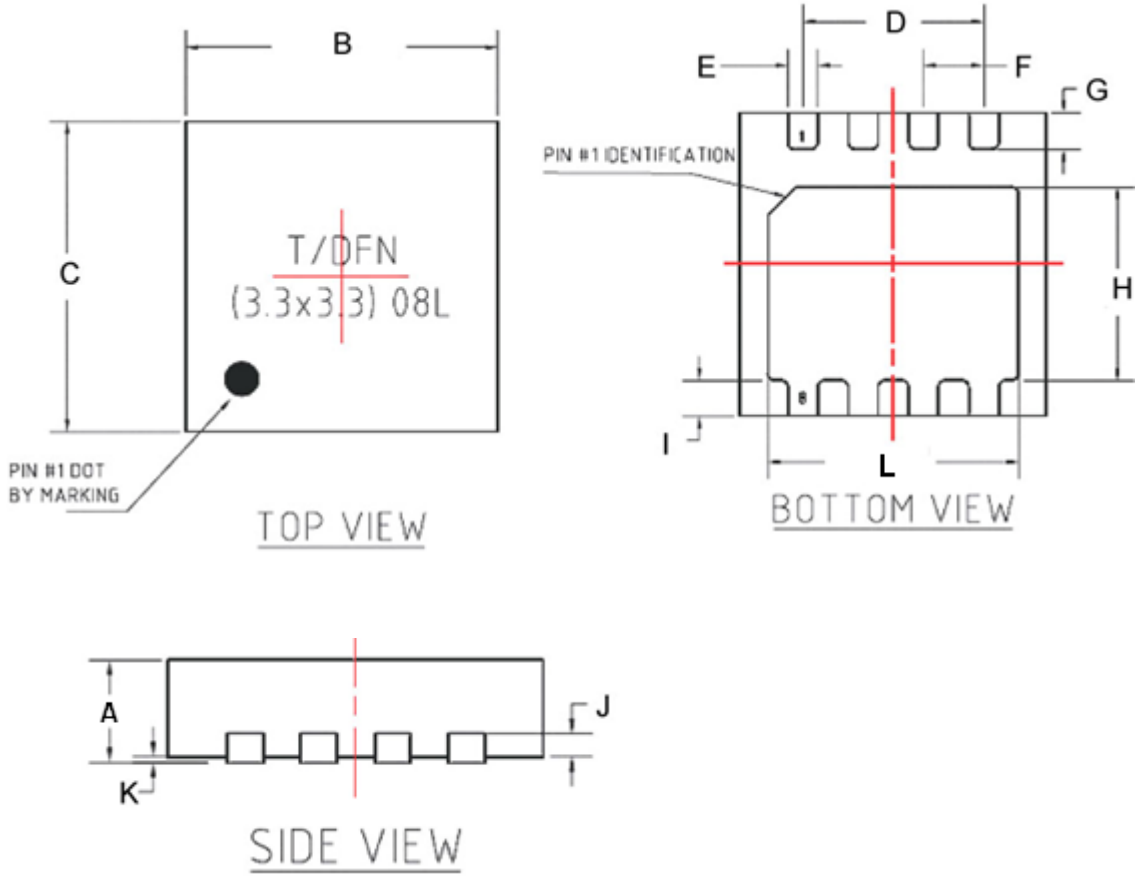
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



DFN 3.3x3.3 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.700	1.000
B	3.250	3.350
C	3.250	3.350
D	1.95REF.	
E	0.270	0.370
F	0.65BSC	
G	0.350	0.450
H	2.050	2.150
I	0.385	0.395
J	0.195	0.211
K	0.000	0.050
L	2.650	2.750