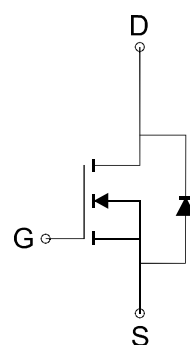
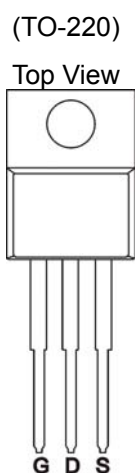


N- Channel 75-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME75N75T is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

PIN CONFIGURATION



N-Channel MOSFET

FEATURES

- $R_{DS(ON)} \leq 10m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter
- Load Switch

Ordering Information: ME75N75T (Pb-free)

ME75N75T-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	75	V
Gate-Source Voltage		V_{GSS}	± 25	V
Continuous Drain Current*	$T_c=25^\circ\text{C}$	I_D	93	A
	$T_c=70^\circ\text{C}$		78	
Pulsed Drain Current		I_{DM}	372	A
Maximum Power Dissipation	$T_c=25^\circ\text{C}$	P_D	200	W
	$T_c=70^\circ\text{C}$		140	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Thermal Resistance-Junction to Case**		$R_{\theta JC}$	0.75	$^\circ\text{C/W}$

* Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 80A.

** The device mounted on 1in² FR4 board with 2 oz copper.

N- Channel 75-V (D-S) MOSFET

Electrical Characteristics (TA=25°C Unless Otherwise Specified)

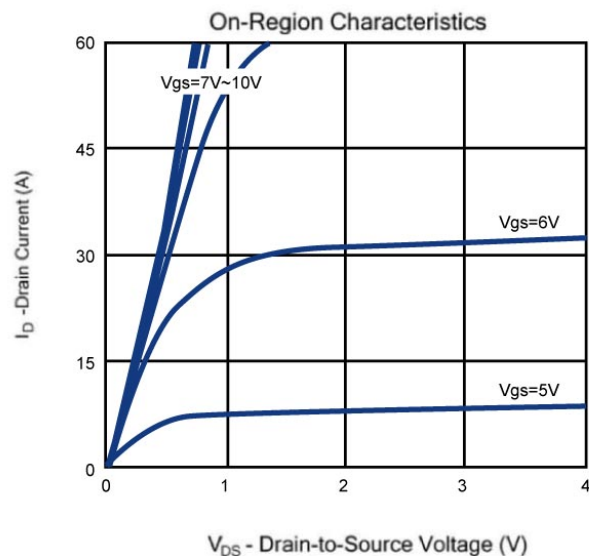
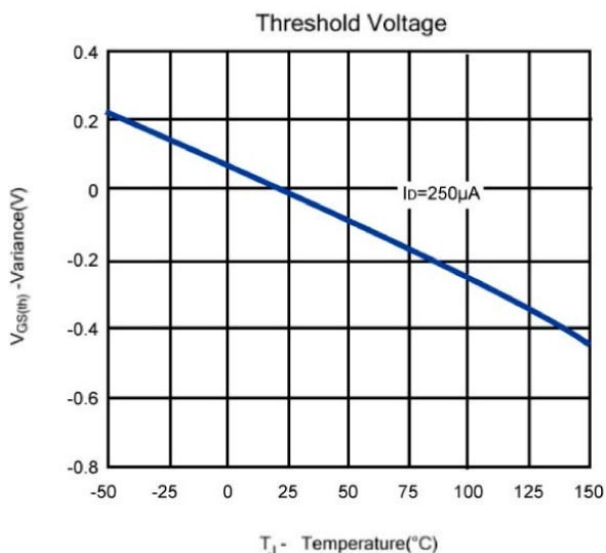
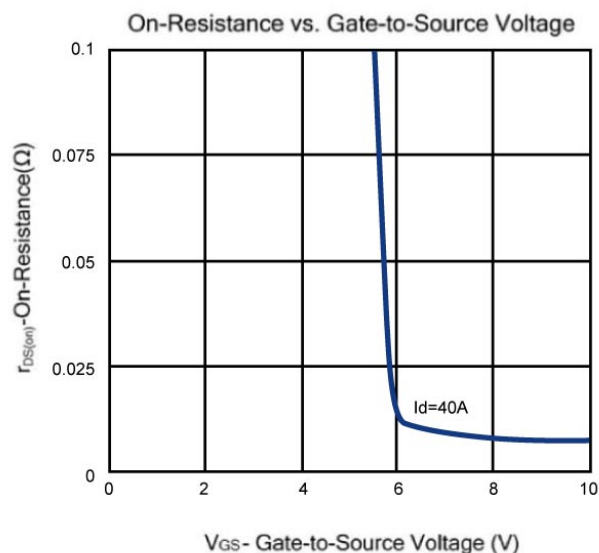
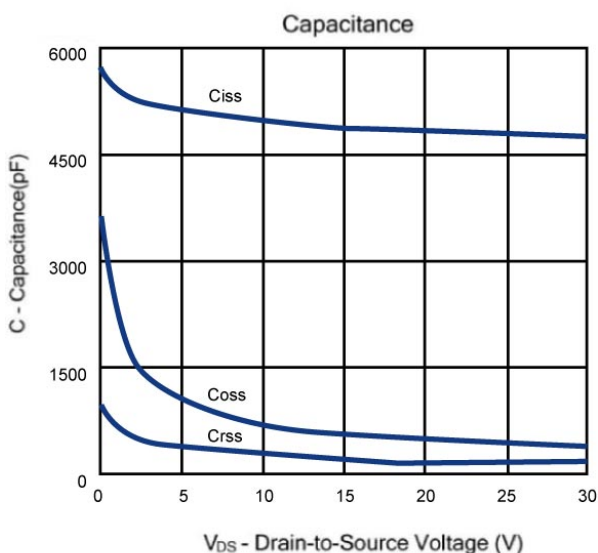
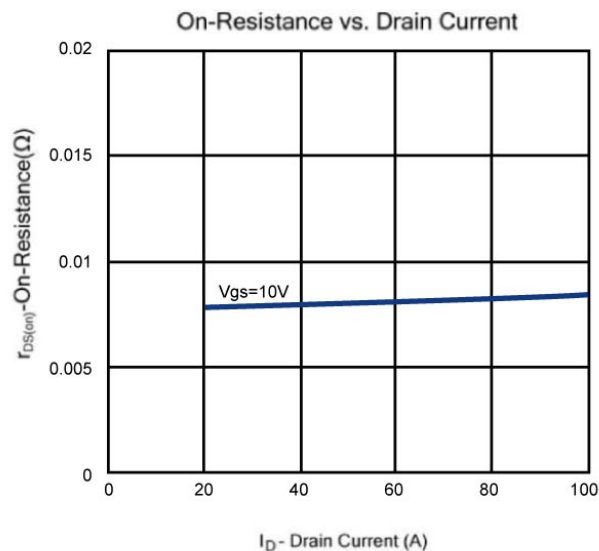
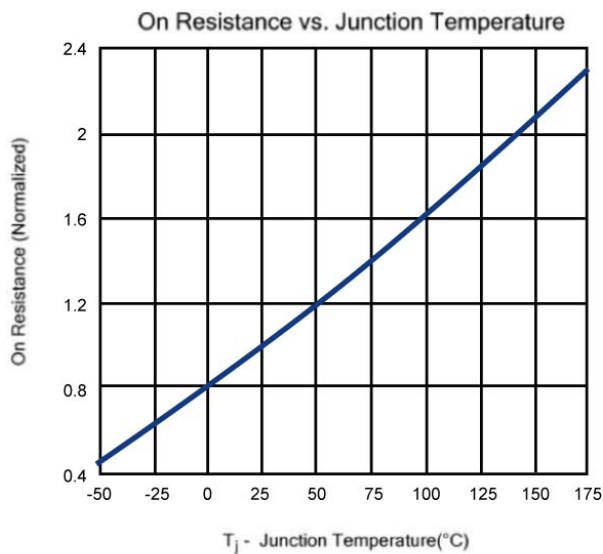
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	75			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μ A	2.0		4.0	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} = $\pm$ 25V			$\pm$ 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =75V, V _{GS} =0V			1	μ A
R _{DS(ON)}	Drain-Source On-Resistance*	V _{GS} =10V, I _D =40A		8	10	m Ω
V _{SD}	Diode Forward Voltage *	I _S =40A, V _{GS} =0V		0.9	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DD} =60V, V _{GS} =10V, I _D =75A		112		nC
Q _g	Total Gate Charge	V _{DD} =60V, V _{GS} =4.5V, I _D =75A		28		
Q _{gs}	Gate-Source Charge			27		
Q _{gd}	Gate-Drain Charge			30		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		0.9		Ω
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz		4900		pF
C _{oss}	Output Capacitance			534		
C _{rss}	Reverse Transfer Capacitance			175		
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, R _L =15 Ω V _{DD} =30V, R _G =10 Ω		48		ns
t _r	Turn-On Rise Time			36		
t _{d(off)}	Turn-Off Delay Time			144		
t _f	Turn-Off Fall Time			48		

Notes: a. pulse test: pulse width $\leq$ 300us, duty cycle $\leq$ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

N- Channel 75-V (D-S) MOSFET

Typical Characteristics (T_J =25°C Noted)



N- Channel 75-V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)

