P-Channel 35V Enhancement Mode MOSFET, ESD Protected

GENERAL DESCRIPTION

The ME7607 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

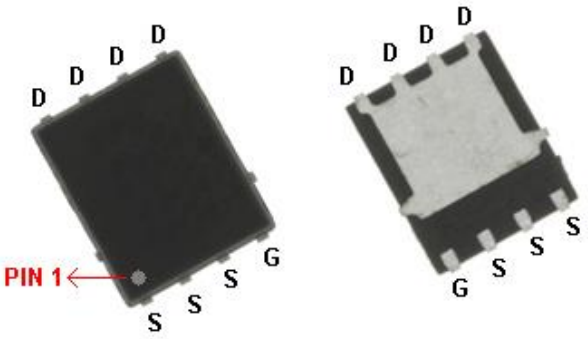
- $R_{DS(ON)} \leqq 6m\Omega @ V_{GS}=-10V$
- $R_{DS(ON)} \leqq 9m\Omega @ V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

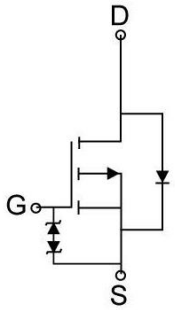
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

PowerDFN 5x6





P-Channel MOSFET

Ordering Information: ME7607(Pb-free)

ME7607-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DSS}	-35	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	-17	A
	T_A=70℃		-13.6	
Pulsed Drain Current		I_{DM}	-68	
Maximum Power Dissipation*	T_A=25℃	P_D	2.8	W
	T_A=70℃		1.8	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	45	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{BR(DSS)}$	Drain-source breakdown voltage	ID=-252μA , V_{GS}=0V	-35			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}= V_{DS}, I_D=-250μA	-1		-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±16V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-35V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=-10V, I_D= -20A		4	6	mΩ
		V_{GS}=-4.5V, I_D= -20A		6	9	
V_{SD}	Diode Forward Voltage	I_{DR}=-20A, V_{GS}=0V		-0.8	-1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DD}=-24V, V_{GS}=-10V, I_D=-20A		118		nC
Qg	Total Gate Charge	V_{DD}=-24V, V_{GS}=-4.5V, I_D=-20A		59.8		
Qgs	Gate-Source Charge			23.3		
Qgd	Gate-Drain Charge			32.7		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=-1MHZ		5359		pF
Coss	Output Capacitance			652		
Crss	Reverse Transfer Capacitance			562		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-24V, R_L =1.2Ω V_{GS}=-10V,R_G=6Ω I_D=-20A		206		ns
t_r	Turn-On Rise Time			164		
$t_{d(off)}$	Turn-Off Delay Time			247		
t_f	Turn-Off Fall Time			106		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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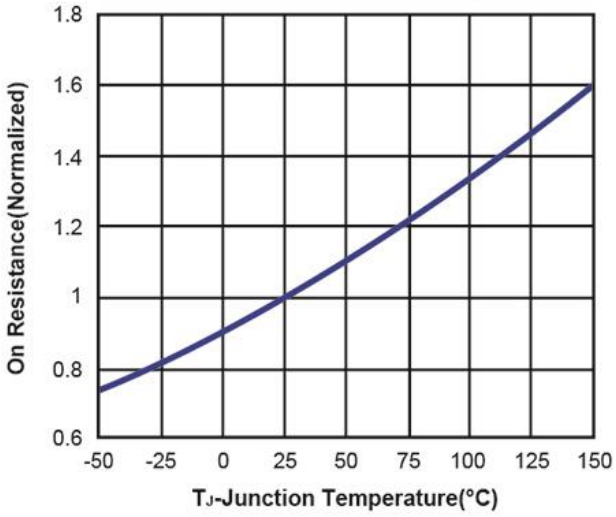
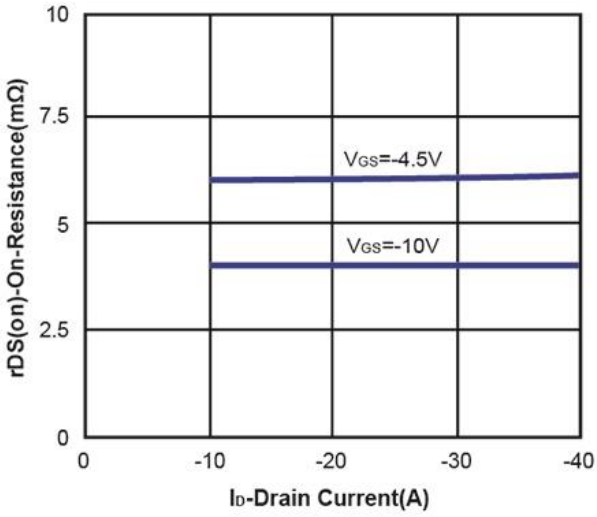
Typical Characteristics (T_J =25℃ Noted)

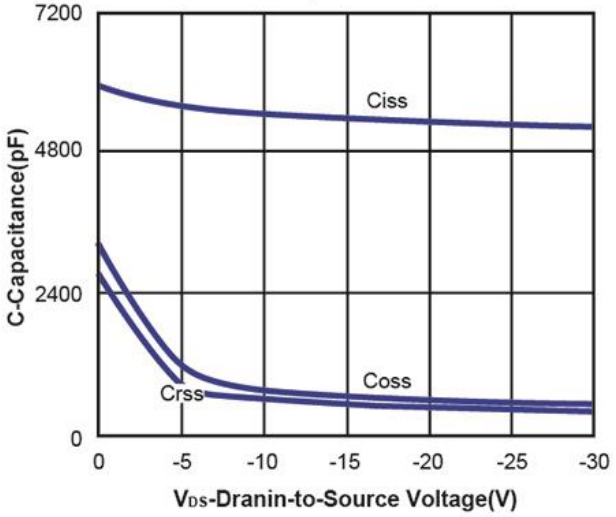
On Resistance vs. Junction Temperature



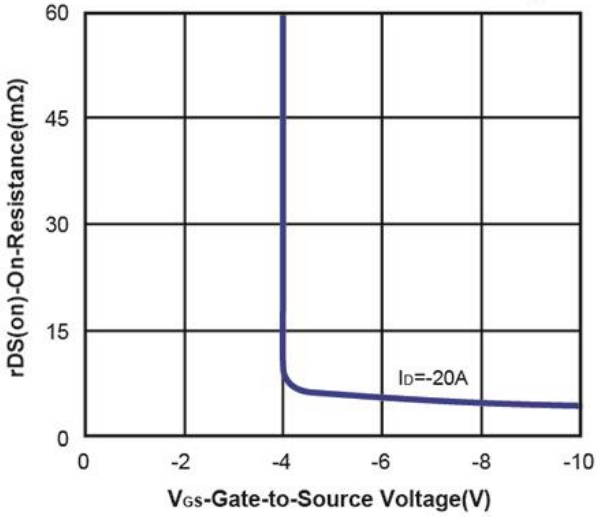
On Resistance vs. Drain Current



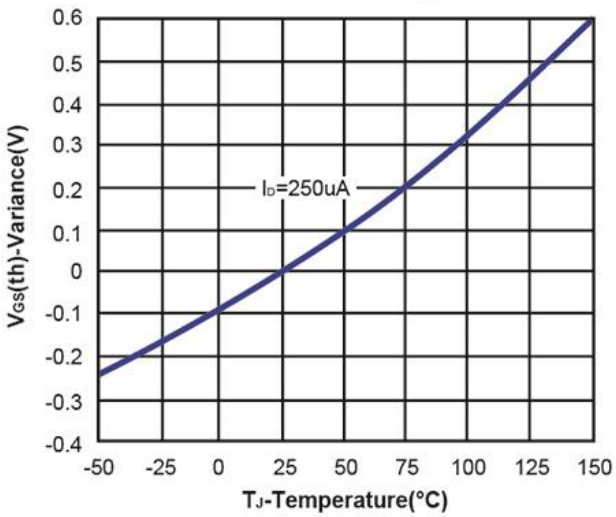
Capacitance



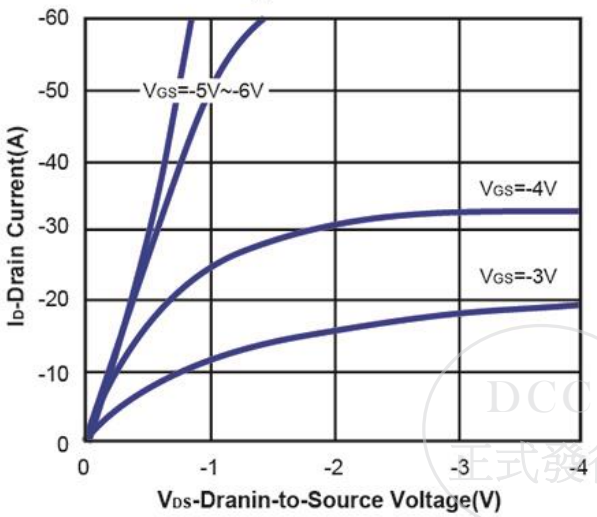
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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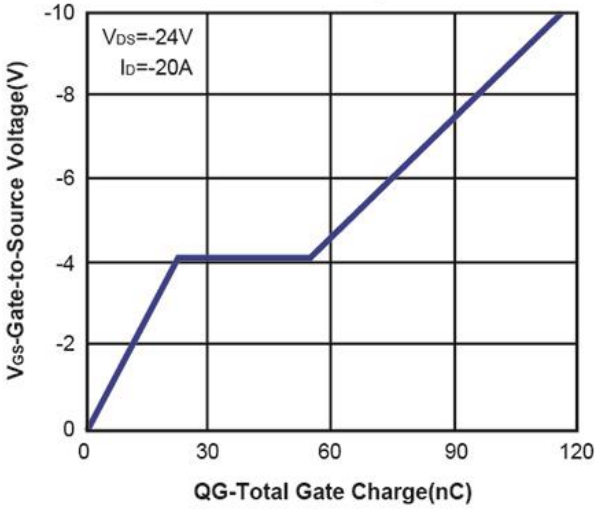
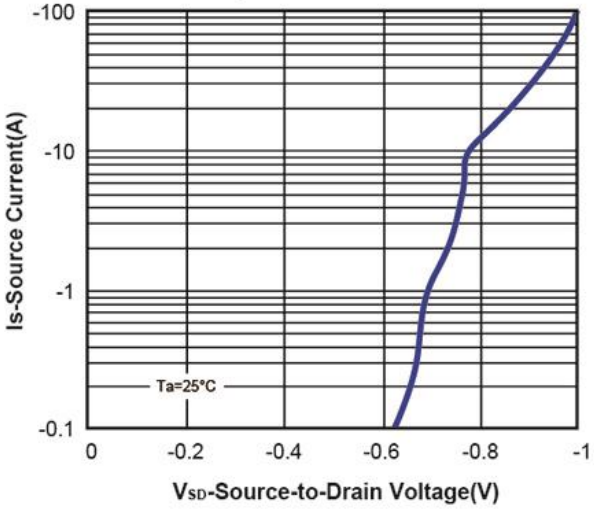
Typical Characteristics (T_J =25℃ Noted)

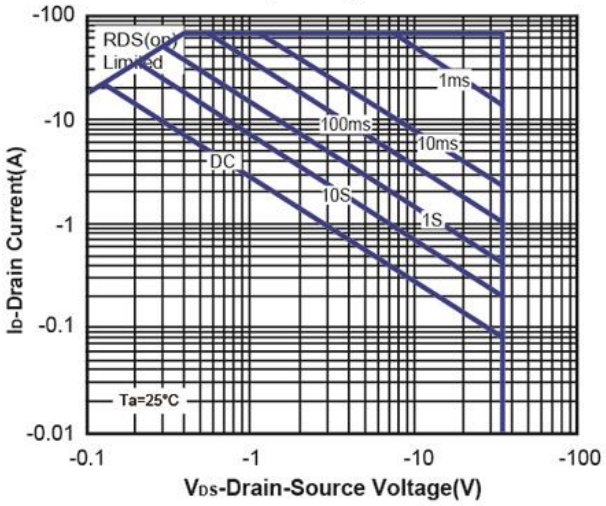
Gate Charge



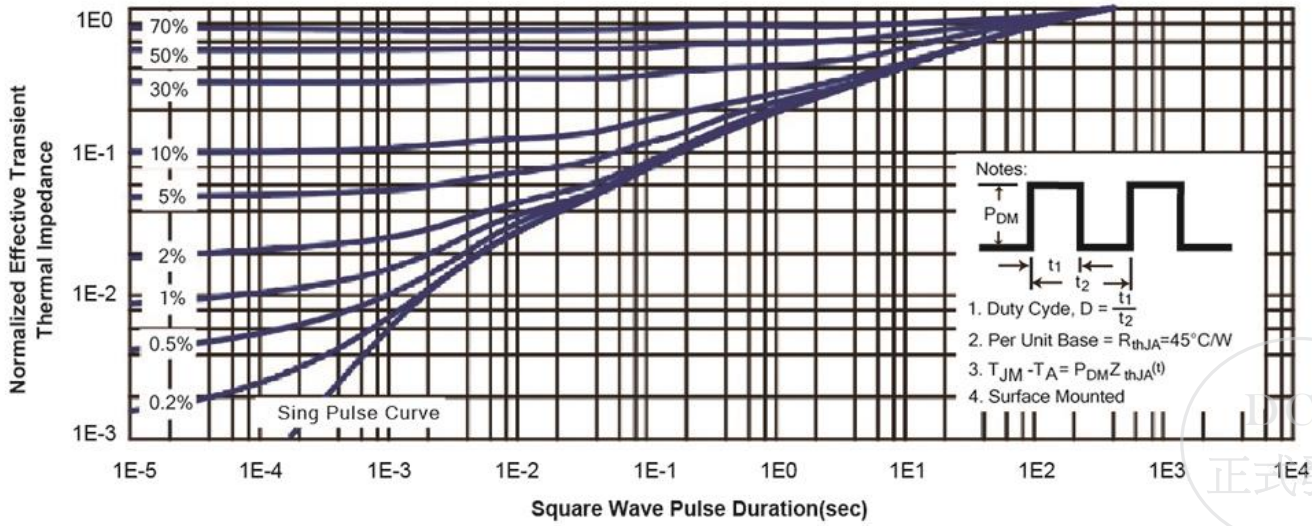
Body-diode characteristics



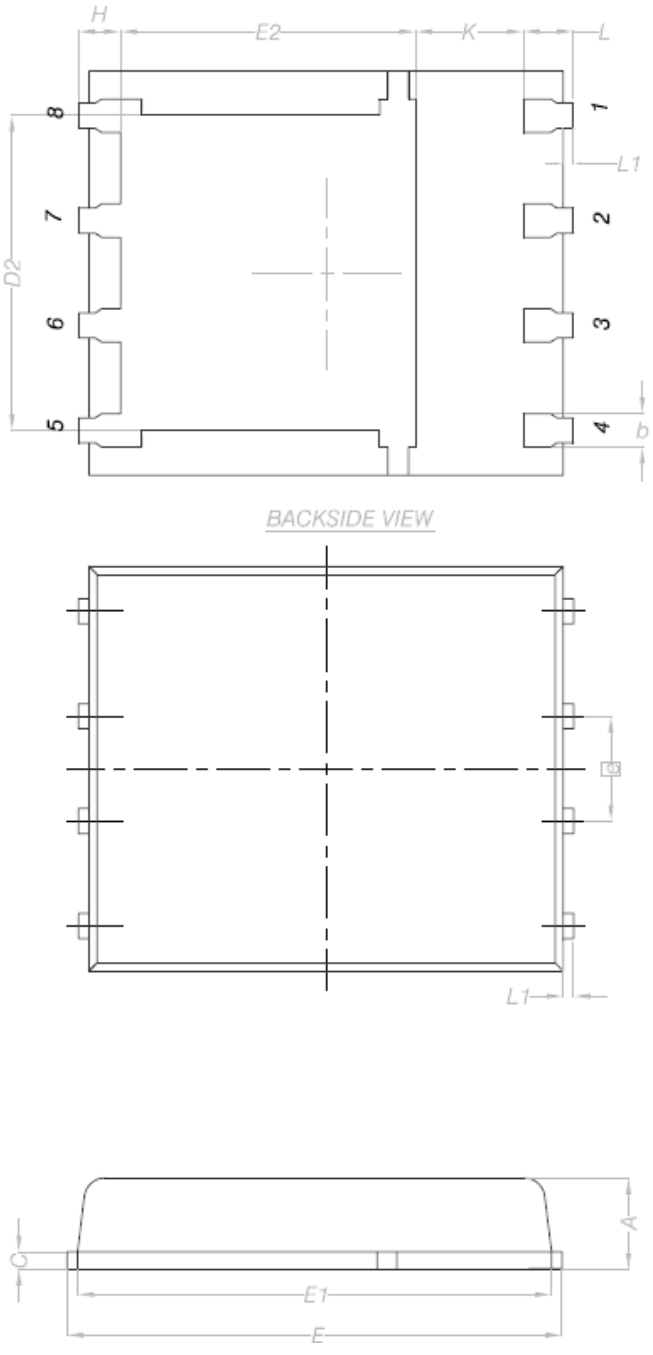
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



PowerDFN5x6 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.10
b	0.33	0.51
C	0.20	0.30
D1	4.80	5.00
D2	3.61	3.96
E	5.90	6.10
E1	5.70	5.80
E2	3.38	3.78
e	1.27 BSC	
H	0.41	0.61
K	1.10	-
L	0.51	0.71
L1	0.06	0.20
α	0°	12°