

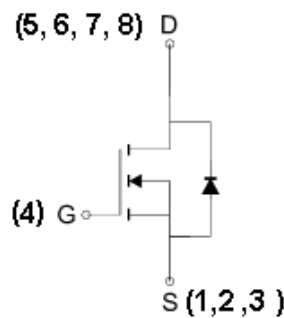
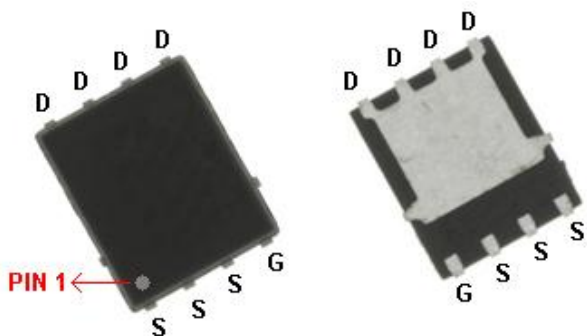
N-Channel 30V(D-S) Enhancement MOSFET

GENERAL DESCRIPTION

The ME7644 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

PowerDFN 5x6



N-Channel MOSFET

Ordering Information: ME7644 (Pb-free)

ME7644-G (Green product-Halogen free)

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V _{DS}	30	V
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current*	T _A =25°C	I _D	45	A
	T _A =70°C		36	
Pulsed Drain Current		I _{DM}	179	A
Maximum Power Dissipation*	T _A =25°C	P _D	2.78	W
	T _A =70°C		1.78	
Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C
Thermal Resistance-Junction to Ambient*		R _{θJA}	45	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (T_J = 25°C Unless Otherwise Specified)

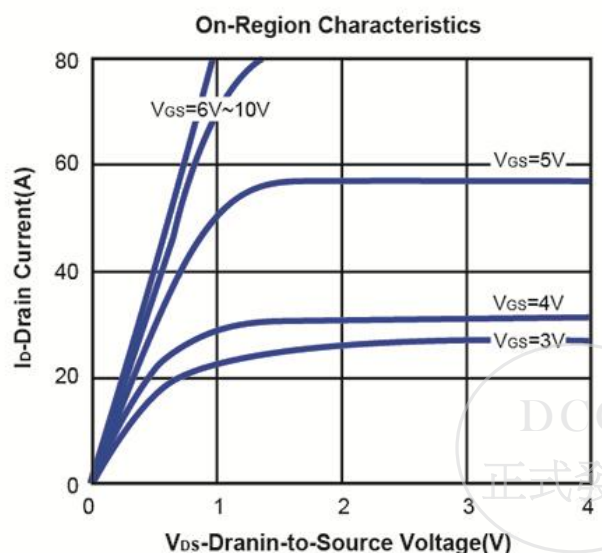
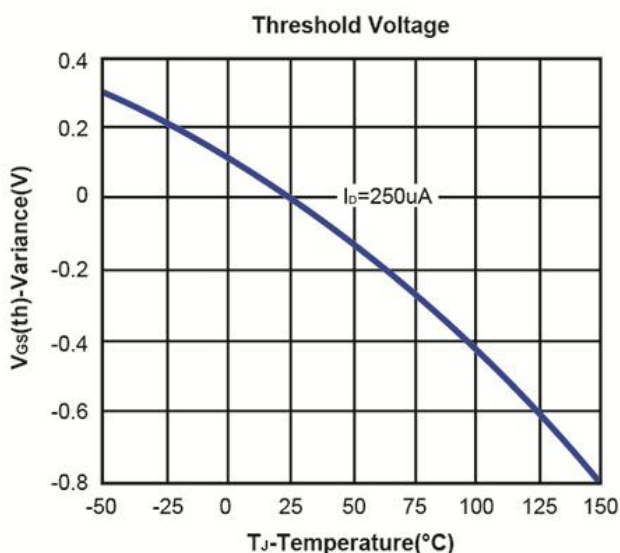
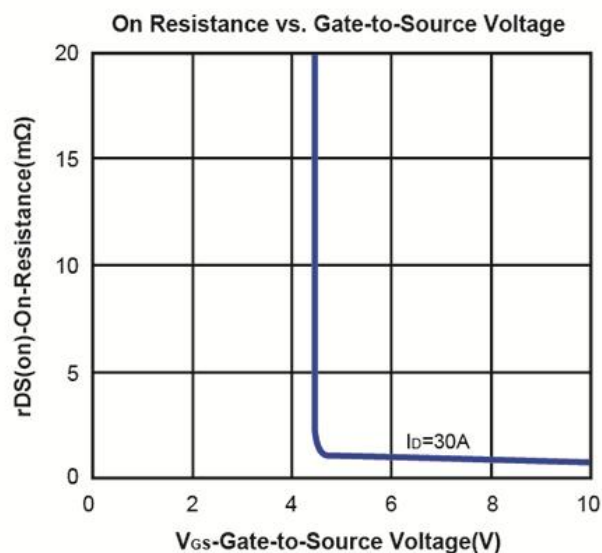
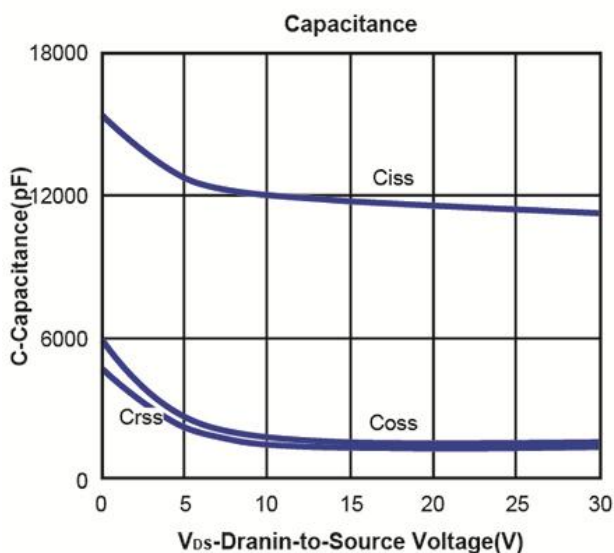
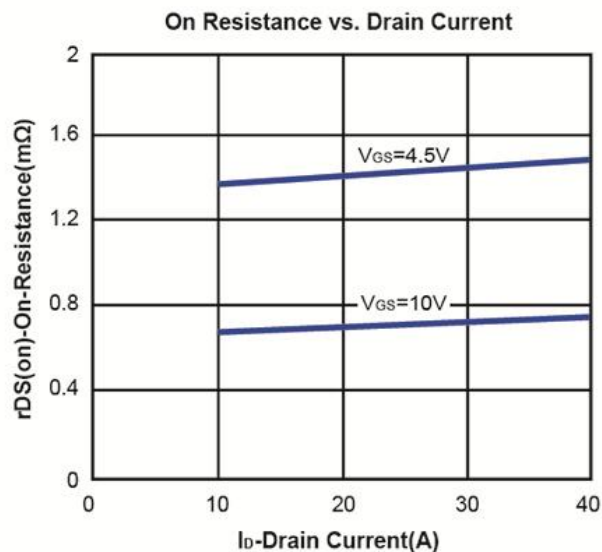
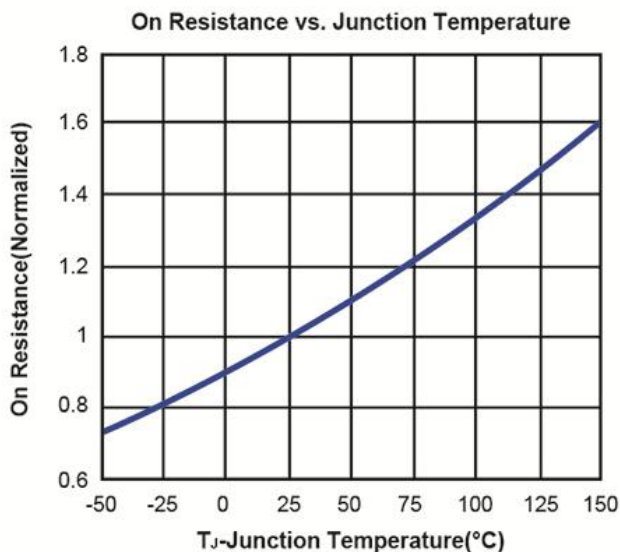
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1.2		2.2	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D =30A		0.72	0.87	mΩ
	Drain-Source On-State Resistance ^a	V _{GS} =4.5V, I _D =30A		1.45	1.89	
V _{SD}	Diode Forward Voltage	I _S =10A, V _{GS} =0V		0.73	1.1	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =30A		209		nC
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =30A		106		
Q _{gs}	Gate-Source Charge			40.1		
Q _{gd}	Gate-Drain Charge			51.1		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, F=1MHz		11727		pF
C _{oss}	Output Capacitance			1549		
C _{rss}	Reverse Transfer Capacitance			1457		
t _{d(on)}	Turn-On Delay Time	V _{DD} =15V, R _L =15Ω I _D =1A, V _{GEN} =4.5V R _G =3Ω		79.6		ns
t _r	Turn-On Rise Time			75.5		
t _{d(off)}	Turn-Off Delay Time			141		
t _f	Turn-Off Fall Time			68.6		

Note: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

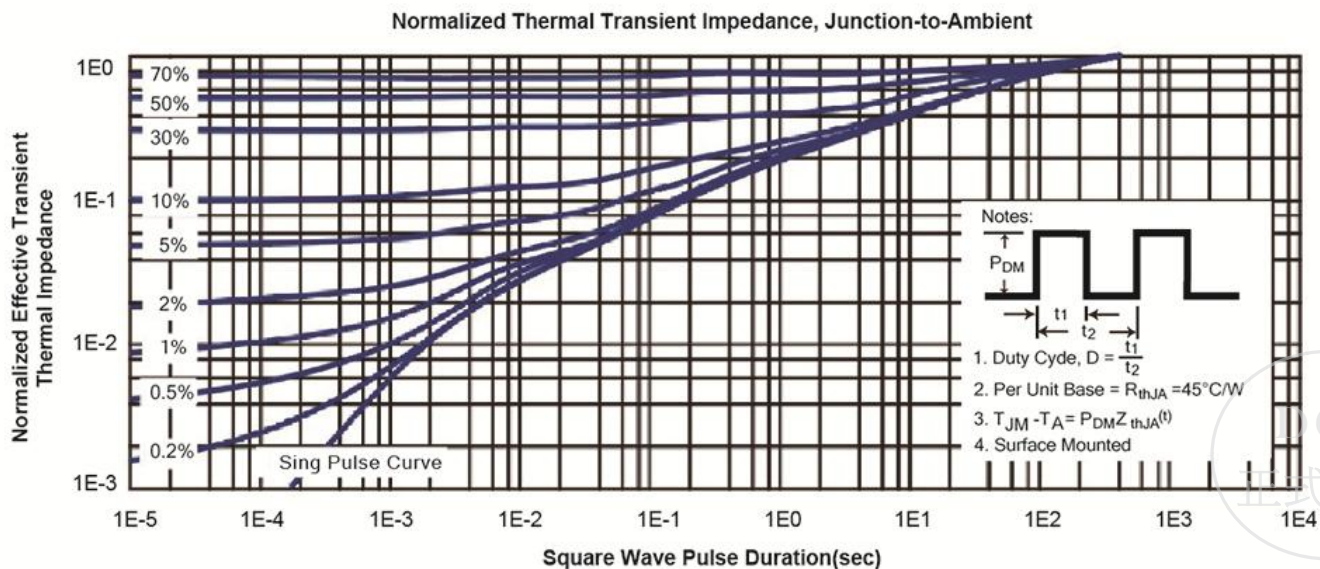
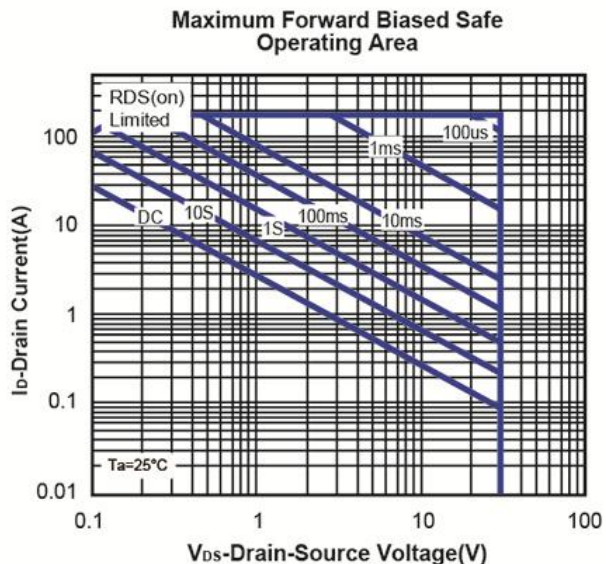
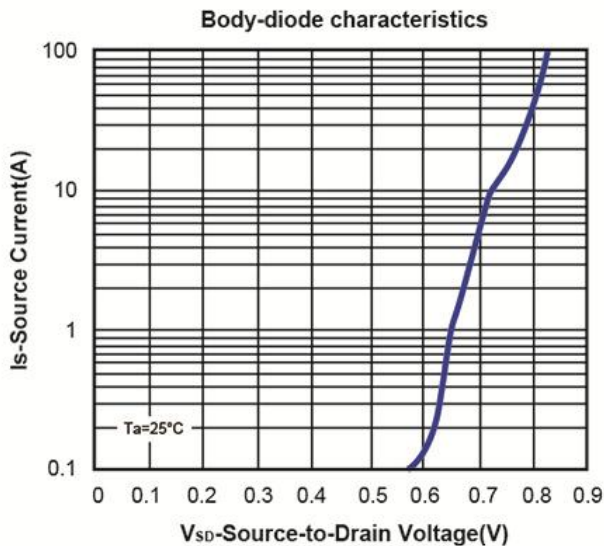
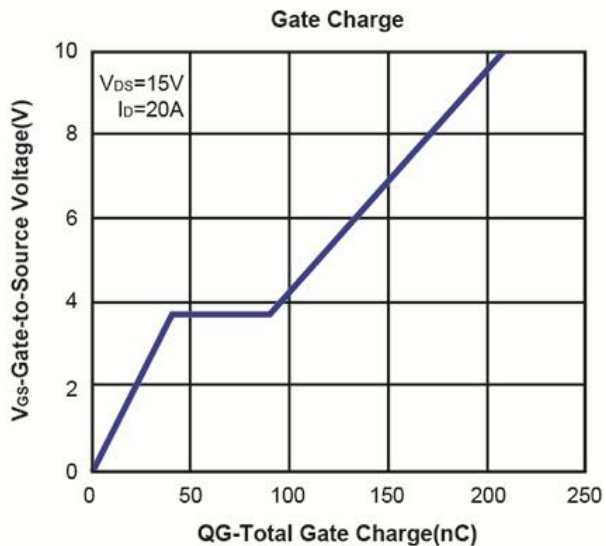
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N-Channel 30V(D-S) Enhancement MOSFET
Typical Characteristics (T_J =25°C Noted)

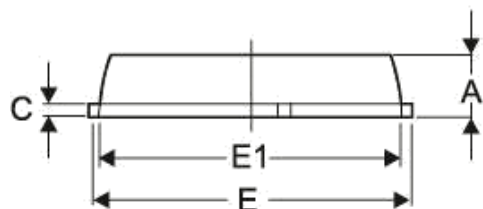
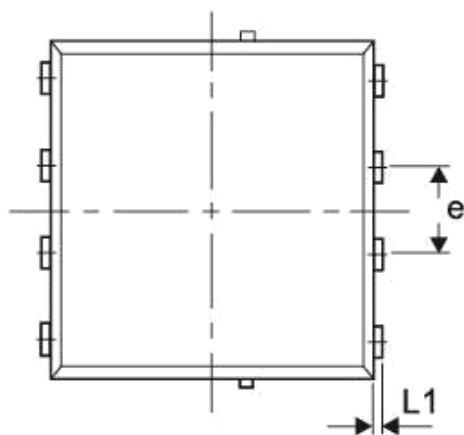
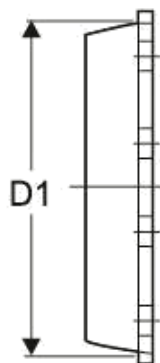
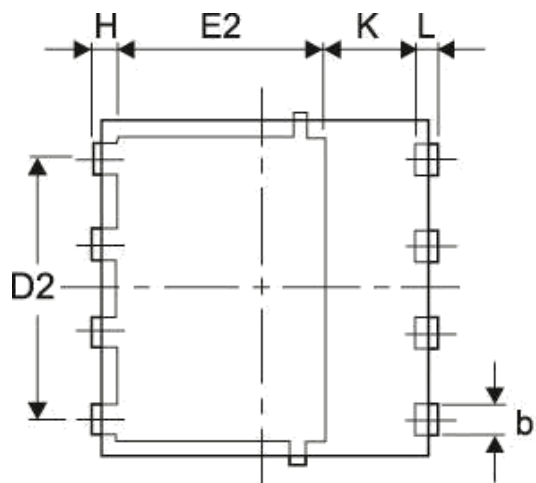


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Typical Characteristics (T_J =25°C Noted)



PowerDFN 5x6 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.25
b	0.33	0.51
C	0.155	0.30
D1	4.80	5.00
D2	3.61	3.96
E	5.8	6.20
E1	5.6	5.90
E2	3.35	4.31
e	1.27 BSC	
H	0.35	0.61
K	1.60	-
L	0.35	0.71
L1	0.05	0.20

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