

N-Channel 60V (D-S) MOSFET

GENERAL DESCRIPTION

The ME7692 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

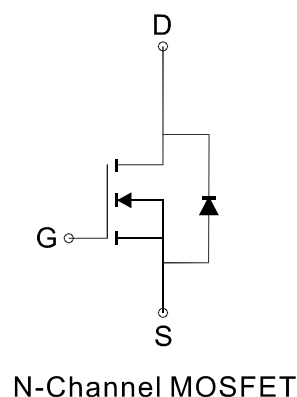
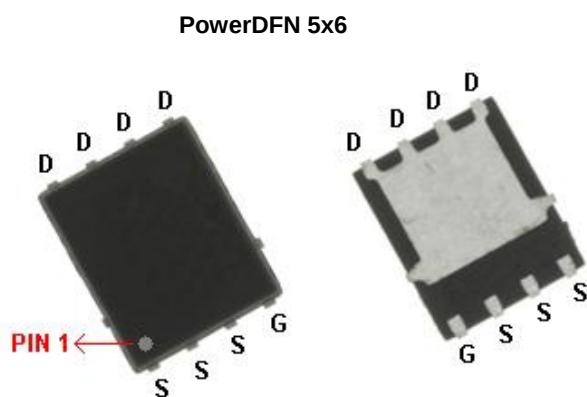
FEATURES

- $R_{DS(ON)} \leq 6m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 8.1m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter

PIN CONFIGURATION



Ordering Information: ME7692 (Pb-free)

ME7692-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current*	$T_A=25^\circ\text{C}$	I_D	17	A
	$T_A=70^\circ\text{C}$		13.6	
Pulsed Drain Current		I_{DM}	68	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.8	W
	$T_A=70^\circ\text{C}$		1.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	45	$^\circ\text{C/W}$

Note 1 : Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 80A.

Note 2 : The device mounted on 1in^2 FR4 board with 2 oz copper.

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Electrical Characteristics ($T_c = 25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60			V
V _{GS(th)}	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1		3	V
I _{GSS}	Gate-Body Leakage	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			1	μA
R _{DS(ON)}	Drain-Source On-Resistance*	$V_{GS}=10V, I_D=25A$		5.0	6	m Ω
		$V_{GS}=4.5V, I_D=25A$		6.1	8.1	
V _{SD}	Diode Forward Voltage*	$I_S=20A, V_{GS}=0V$		0.8	1.3	V
DYNAMIC						
Q _g	Total Gate Charge	$V_{DS}=30V, V_{GS}=10V, I_D=30A$		169		nC
Q _g	Total Gate Charge	$V_{DS}=30V, V_{GS}=4.5V, I_D=30A$		78.5		
Q _{gs}	Gate-Source Charge			35		
Q _{gd}	Gate-Drain Charge			38.5		
C _{iss}	Input Capacitance	$V_{DS}=30V, V_{GS}=0V, f=1MHz$		8861		pF
C _{oss}	Output Capacitance			325		
C _{rss}	Reverse Transfer Capacitance			285		
t _{d(on)}	Turn-On Delay Time	$V_{DS}=30V, I_D=1A,$ $V_{GS}=10V, R_G=6\Omega,$ $R_L=30\Omega$		46.1		ns
t _r	Turn-On Rise Time			33.6		
t _{d(off)}	Turn-Off Delay Time			204		
t _f	Turn-Off Fall Time			55.7		

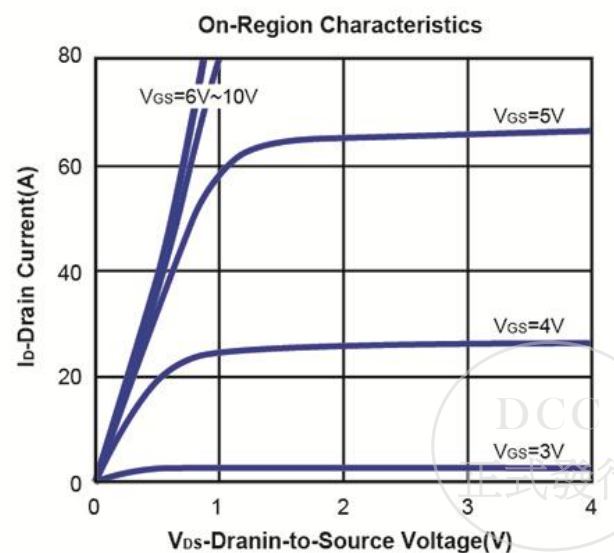
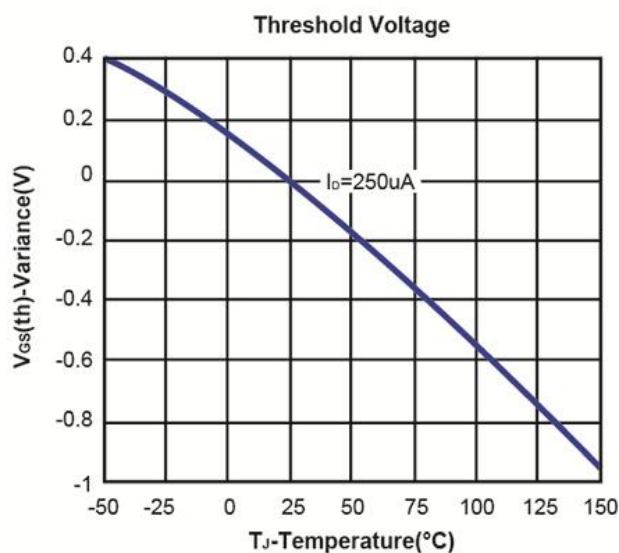
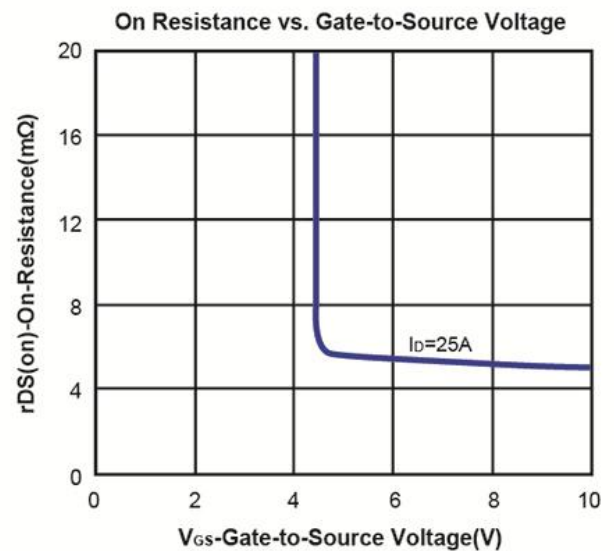
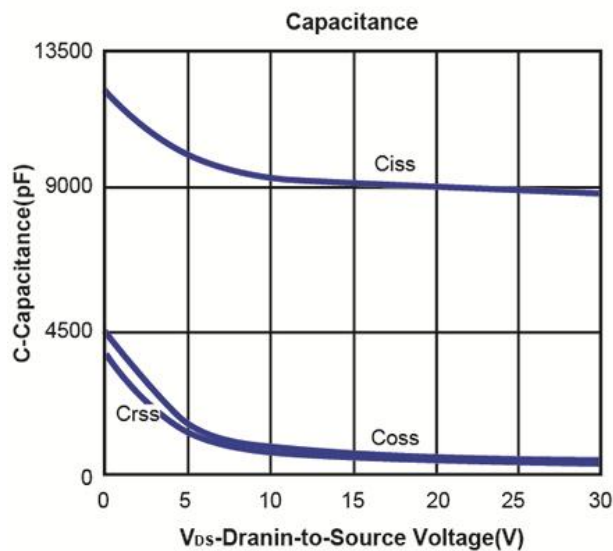
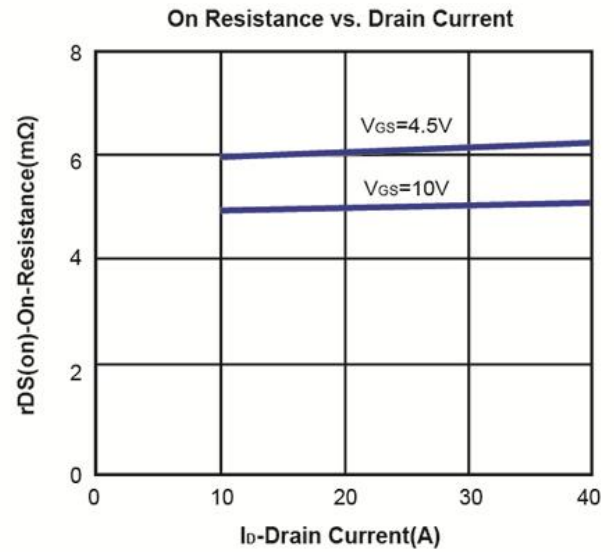
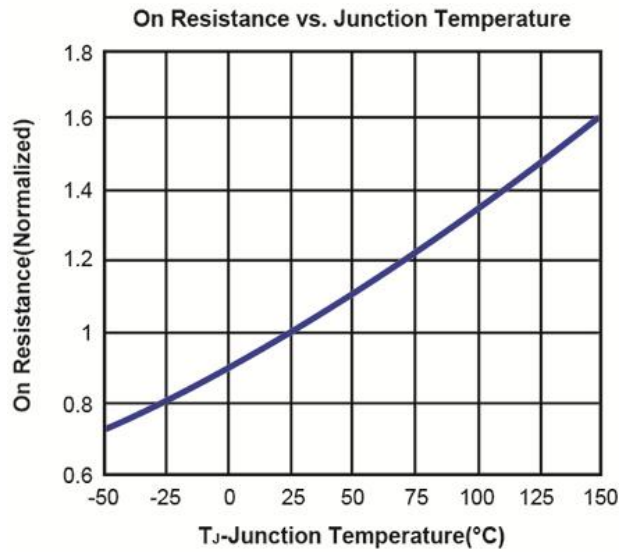
 Notes: a, pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$, Guaranteed by design, not subject to production testing.

b, Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



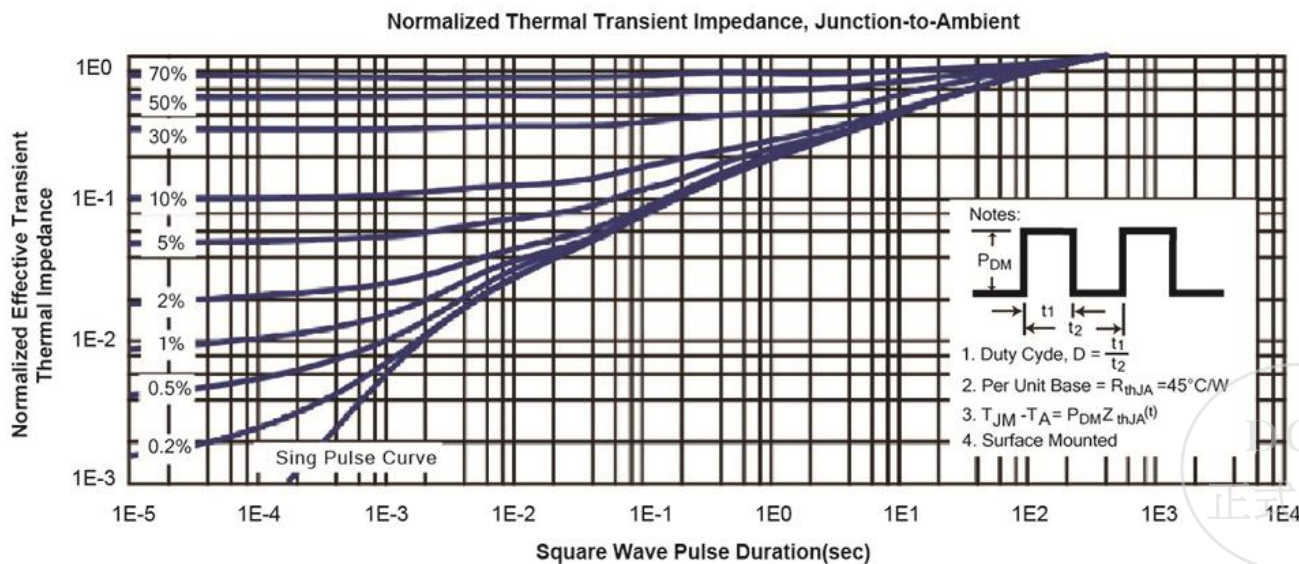
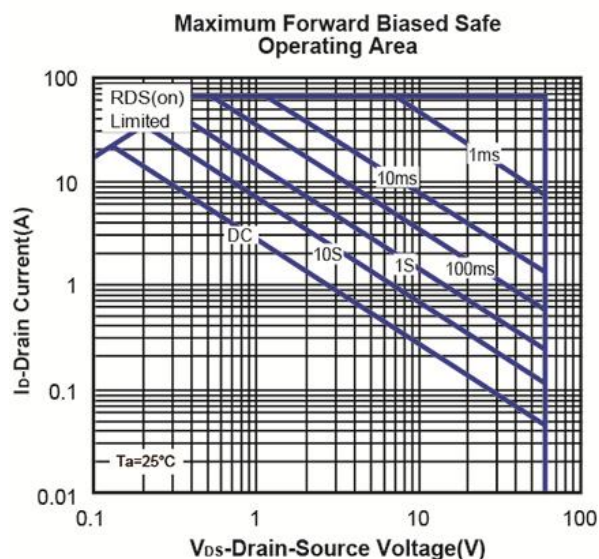
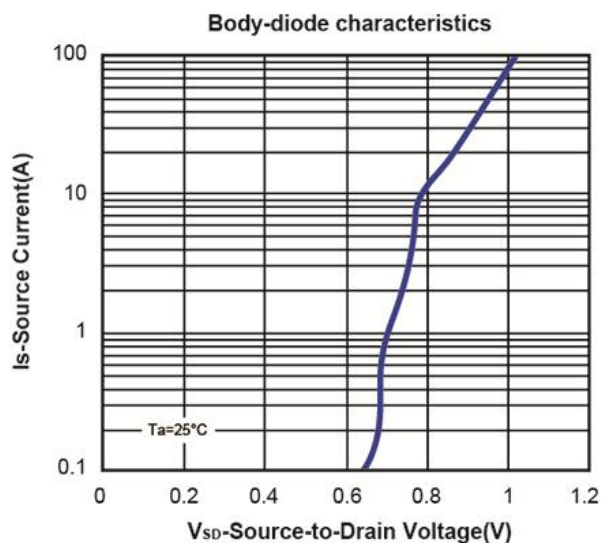
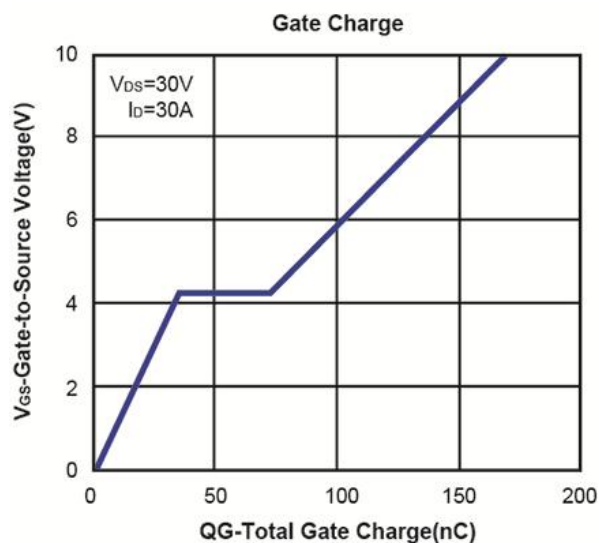
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Typical Characteristics (T_J =25°C Noted)

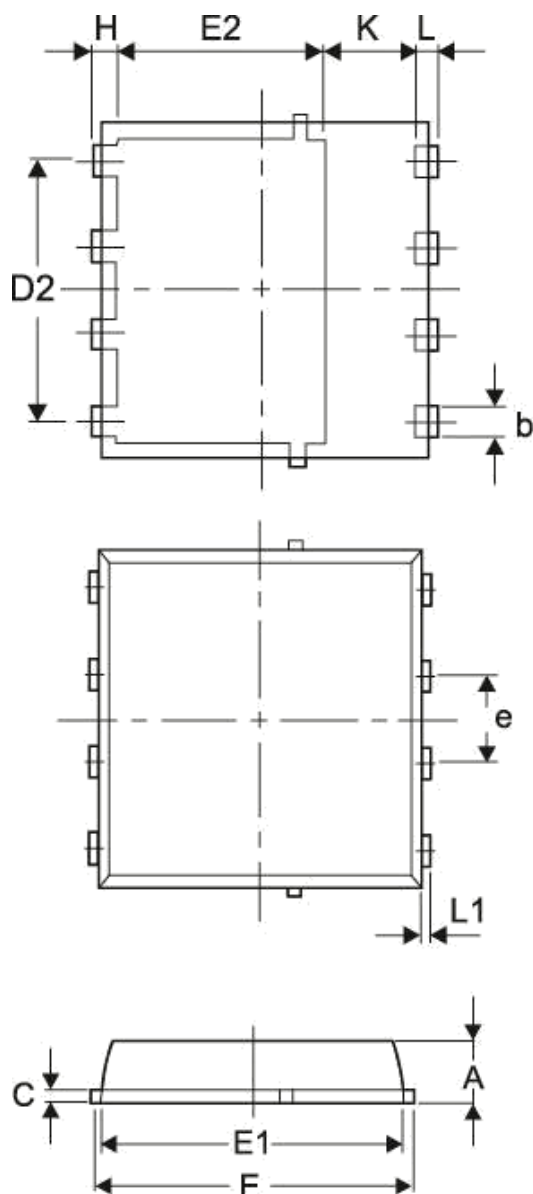


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DFN5X6 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.25
b	0.33	0.51
C	0.155	0.30
D1	4.80	5.00
D2	3.61	3.96
E	5.8	6.20
E1	5.6	5.90
E2	3.35	4.31
e	1.27 BSC	
H	0.35	0.61
K	1.60	-
L	0.35	0.71
L1	0.05	0.20

