N-Channel 30V (D-S) MOSFET, ESD Protected

GENERAL DESCRIPTION

The ME7804-G N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦16mΩ@V_{GS}=10V
- $R_{DS(ON)}$ ≦25mΩ@ V_{GS}=4.5V

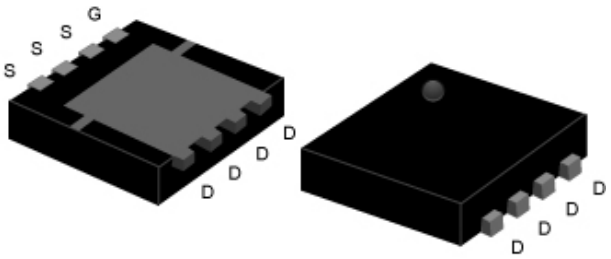
APPLICATIONS

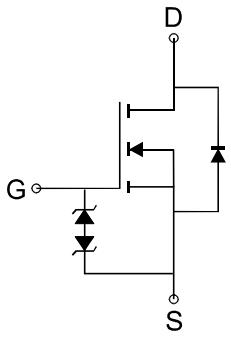
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC
- ESD Protected

PIN CONFIGURATION

(DFN 3.3x3.3)

Top View





Ordering Information: ME7804S-G (Green product-Halogen free)

Absolute Maximum Ratings (T_j=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	12.2	A
	T_A=70℃		9.7	
Pulsed Drain Current		I_{DM}	50	A
Maximum Power Dissipation	T_A=25℃	P_D	3.8	W
	T_A=70℃		2.4	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	33	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±16V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=10V, I_D= 10A		13	16	mΩ
		V_{GS}=4.5V, I_D= 5A		19	25	
V_{SD}	Diode Forward Voltage	I_S=9A, V_{GS}=0V		0.8		V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=10A		18		nC
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=10A		8.8		
Qgs	Gate-Source Charge			4.2		
Qgd	Gate-Drain Charge			3.7		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V,f=1MHz		729		pF
Coss	Output Capacitance			94		
Crss	Reverse Transfer Capacitance			29		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V,f=1MHz		0.9		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=25V, R_L =25Ω R_{GEN}=6Ω, V_{GS}=10V		14		ns
t_r	Turn-On Rise Time			9.5		
$t_{d(off)}$	Turn-Off Delay Time			44		
t_f	Turn-Off Fall Time			5.7		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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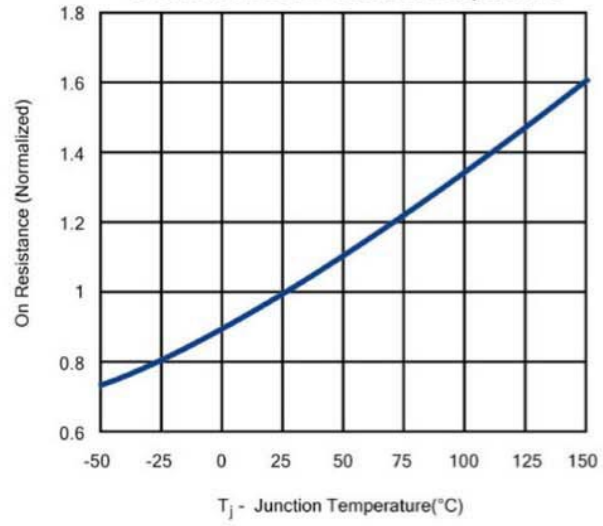
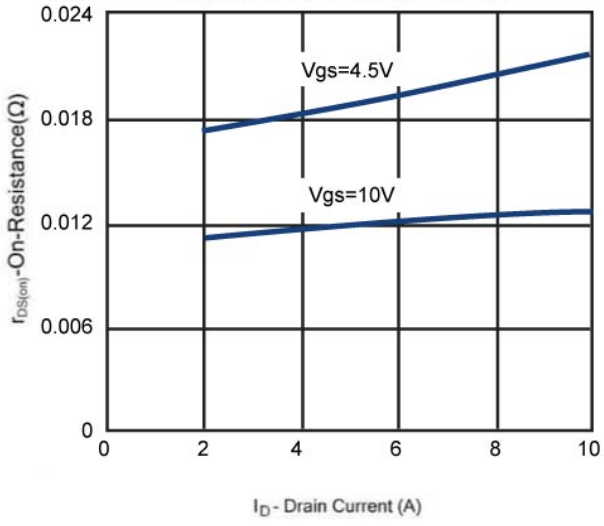
Typical Characteristics (T_J =25℃ Noted)

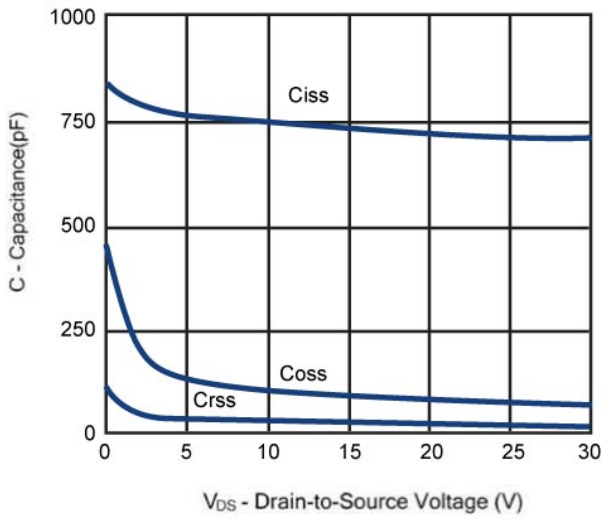
On Resistance vs. Junction Temperature



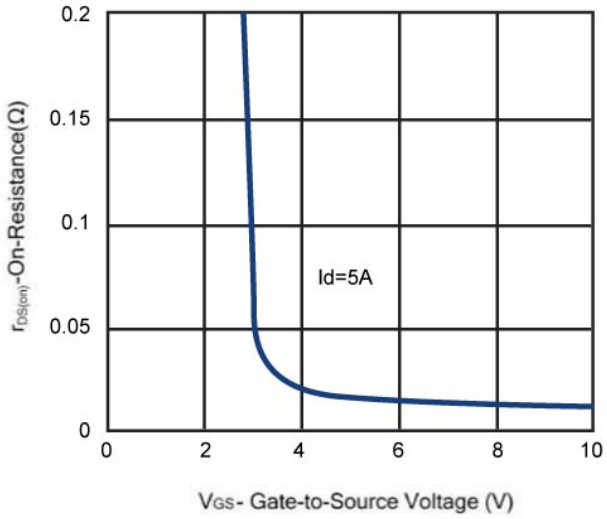
On-Resistance vs. Drain Current



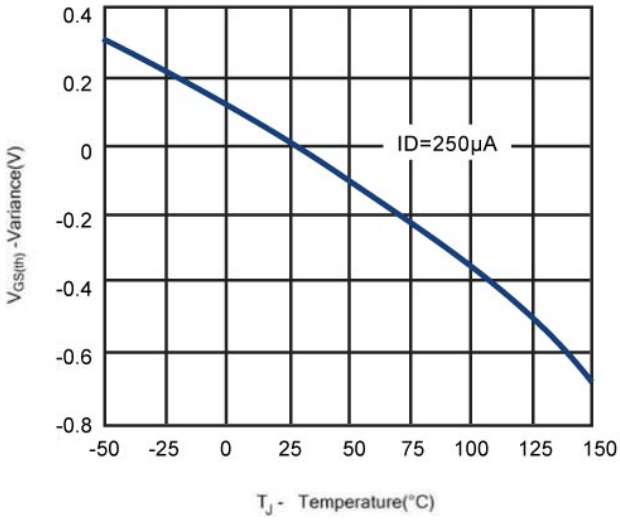
Capacitance



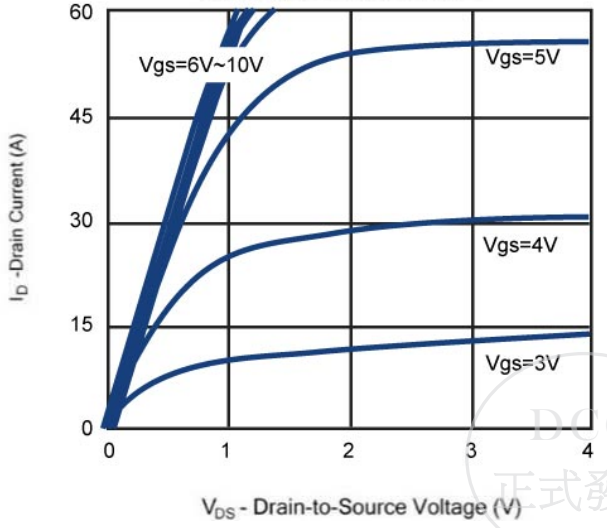
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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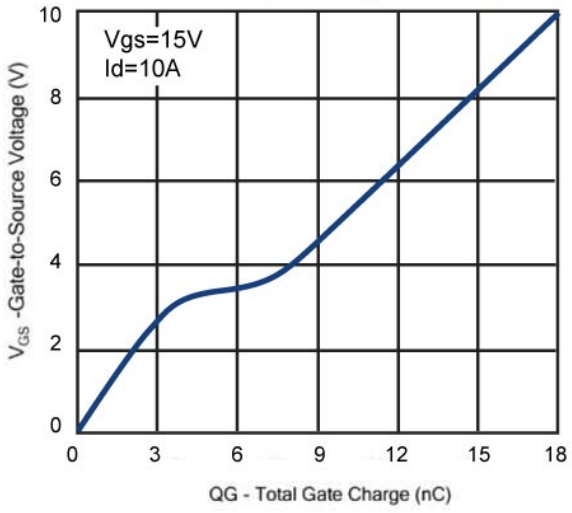
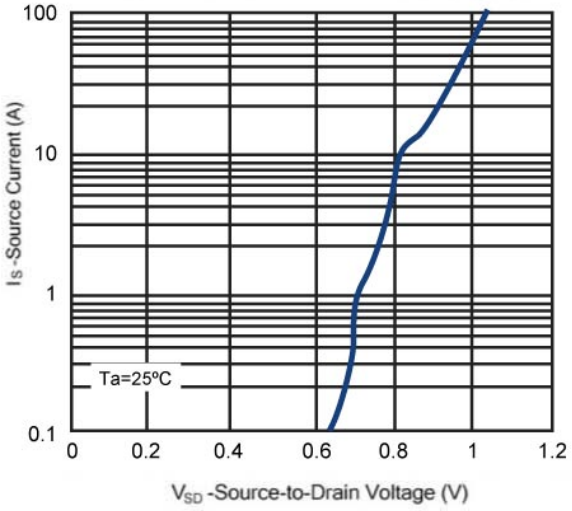
Typical Characteristics (T_J =25℃ Noted)

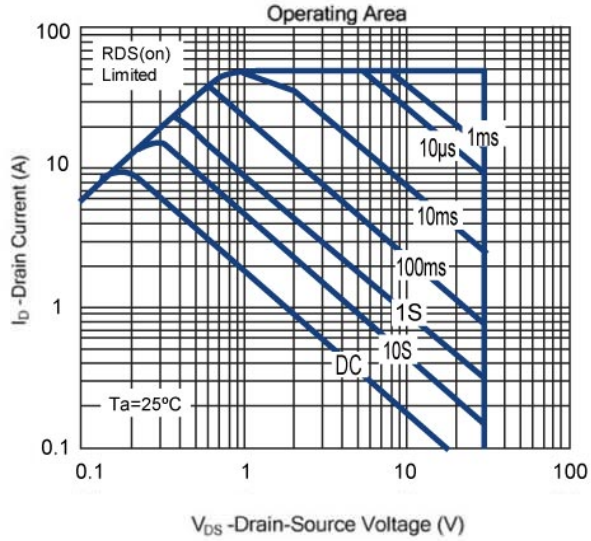
Gate Charge



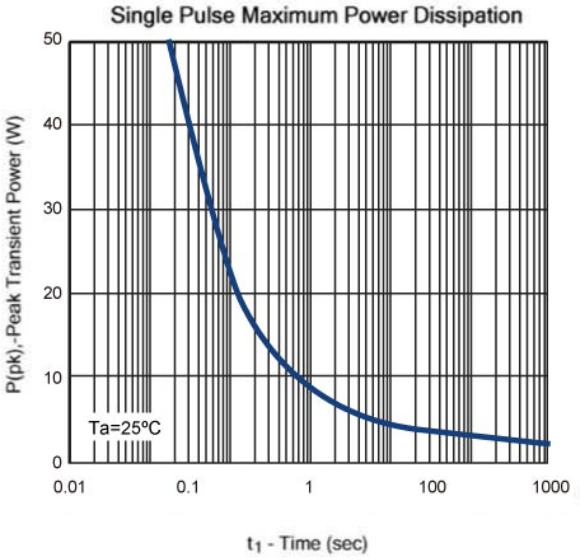
Source to Drain Diode Forward Voltage



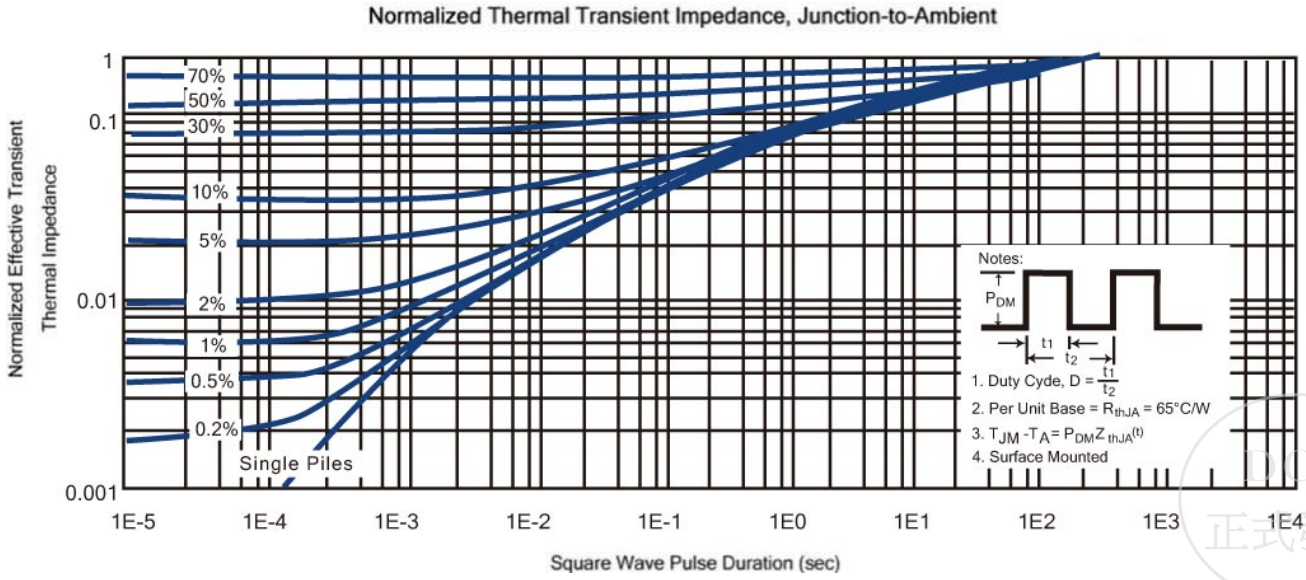
Maximum Forward Biased Safe Operating Area



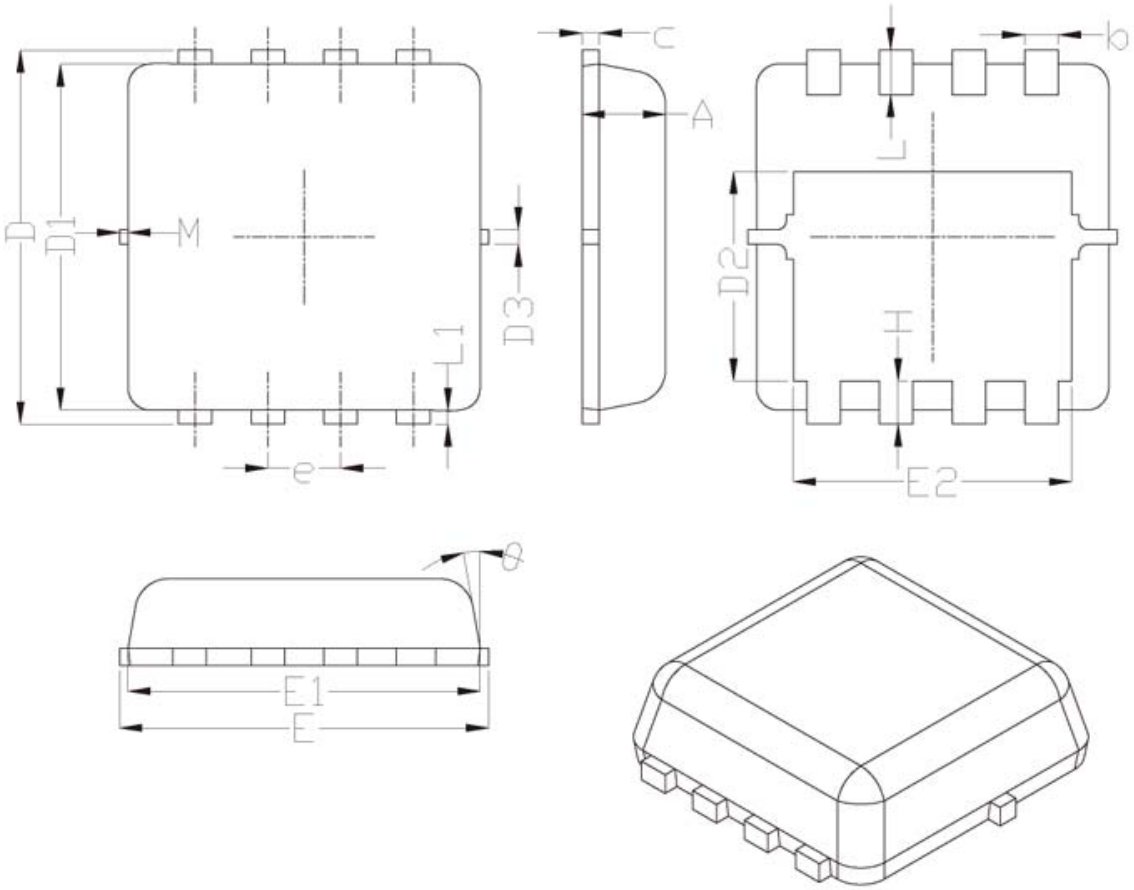
Single Pulse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



DFN(S) 3.3x3.3 Package Outline



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e		0.65BSC	
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			