

N-Channel 30-V (D-S) MOSFET Integrated Schottky Diode

GENERAL DESCRIPTION

The ME7812S N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

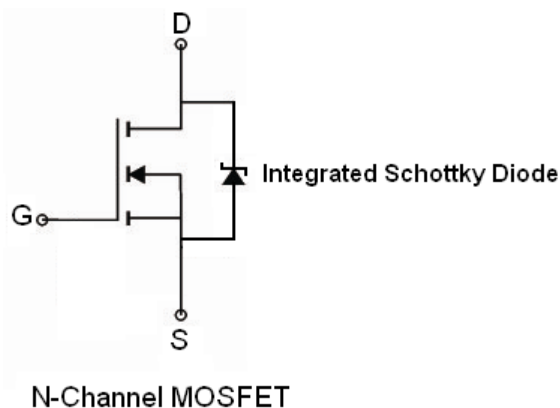
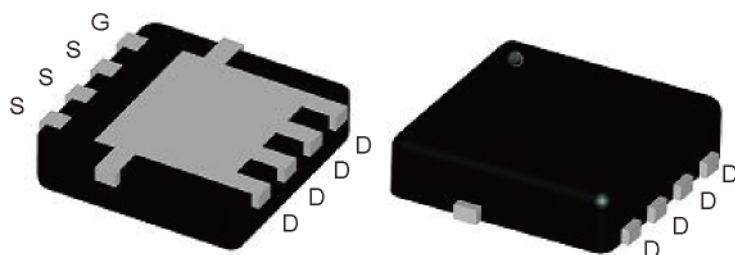
- $R_{DS(ON)} \leq 8.5m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 17.5m\Omega @ V_{GS}=4.5V$

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

(DFN 3.3x3.3)
Top View



Ordering Information: ME7812S-G (Green product-Halogen free)

Absolute Maximum Ratings (T_j=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current	I _D	T _A =25°C	15.2
		T _A =70°C	12.1
Pulsed Drain Current	I _{DM}	61	A
Maximum Power Dissipation	P _D	T _A =25°C	3.1
		T _A =70°C	2.0
Operating Junction Temperature	T _J	-55 to 150	°C
Thermal Resistance-Junction to Ambient*	R _{θJA}	40	°C/W

*The device mounted on 1in² FR4 board with 2 oz copper



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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} =0V			100	μA
R _{DS(ON)}	Drain-Source On-State Resistance ^a	V _{GS} =10V, I _D = 13.5A		7	8.5	mΩ
		V _{GS} =4.5V, I _D = 11A		13.5	17.5	
V _{SD}	Diode Forward Voltage	I _S =1.0A, V _{GS} =0V		0.45	0.55	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _D =13.5A		28		nC
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _D =13.5A		14		
Q _{gs}	Gate-Source Charge			6.5		
Q _{gd}	Gate-Drain Charge			7.5		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		1260		pF
C _{oss}	Output Capacitance			527		
C _{rss}	Reverse Transfer Capacitance			121		
t _{d(on)}	Turn-On Delay Time	V _{DS} =15V, R _L =15Ω R _{GEN} =3Ω, V _{GS} =10V		17		ns
t _r	Turn-On Rise Time			14		
t _{d(off)}	Turn-Off Delay Time			47		
t _f	Turn-Off Fall Time			6		

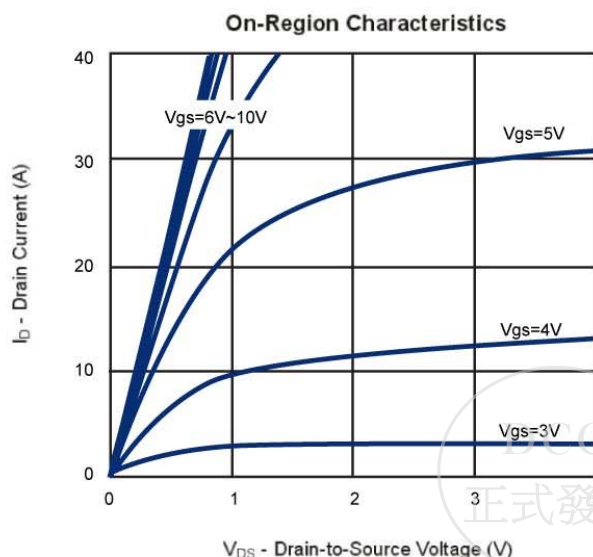
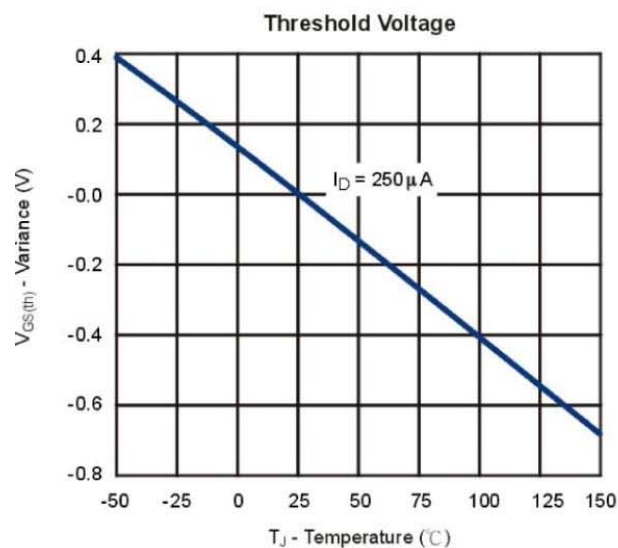
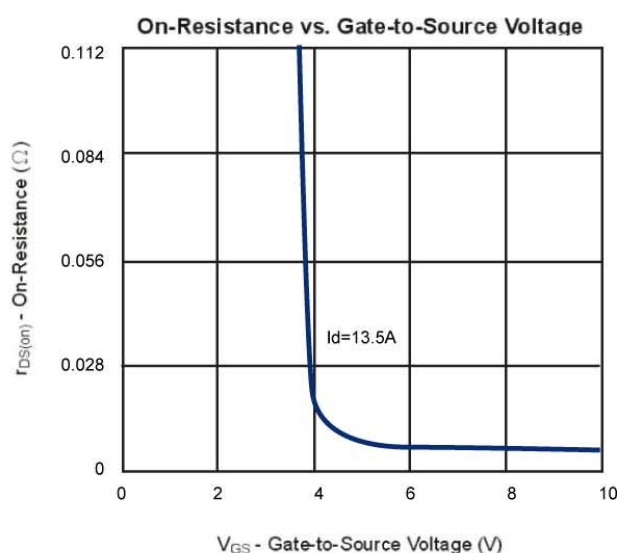
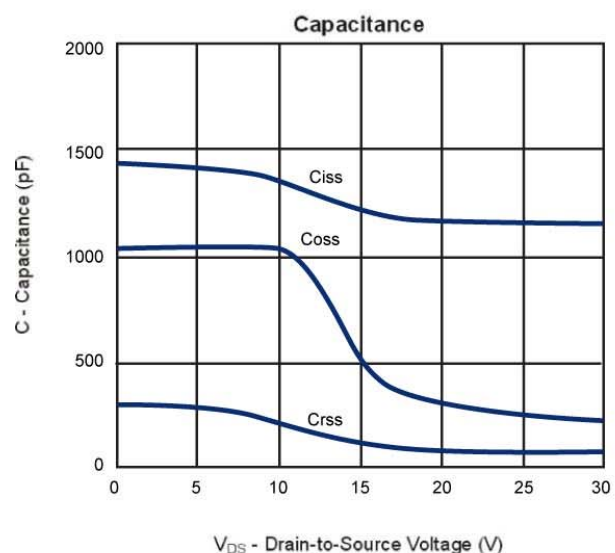
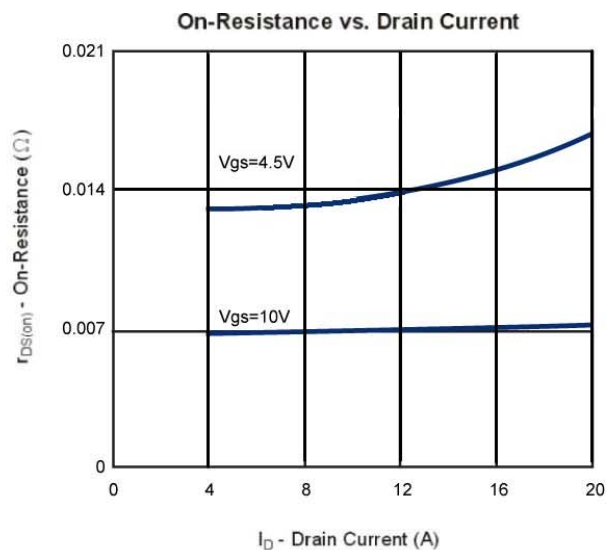
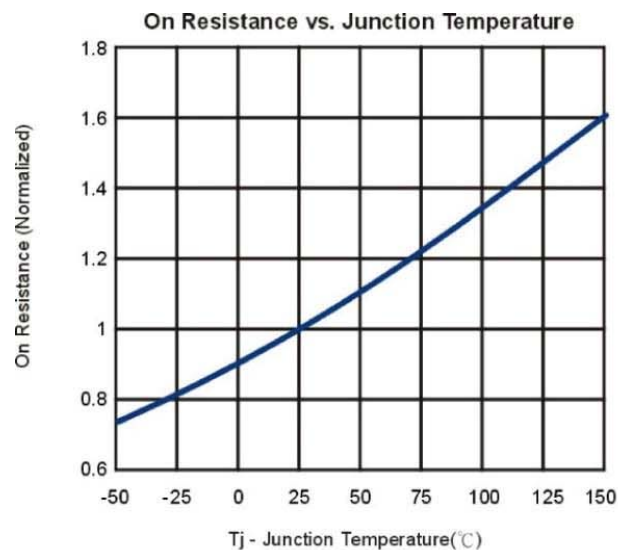
Note: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



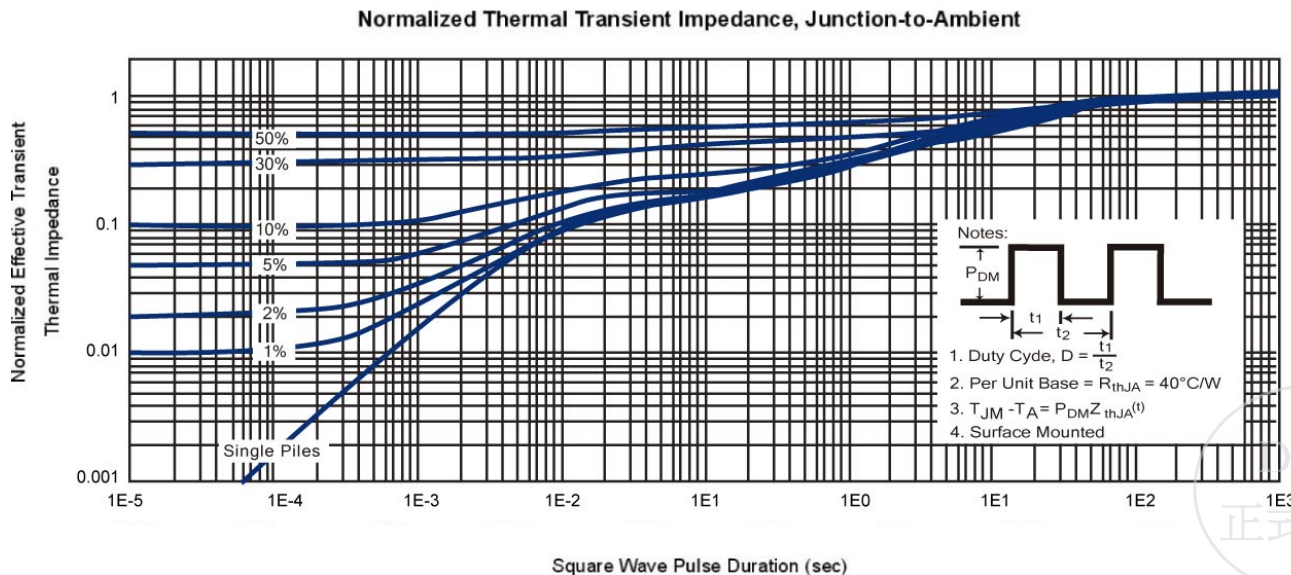
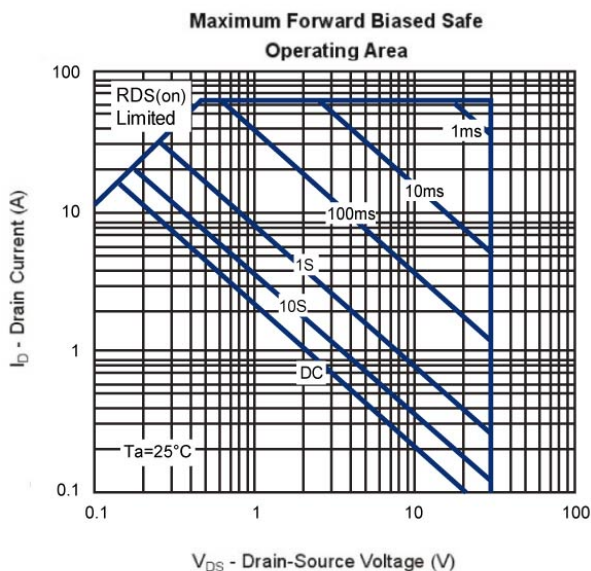
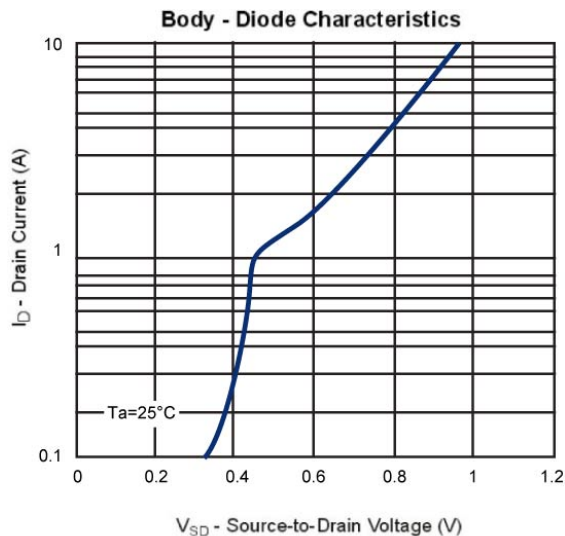
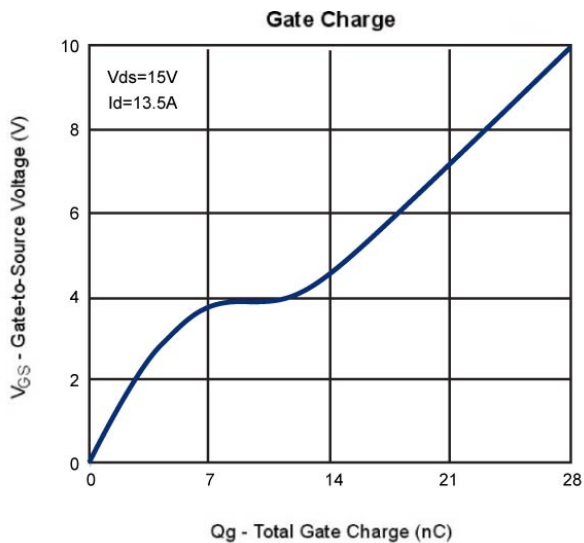
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Typical Characteristics (T_J = 25°C Noted)

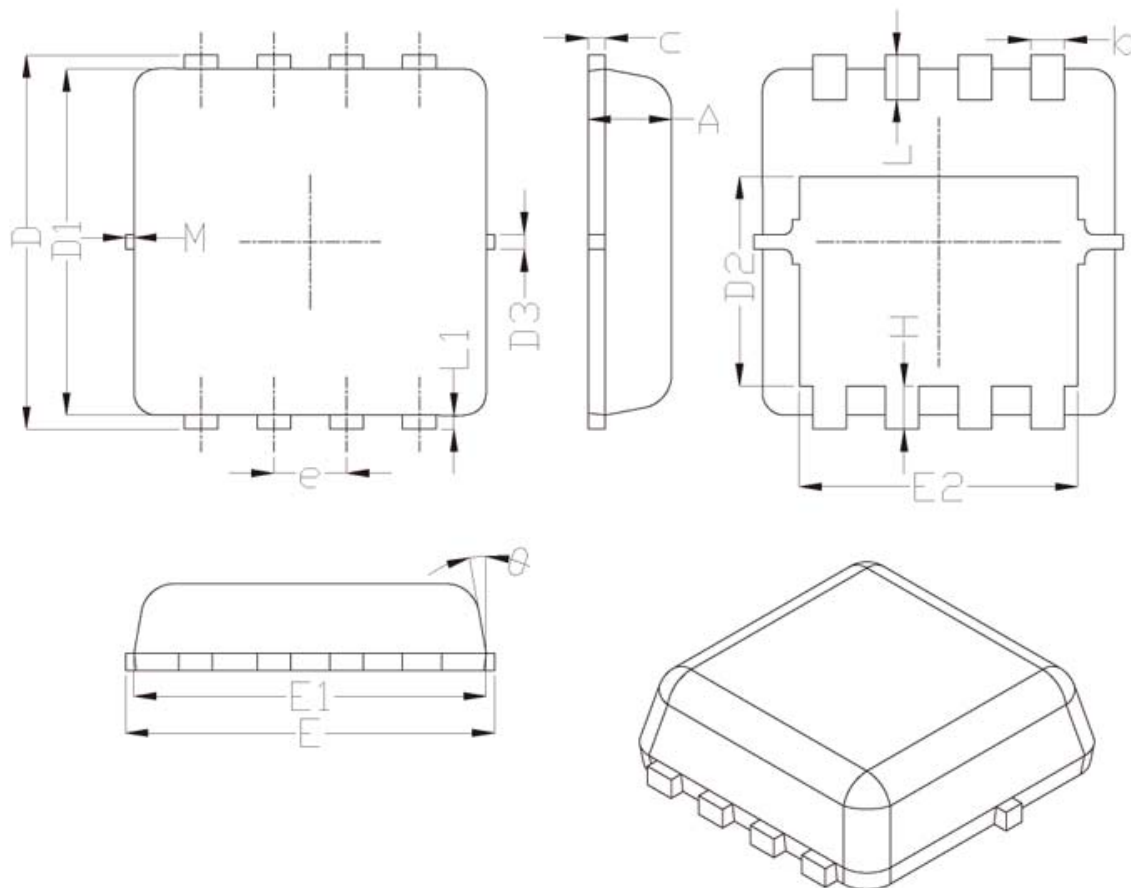


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DFN(S) 3.3x3.3 Package Outline



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
theta	---	10°	12°
M	*	*	0.15

* Not specified

