N-Channel 30V (D-S) MOSFET

GENERAL DESCRIPTION

The ME7814S-G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 3.6m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 5.1m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

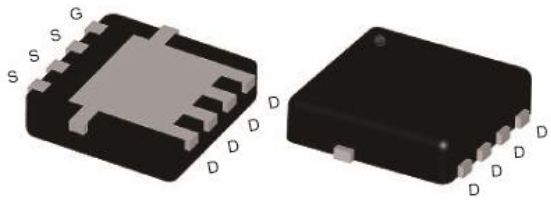
APPLICATIONS

- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

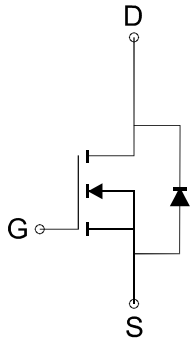
(DFN(S) 3.3x3.3)

Top View



Ordering Information: ME7814S (Pb-free)

ME7814S-G (Green product-Halogen free)



N-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	T_A=25℃	I_D	25.6	A
	T_A=70℃		20.5	
Pulsed Drain Current		I_{DM}	102	A
Maximum Power Dissipation*	T_A=25℃	P_D	3.7	W
	T_A=70℃		2.4	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	33	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.3		2.2	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D=30A		2.9	3.6	mΩ
		V_{GS}=4.5V, I_D=30A		4.1	5.1	
V_{SD}	Diode Forward Voltage	I_S=10A, V_{GS}=0V		0.77	1.1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=30A		74		nC
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=30A		35.6		
Qgs	Gate-Source Charge			15.1		
Qgd	Gate-Drain Charge			17.5		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, F=1MHz		3906		pF
Coss	Output Capacitance			434		
Crss	Reverse Transfer Capacitance			374		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L=15Ω V_{GEN}=10V, R_G=3Ω		22.4		ns
tr	Turn-On Rise Time			19.1		
$t_{d(off)}$	Turn-Off Delay Time			81.3		
t_f	Turn-Off Fall Time			13.7		

Note: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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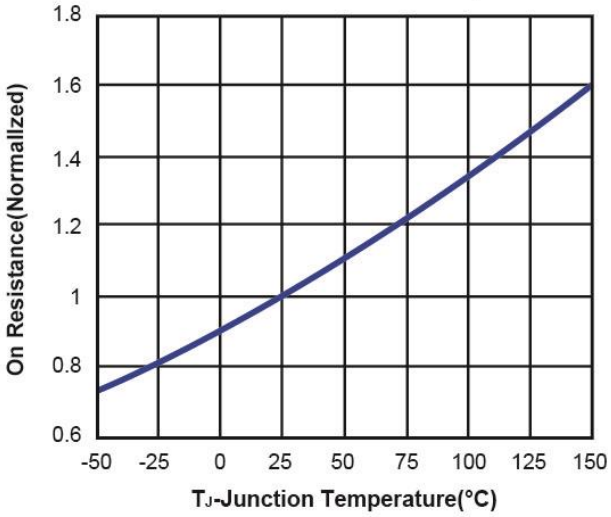
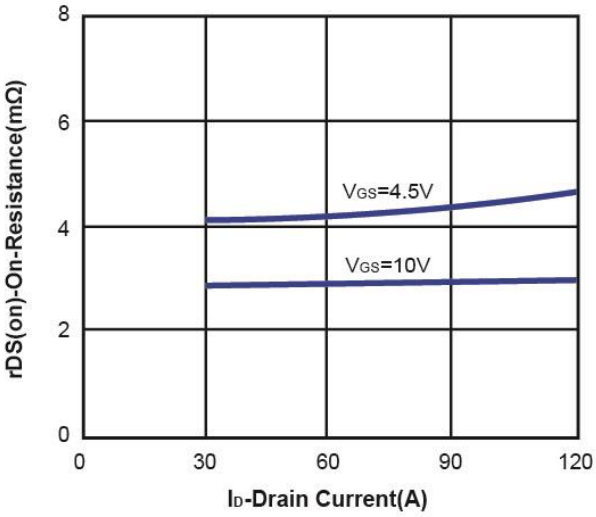
Typical Characteristics (T_J =25℃ Noted)

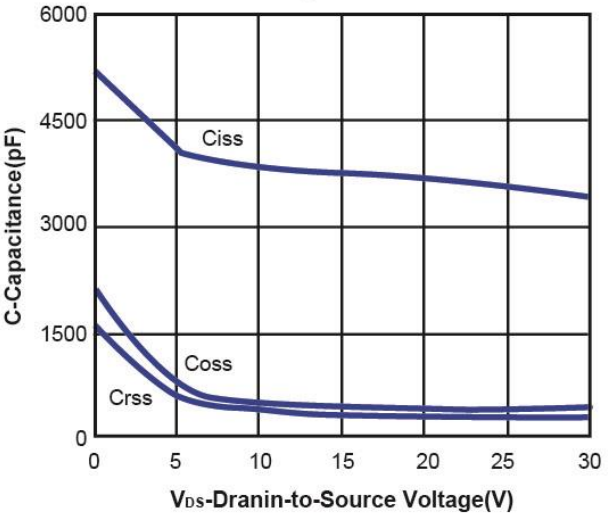
On Resistance vs. Junction Temperature



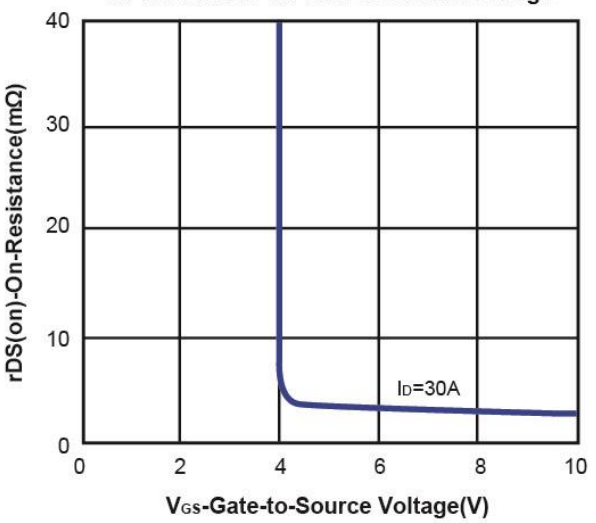
On Resistance vs. Drain Current



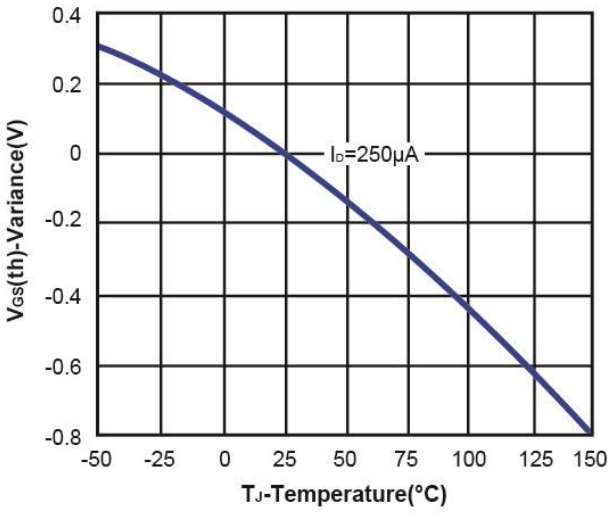
Capacitance



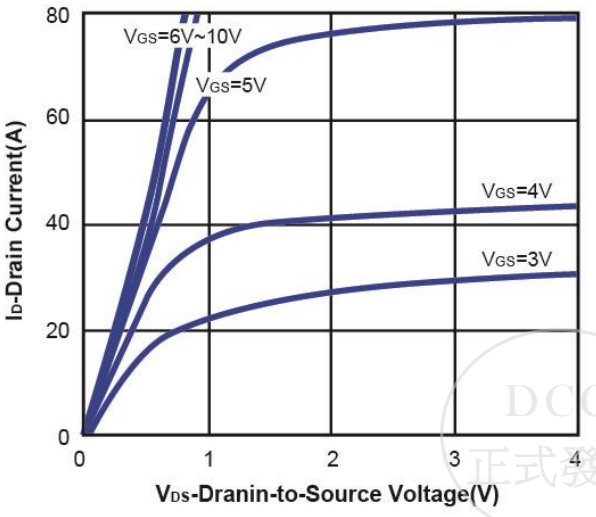
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



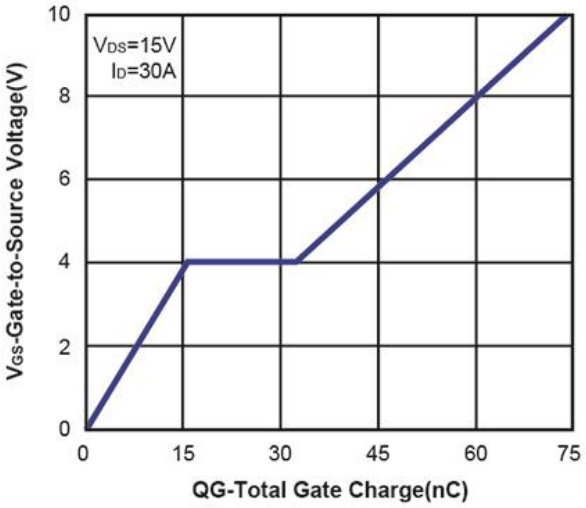
On-Region Characteristics



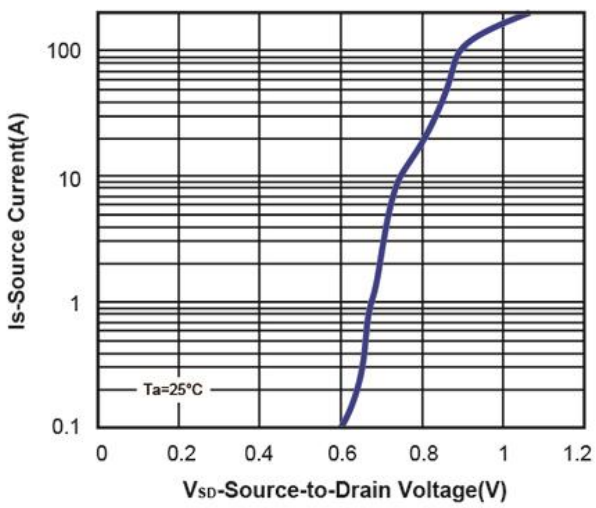
N-Channel 30V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

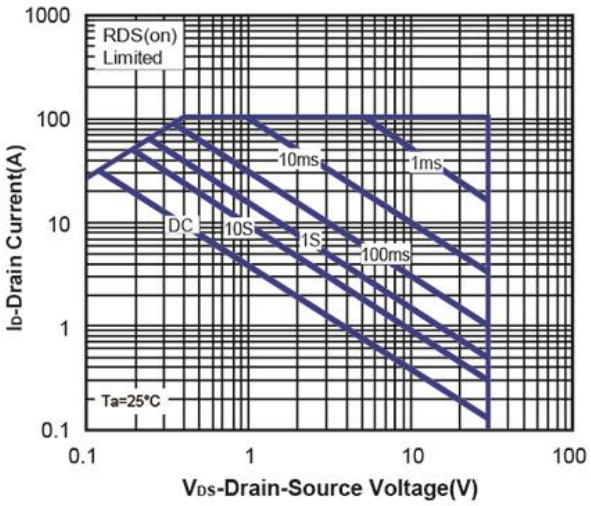
Gate Charge



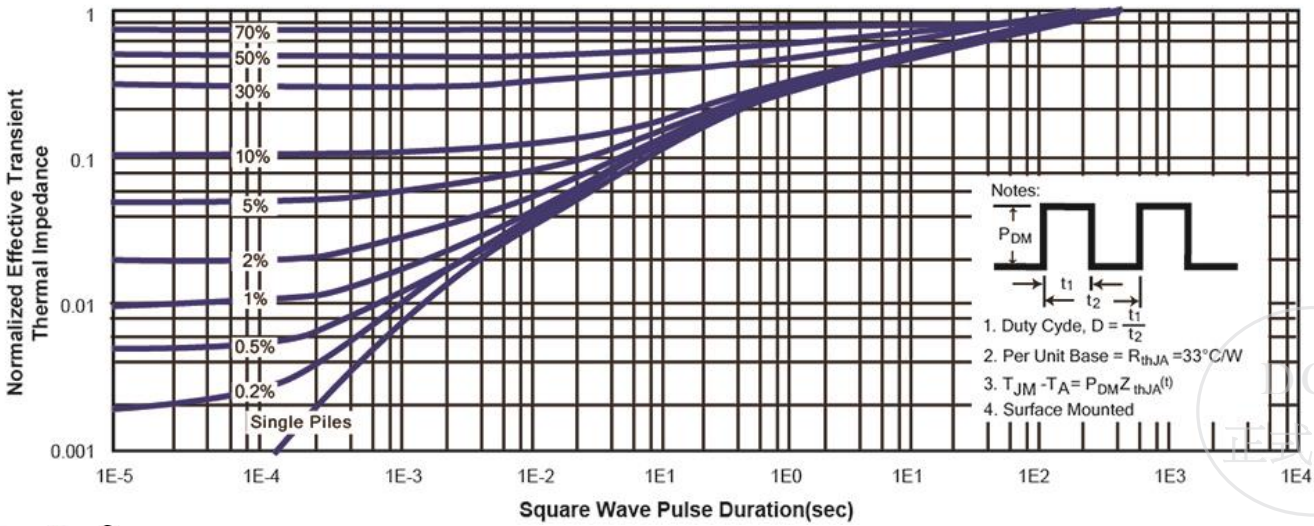
Body-diode characteristics



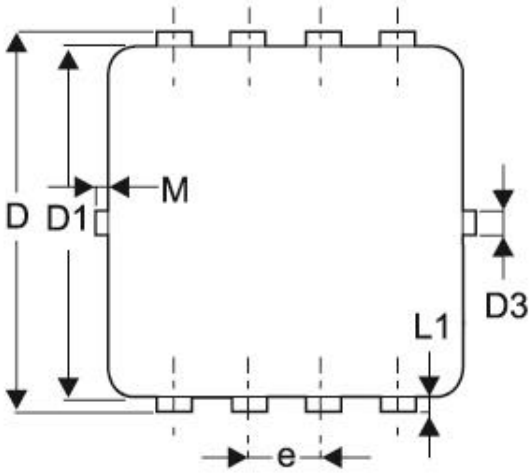
Maximum Forward Biased Safe Operating Area

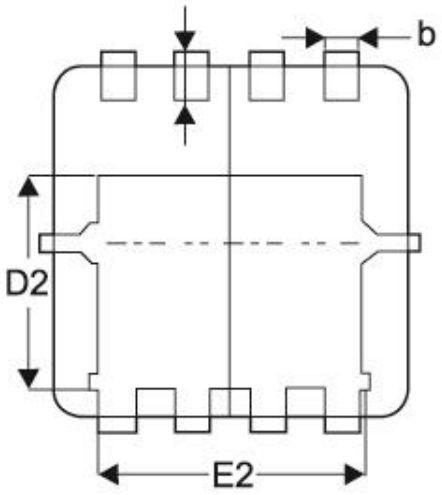


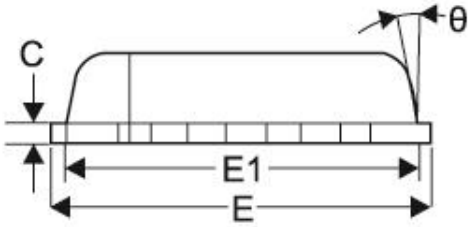
Normalized Thermal Transient Impedance, Junction-to-Ambient



DFN(S) 3.3x3.3 Package Outline







Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	0.70	0.80
b	0.25	0.35
c	0.10	0.25
D	3.25	3.45
D1	3.00	3.20
D2	1.48	1.68
D3	0.13TYP	
E	3.20	3.40
E1	3.00	3.20
E2	2.39	2.59
e	0.65 BSC	
H	0.30	0.50
L	0.30	0.50
L1	0.13REF	
θ	--	12°
M	--	0.15