P-Channel Enhancement Mode Mosfet

GENERAL DESCRIPTION

The ME7835 P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

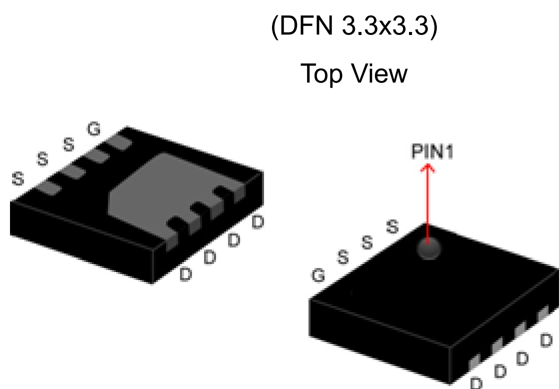
FEATURES

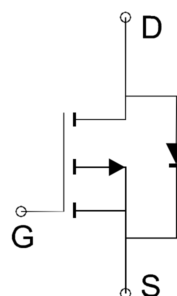
- RDS(ON) ≦18mΩ@VGS=-10V
- RDS(ON) ≦36mΩ@VGS=-4.5V

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION





Ordering Information: ME7835 (Pb-free)

ME7835-G (Green product-Halogen free)

Absolute Maximum Ratings (Tj=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±25	V
Continuous Drain Current	T_A=25℃	I_D	-11.5	A
	T_A=70℃		-9.2	
Pulsed Drain Current		I_{DM}	-46	A
Maximum Power Dissipation	T_A=25℃	P_D	3.8	W
	T_A=70℃		2.4	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	33	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250 μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250 μA	-1		-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=-10V, I_D= -8.5A		15	18	mΩ
		V_{GS}=-4.5V, I_D= -6.3A		27	36	
V_{SD}	Diode Forward Voltage	I_S=-8.5A, V_{GS}=0V		0.85	1.2	V
DYNAMIC						
Qg	Total Gate Charge (-10V)	V_{DS}=-15V,V_{GS}=-10V, I_D=-8.5A		28		nC
Qg	Total Gate Charge (-4.5)			14		
Qgs	Gate-Source Charge			6		
Qgd	Gate-Drain Charge			6.5		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V,f=1MHz		1180		pF
Coss	Output Capacitance			223		
Crss	Reverse Transfer Capacitance			73		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-15V, R_L =15Ω R_{GEN}=6Ω, V_{GS}=-10V		39		ns
t_r	Turn-On Rise Time			16		
$t_{d(off)}$	Turn-Off Delay Time			78		
t_f	Turn-Off Fall Time			19		

Note: a.Pulse test: pulse width≦300us, duty cycle≦2%

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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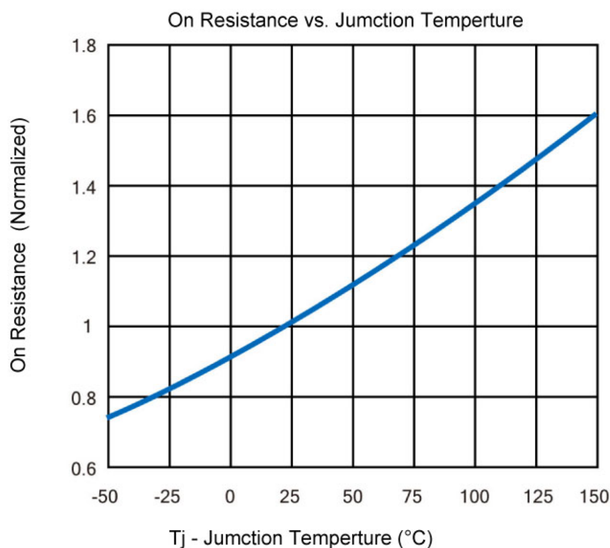
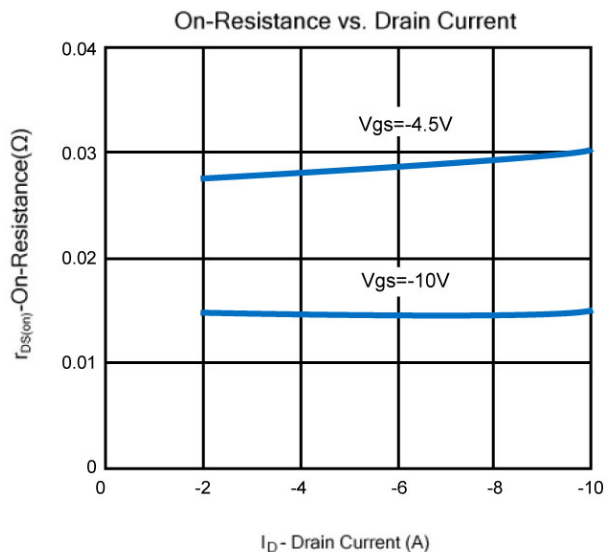
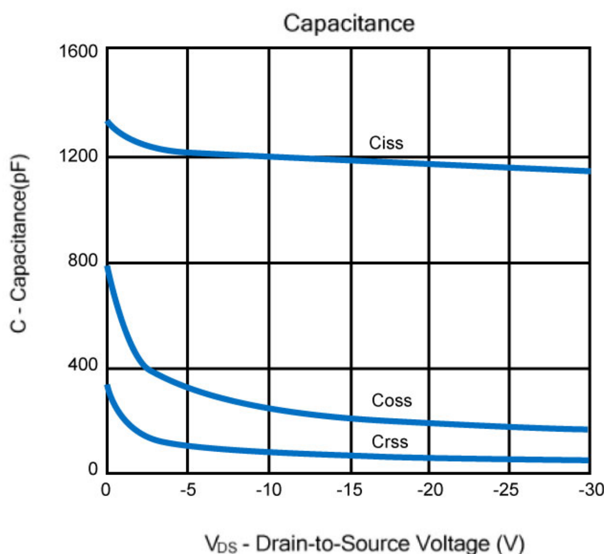
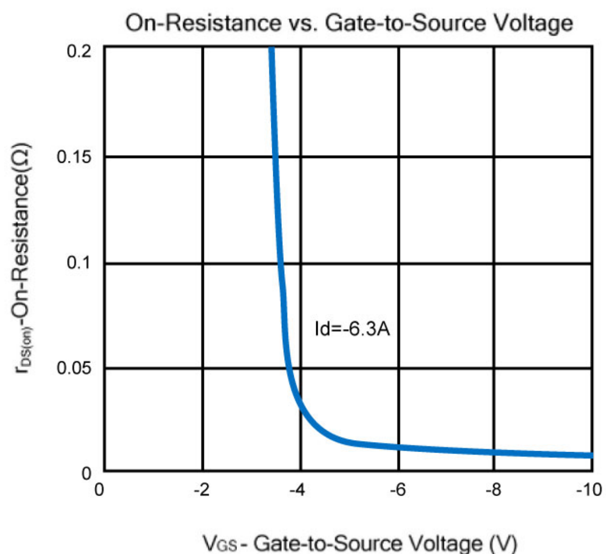
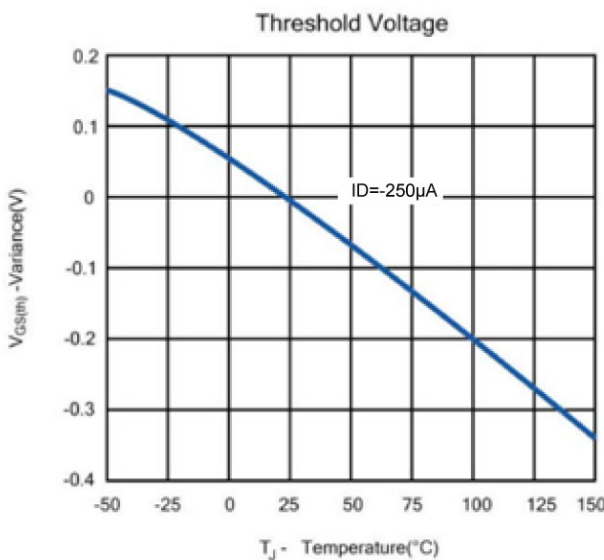
Typical Characteristics (T_J =25℃ Noted)

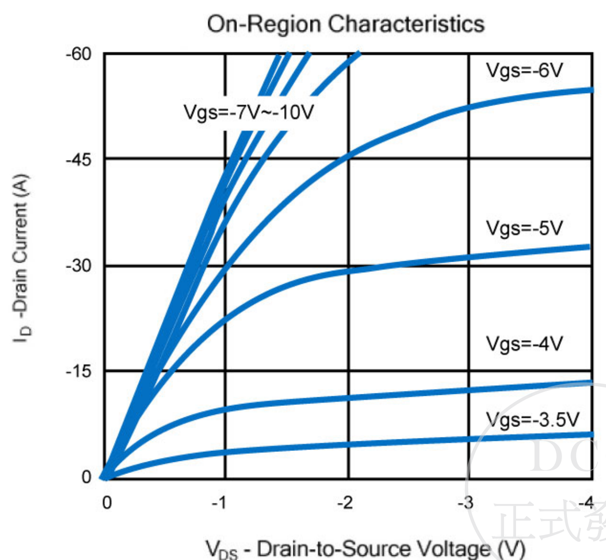












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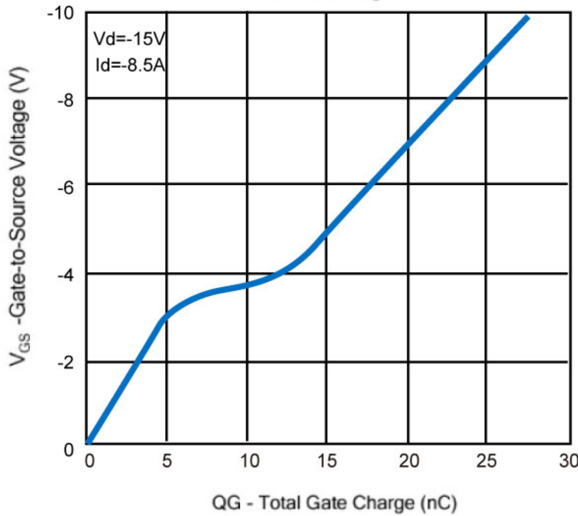
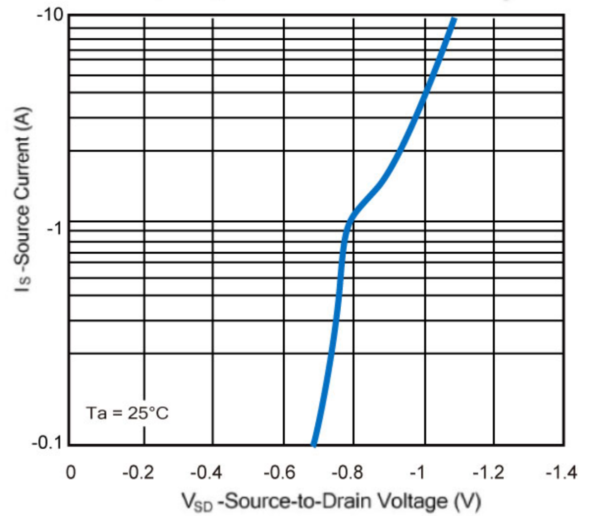
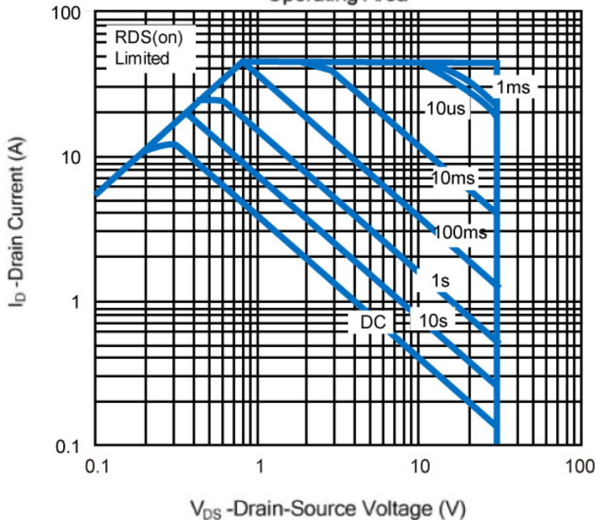
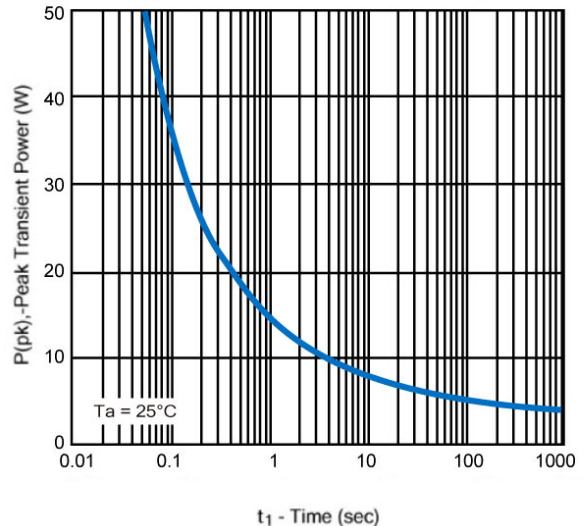
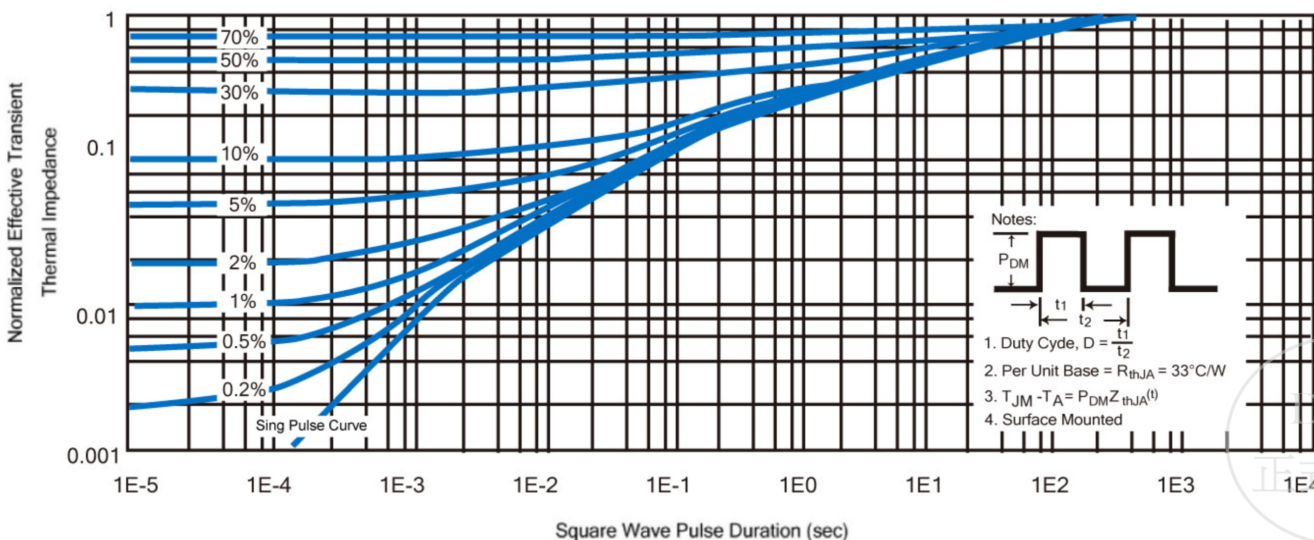




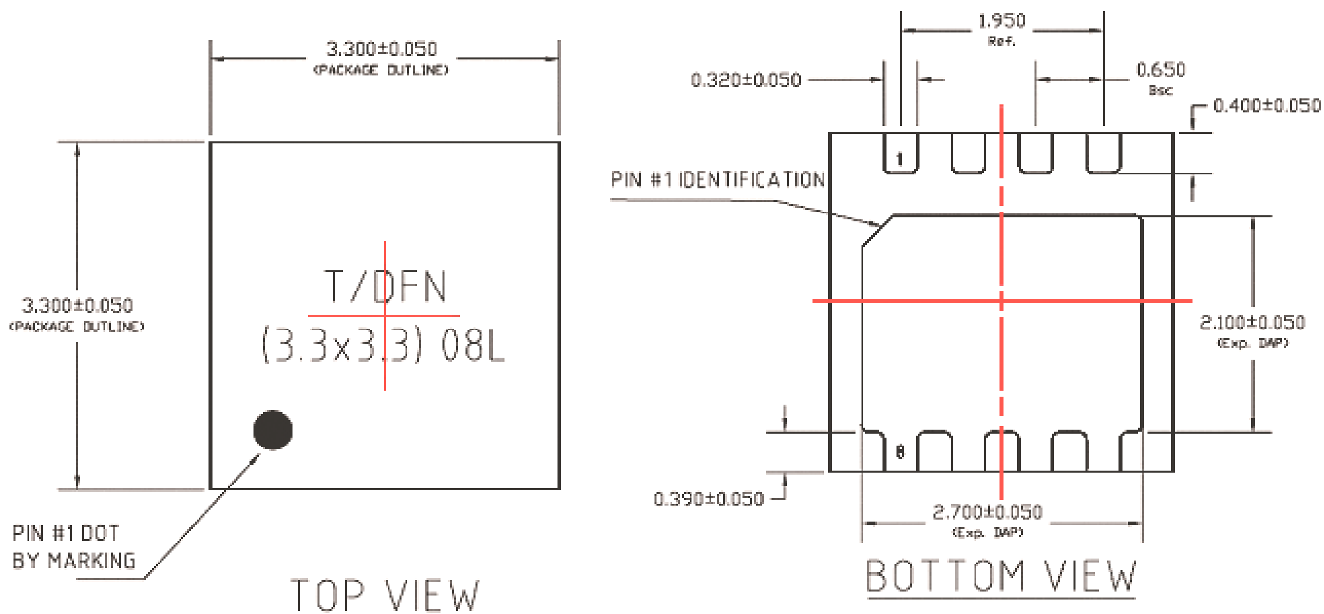


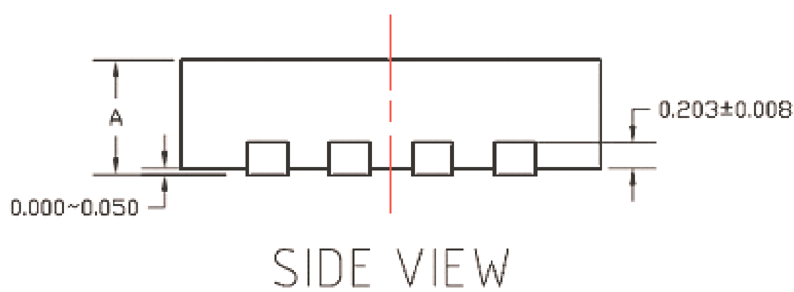




DCC 正式發行

DFN 3.3x3.3 Package Outline





		DFN	TDFN
A	MAX.	1.000	0.800
	NOM.	0.850	0.750
	MIN.	0.800	0.700

Unit：mm