ME7839S-G

P-Channel 30-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME7839S P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

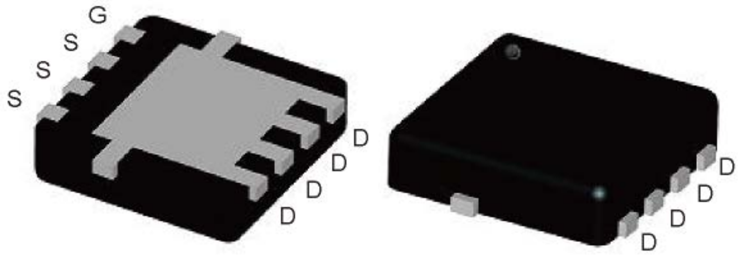
- ● $R_{DS(ON)}$ ≦12mΩ@V_{GS}=-10V
- ● $R_{DS(ON)}$ ≦19mΩ@V_{GS}=-4.5V

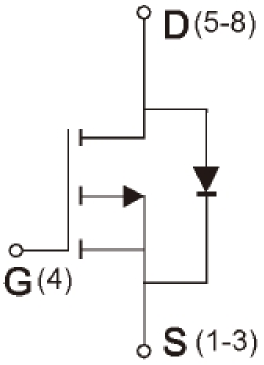
APPLICATIONS

- ● Power Management in Note book
- ● Portable Equipment
- ● Battery Powered System
- ● Load Switch
- ● DSC

PIN CONFIGURATION

(DFN(S) 3X3)
Top View





P-Channel

- **Ordering Information**: ME7839S-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_A=25℃	I_D	36.1	A
	T_A=70℃		28.9	
Pulsed Drain Current		I_{DM}	144	A
Maximum Power Dissipation	T_A=25℃	P_D	25	W
	T_A=70℃		16	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	5	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

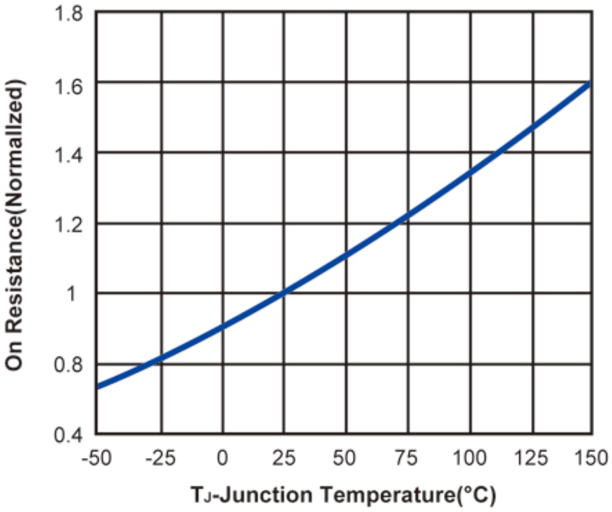
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1		-2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=-10V, I_D= -12A		8	12	mΩ
		V_{GS}=-4.5V, I_D= -9A		12	19	
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V			-1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-15V,V_{GS}=-4.5V, I_D=-15A		27.6		nc
Qgs	Gate-Source Charge			14.1		
Qgd	Gate-Drain Charge			16.3		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V,f=1MHz		2690		pF
Coss	Output Capacitance			371		
Crss	Reverse Transfer Capacitance			293		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V,f=1MHz		6.5		Ω
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-15V, R_L =15Ω R_{GEN}=3.3Ω, V_{GS}=-10V		45.5		ns
t_r	Turn-On Rise Time			19.3		
$t_{d(off)}$	Turn-Off Delay Time			152		
t_f	Turn-Off Fall Time			40.8		

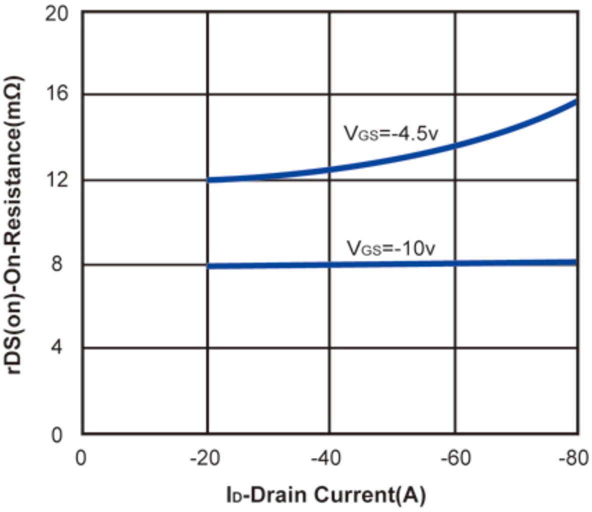
Note:a. Pulse test: pulse width≦300us, duty cycle≦2%

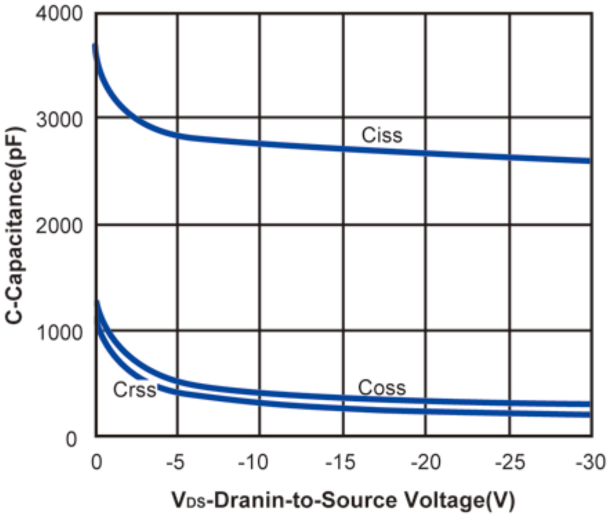
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

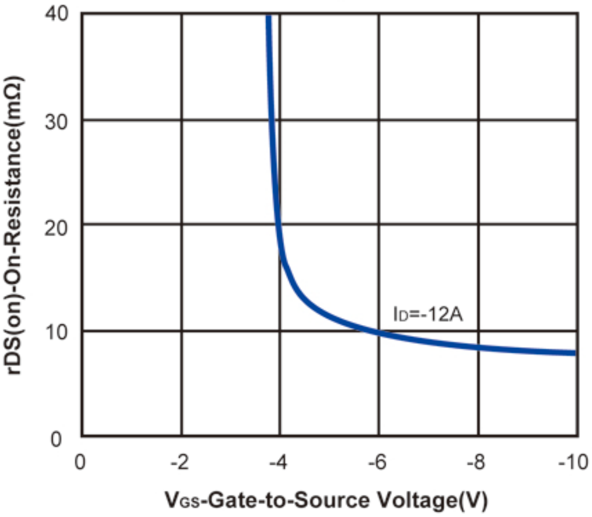
P-Channel 30-V (D-S) MOSFET

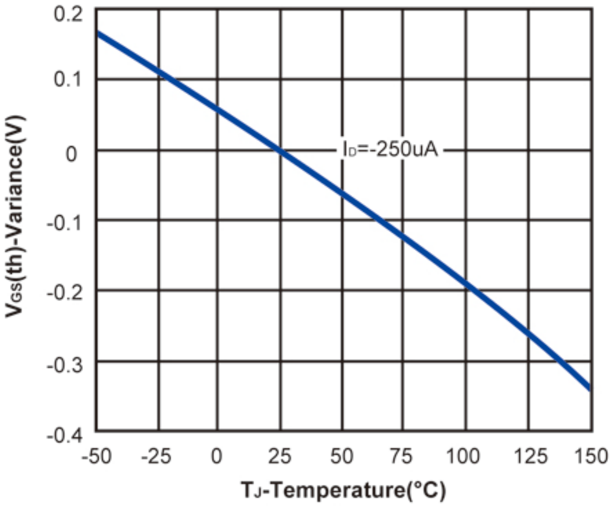
Typical Characteristics (TJ =25℃ Noted)

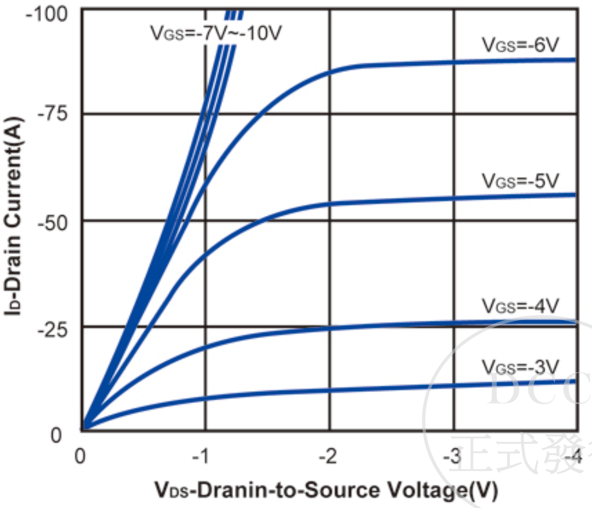

On Resistance vs. Junction Temperature


On Resistance vs. Drain Current

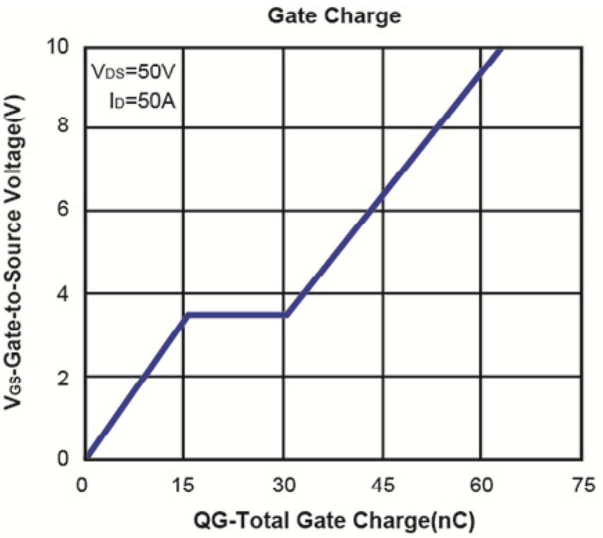

Capacitance


On Resistance vs. Gate-to-Source Voltage

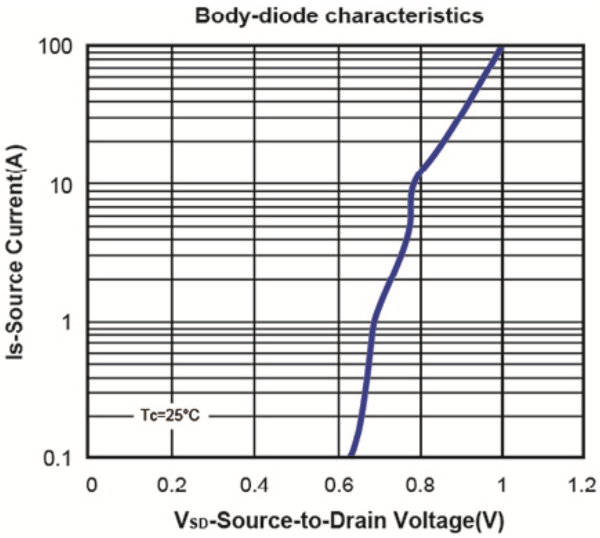

Threshold Voltage


On-Region Characteristics

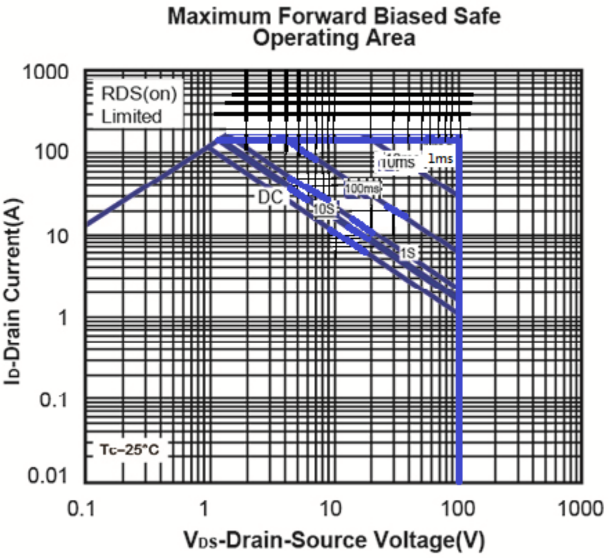
Typical Characteristics (TJ =25℃ Noted)



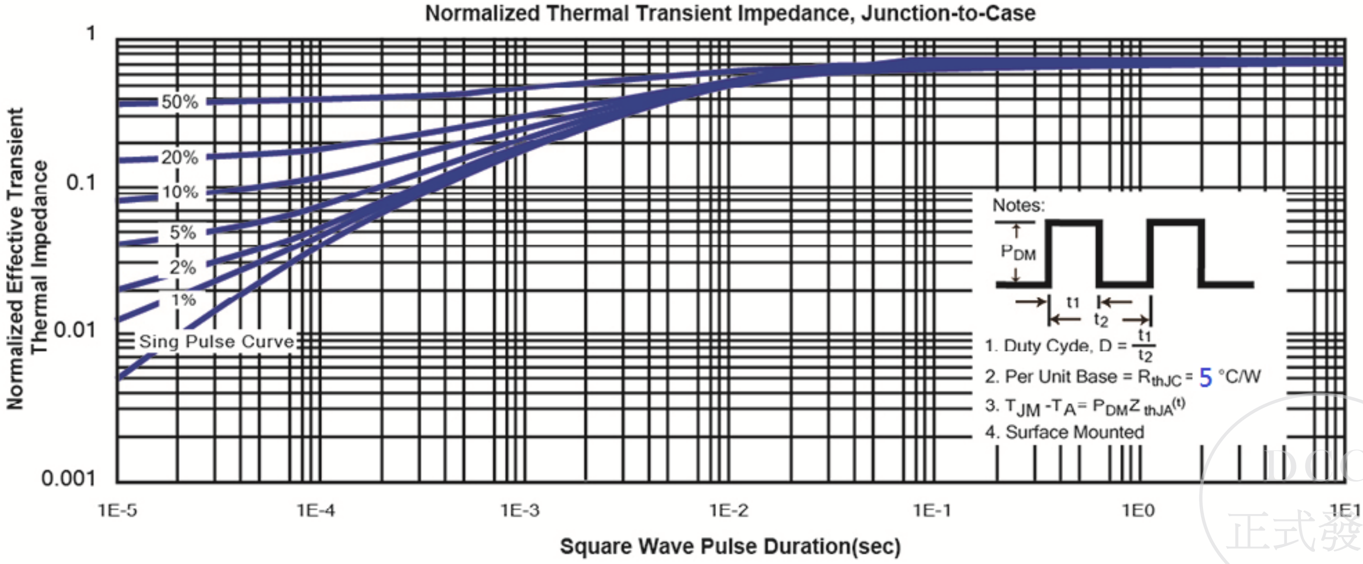
Gate Charge



Body-diode characteristics

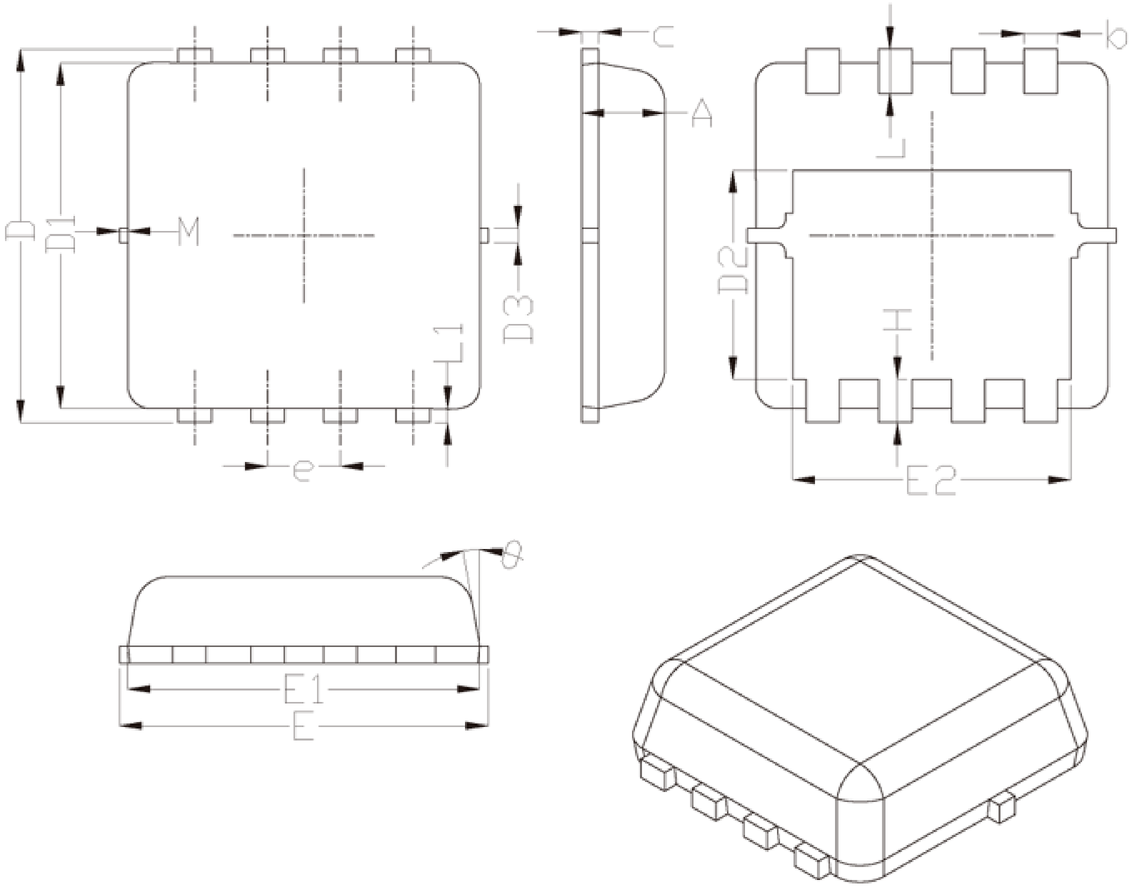


Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

DFN(S) 3x3 Package Outline



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15
* Not specified			