Dual N-Channel 20-V(D-S) MOSFET , ESD Protection

GENERAL DESCRIPTION

The ME7900ED-G is the dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology . This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 22m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 23m\Omega @ V_{GS}=4V$
- $R_{DS(ON)} \leqq 25m\Omega @ V_{GS}=3.1V$
- $R_{DS(ON)} \leqq 30m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

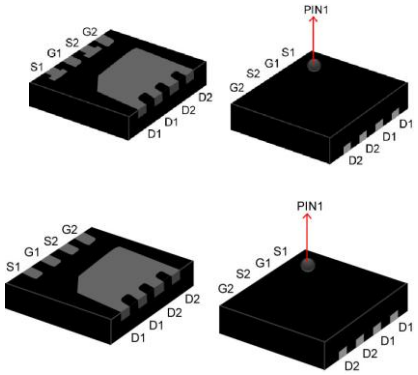
APPLICATIONS

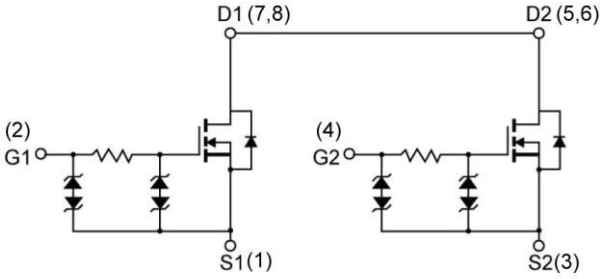
- Power Management in Note book
- Battery Powered System
- DC/DC Converter low side switching
- Load Switch

PIN CONFIGURATION

(DFN 3x3)

Top View





Ordering Information: ME7900ED-G (Green product- Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current*	T_A=25℃	I_D	8.3	A
	T_A=70℃		6.6	
Pulsed Drain Current		I_{DM}	33	A
Maximum Power Dissipation*	T_A=25℃	P_D	2.4	W
	T_A=70℃		1.5	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	52	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.5		1.2	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=4.5V, I_D= 4A		17	22	mΩ
		V_{GS}=4V, I_D= 4A		18	23	
		V_{GS}=3.1V, I_D=4A		19	25	
		V_{GS}=2.5V, I_D=2A		22	30	
V_{SD}	Diode Forward Voltage	I_S=6.5A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=6.5A		11		nC
Qgs	Gate-Source Charge			1.9		
Qgd	Gate-Drain Charge			3		
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1.0MHz		330		pF
Coss	Output Capacitance			100		
Crss	Reverse Transfer Capacitance			31		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=10V,I_D=1.0A, V_{GEN}=4.5V R_G=6Ω		300		ns
tr	Turn-On Rise Time			472		
$t_{d(off)}$	Turn-Off Delay Time			4570		
t_f	Turn-Off Fall Time			1510		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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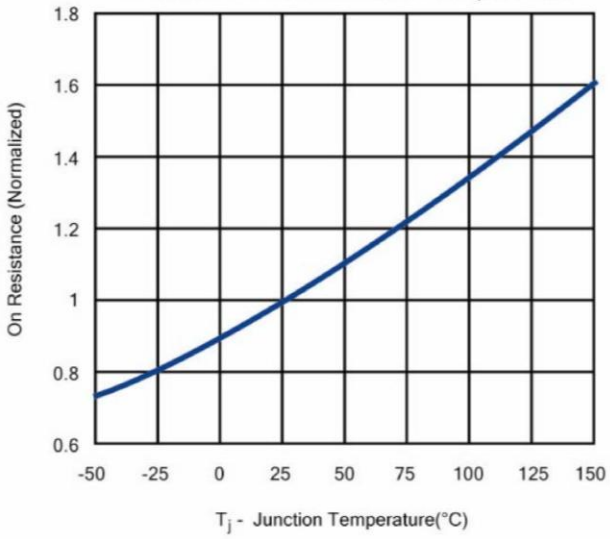
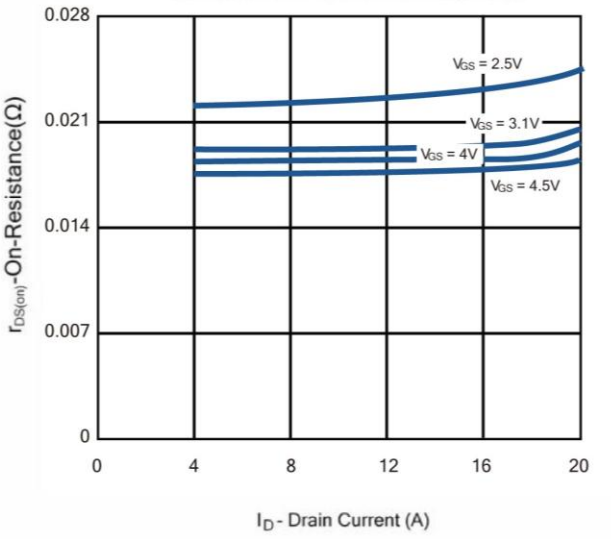
Typical Characteristics (T_J =25℃ Noted)

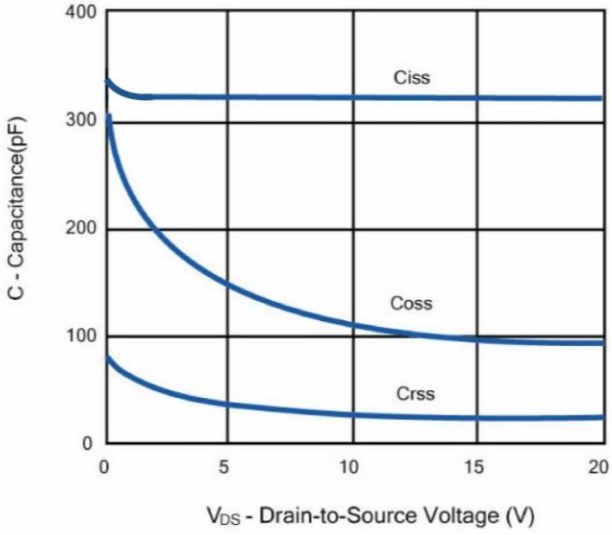
On Resistance vs. Junction Temperature



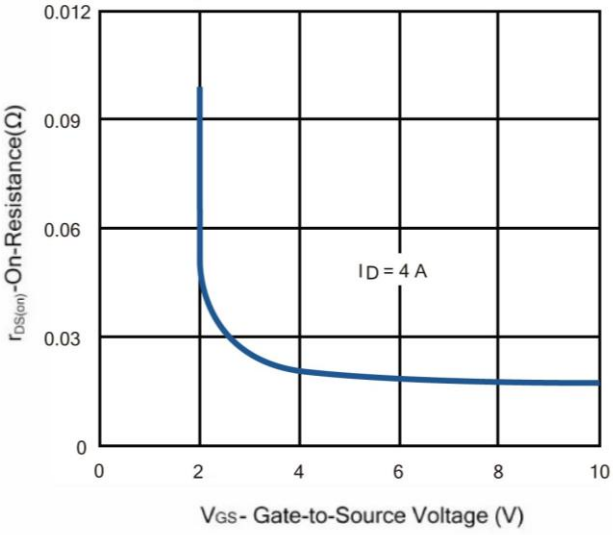
On-Resistance vs. Drain Current



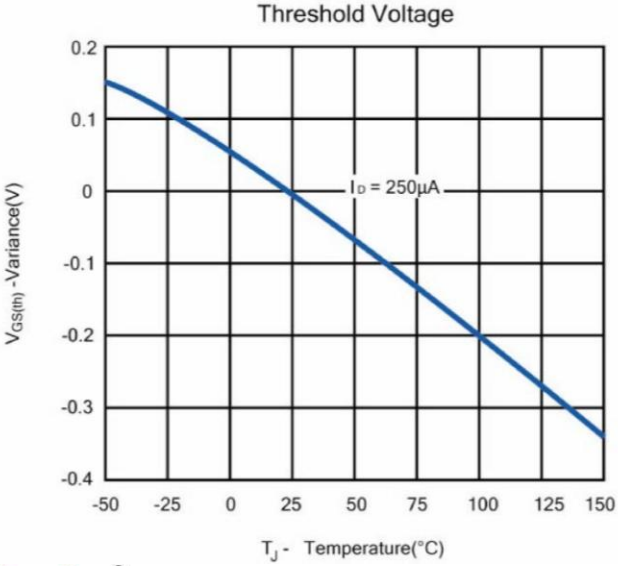
Capacitance



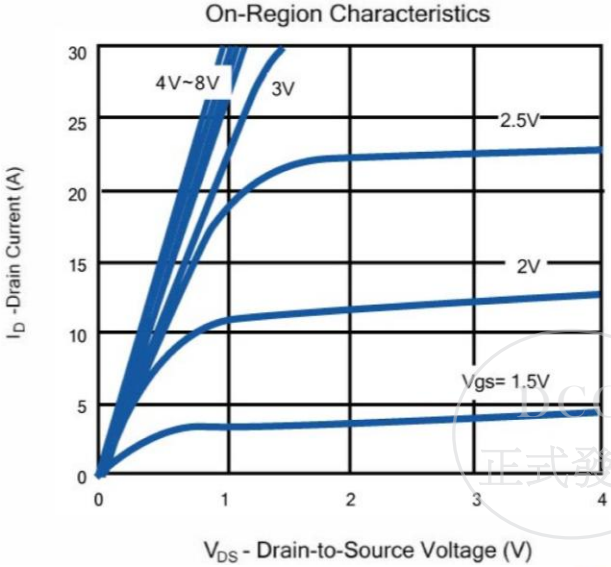
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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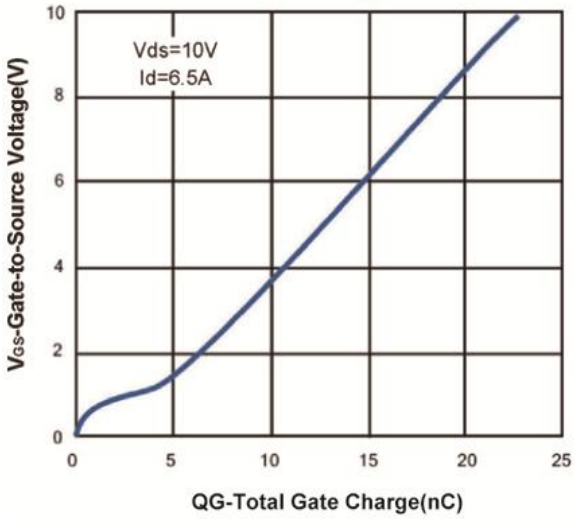
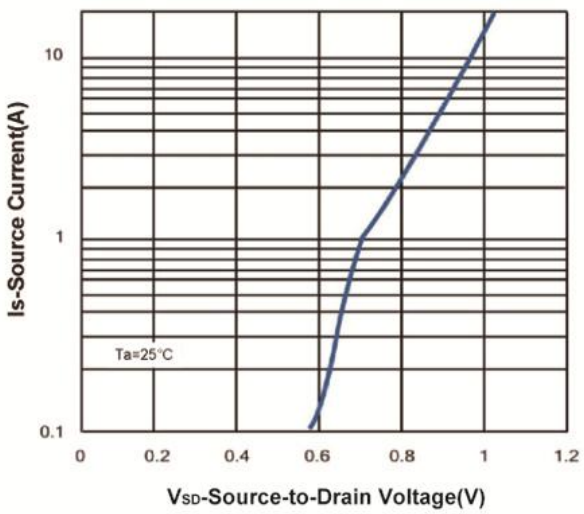
Typical Characteristics (T_J =25℃ Noted)

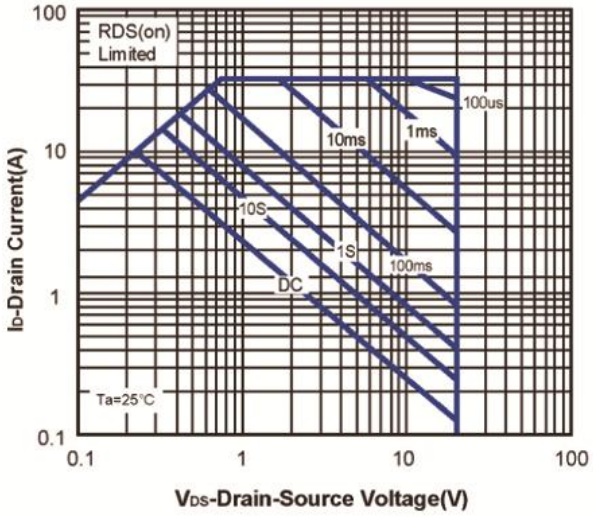
Gate Charge



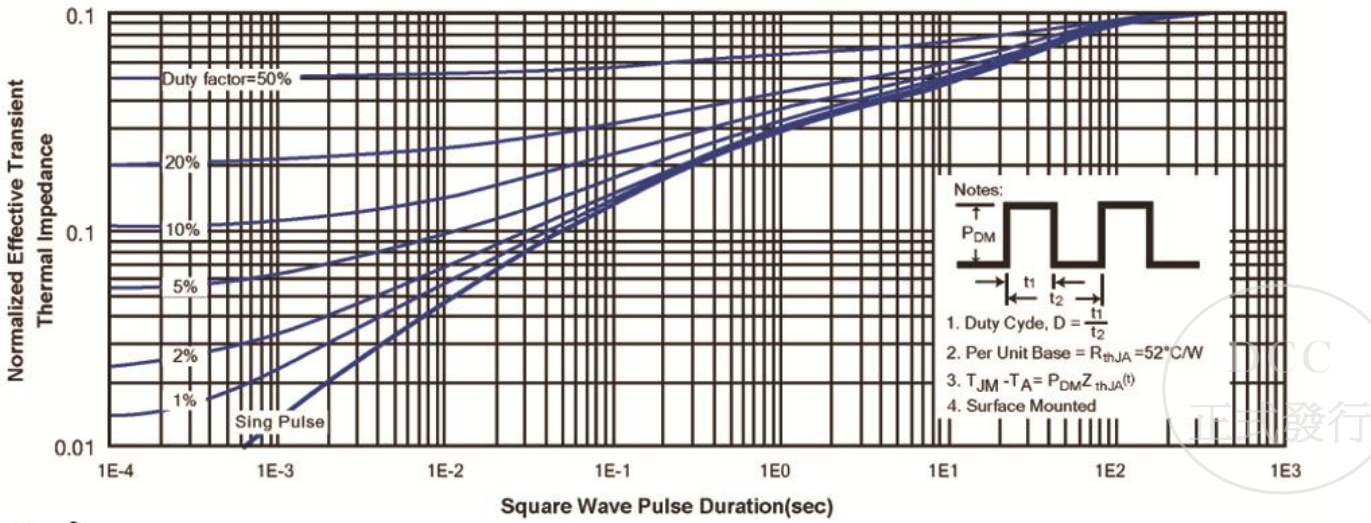
Body-diode characteristics



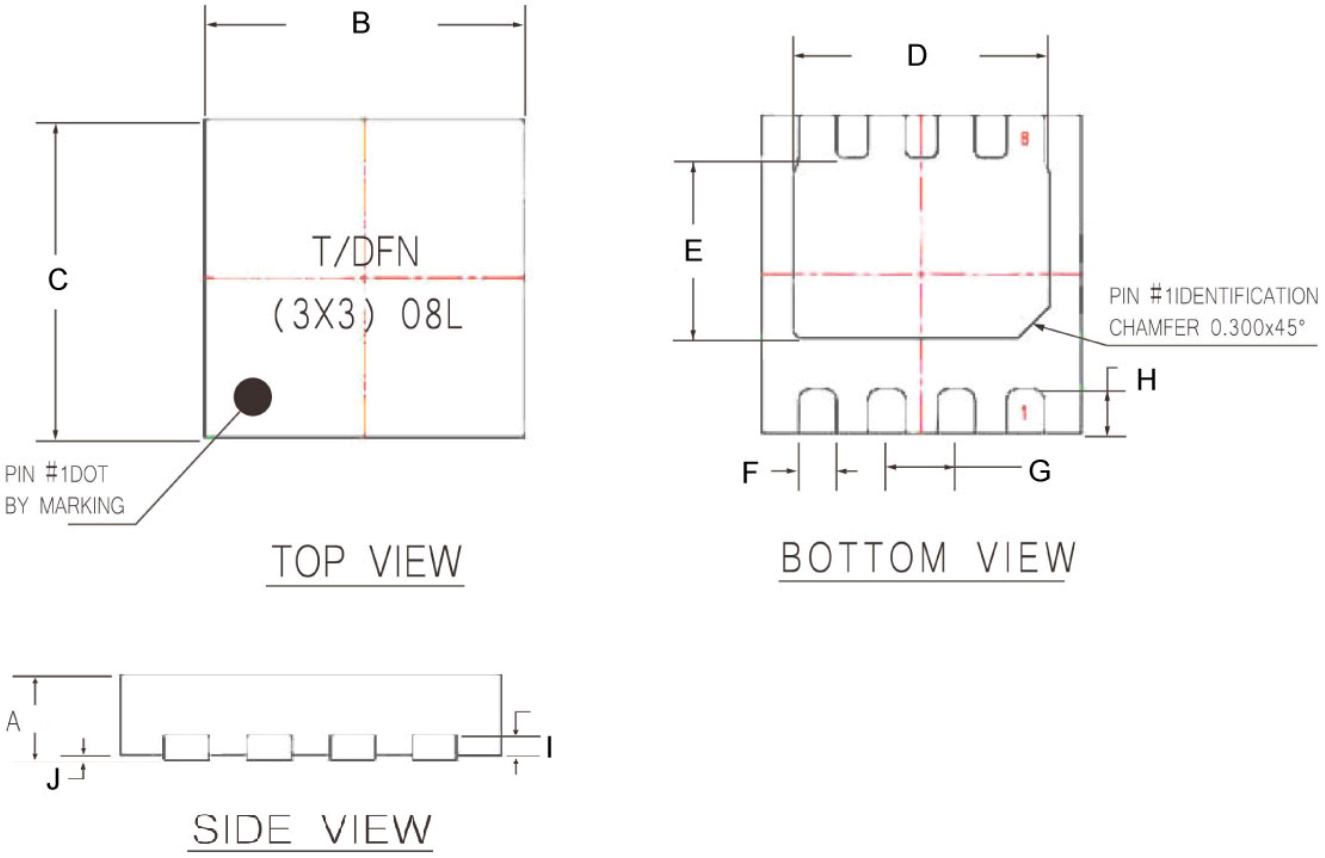
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

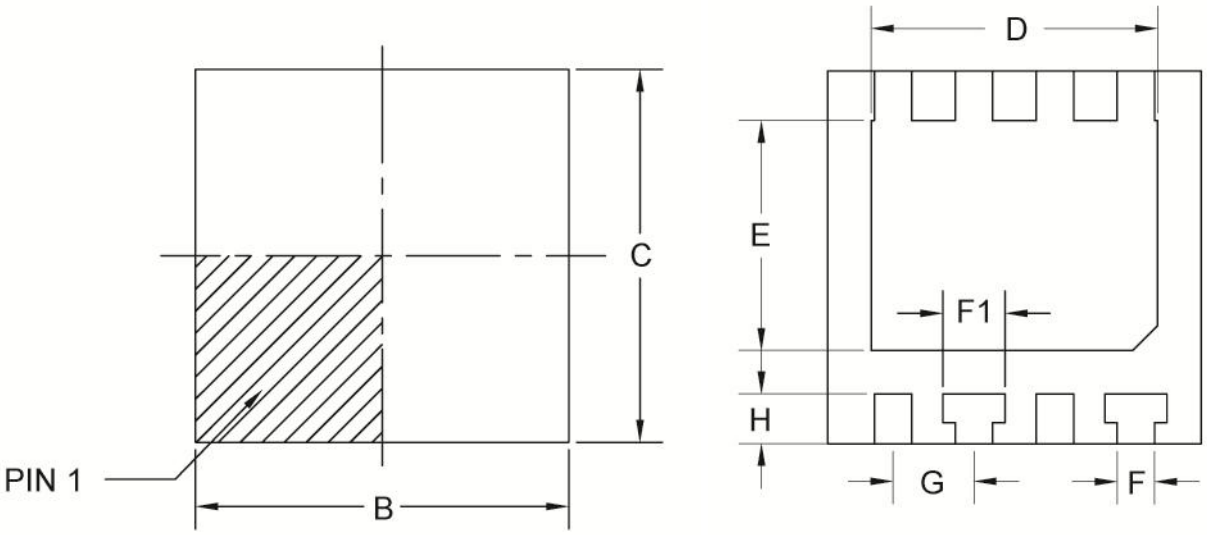


DFN 3x3 Package Outline



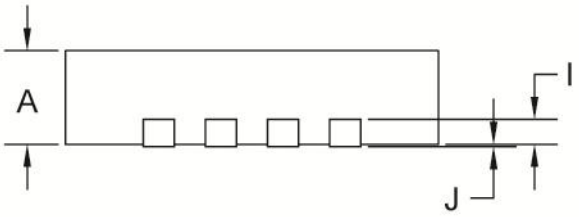
SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.700	0.900
B	2.900	3.100
C	2.900	3.100
D	2.350	2.450
E	1.650	1.750
F	0.300	0.400
G	0.65BSC	
H	0.370	0.470
I	0.195	0.211
J	0.000	0.050

DFN 3x3 (II)Package Outline



TOP VIEW

BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.70	0.80
B	3.00 BSC	
C	3.00 BSC	
D	2.20	2.40
E	1.75	1.95
F	0.25	0.35
F1	0.42	0.58
G	0.65 BSC	
H	0.30	0.50
I	0.20 REF	
J	0.00	0.05