

Dual N-Channel 20-V(D-S) MOSFET , ESD Protection

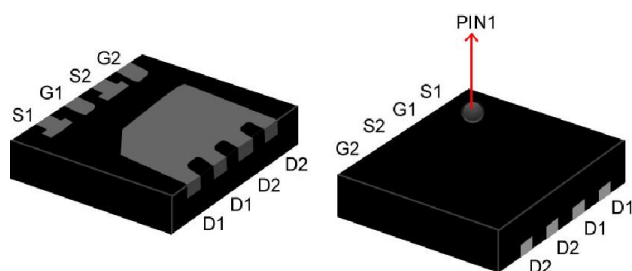
GENERAL DESCRIPTION

The ME7910D is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

(DFN 3x3)

Top View

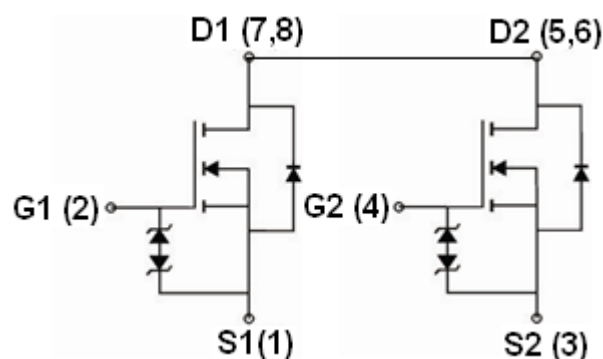


FEATURES

- $R_{DS(ON)} \leq 14m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leq 15m\Omega @ V_{GS}=4V$
- $R_{DS(ON)} \leq 17.5m\Omega @ V_{GS}=3.1V$
- $R_{DS(ON)} \leq 21m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Battery Powered System
- DC/DC Converter low side switching
- Load Switch



Ordering Information: ME7910D (Pb-free)

ME7910D-G (Green product- Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current*	$T_A=25^\circ C$	I_D	10.3	A
	$T_A=70^\circ C$		8.2	
Pulsed Drain Current		I_{DM}	41	A
Maximum Power Dissipation*	$T_A=25^\circ C$	P_D	2.4	W
	$T_A=70^\circ C$		1.5	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	52	$^\circ C/W$

* The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V, ID=1mA	20			V
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=1mA	0.5		1.3	V
IGSS	Gate Leakage Current	VDS=0V, VGS=±10V			±10	μA
IDSS	Zero Gate Voltage Drain Current	VDS=20V, VGS=0V			1	μA
RDS(ON)	Drain-Source On-State Resistance ^a	VGS=4.5V, ID= 5A		10.5	14	mΩ
		VGS=4V, ID= 5A		11	15	
		VGS=3.1V, ID=5A		12.5	17.5	
		VGS=2.5V, ID=2A		15	21	
VSD	Diode Forward Voltage	IS=10A, VGS=0V		0.77	1.2	V
DYNAMIC						
Qg	Total Gate Charge	VDS=10V, VGS=10V, ID=10A		30.9		nC
Qgs	Gate-Source Charge			3.7		
Qgd	Gate-Drain Charge			4.9		
Ciss	Input capacitance	VDS=15V, VGS=0V, f=1.0MHz		780		pF
Coss	Output Capacitance			275		
Crss	Reverse Transfer Capacitance			106		
td(on)	Turn-On Delay Time	VDD=10V, ID=2A, VGEN=4.5V RG=1Ω		21.7		ns
tr	Turn-On Rise Time			70.7		
td(off)	Turn-Off Delay Time			71.5		
tf	Turn-Off Fall Time			33.3		

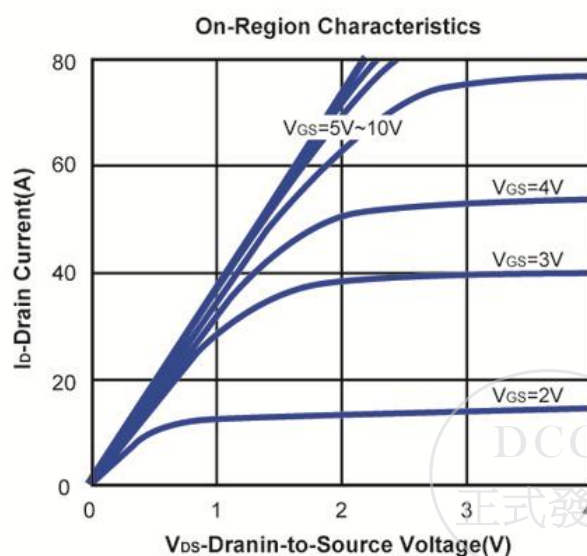
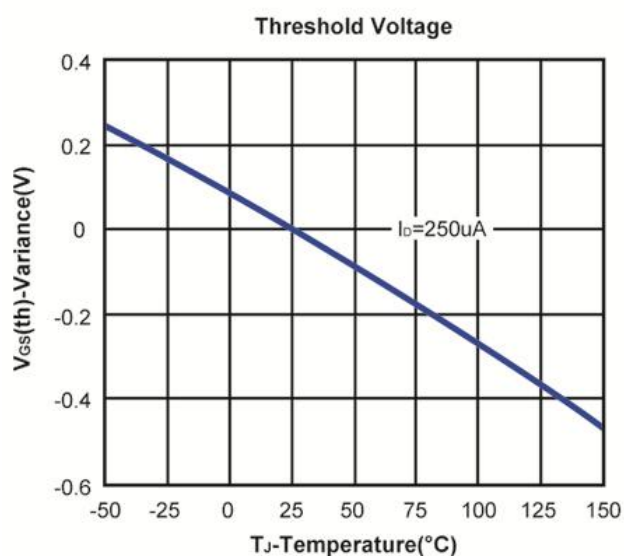
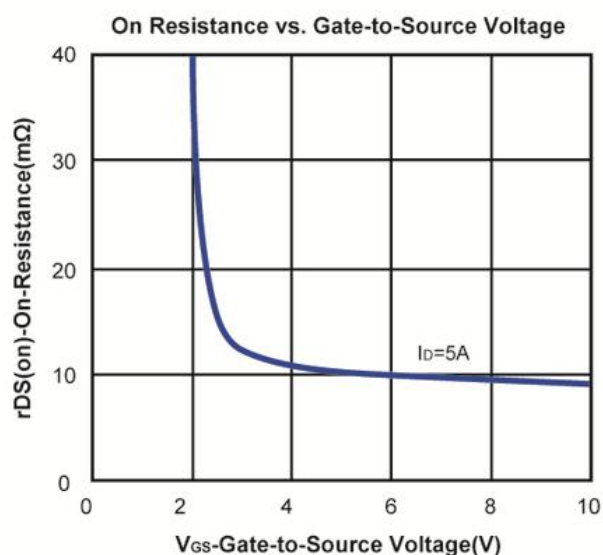
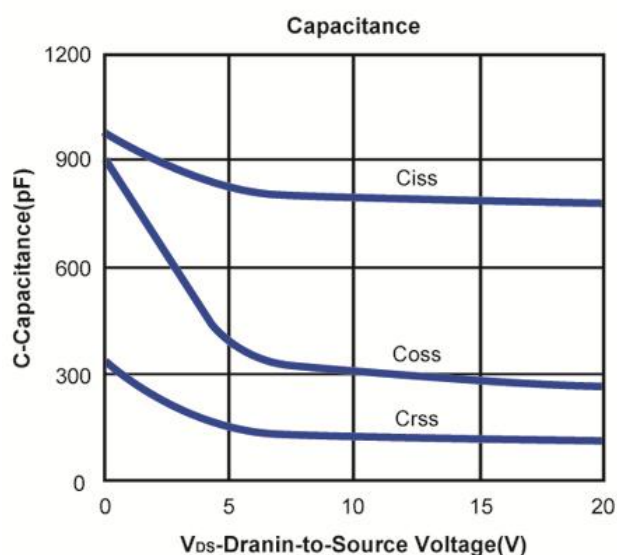
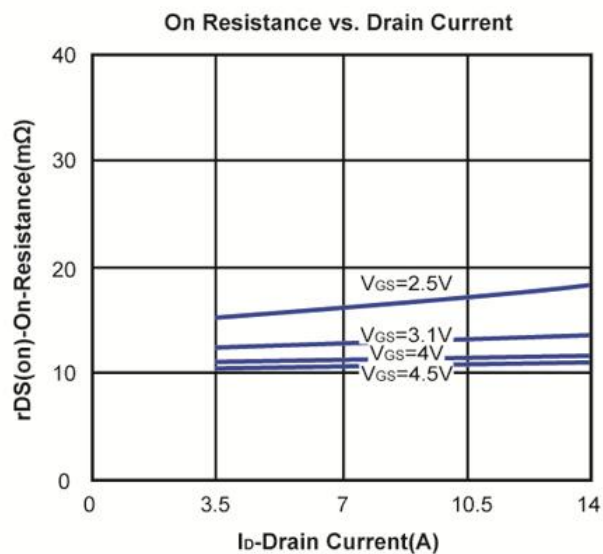
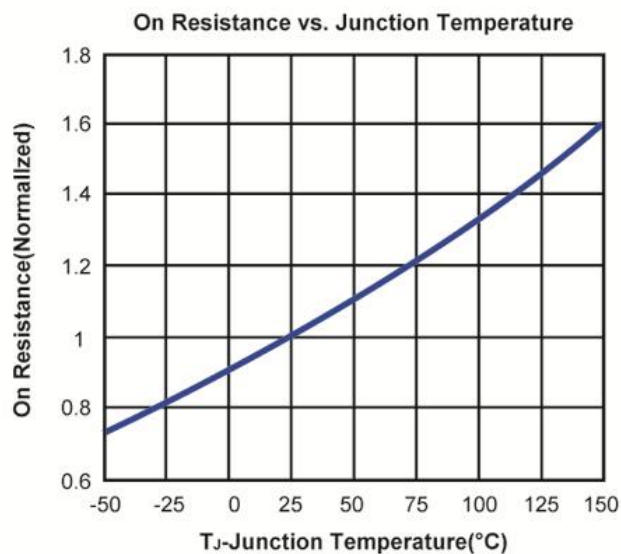
Notes: a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.



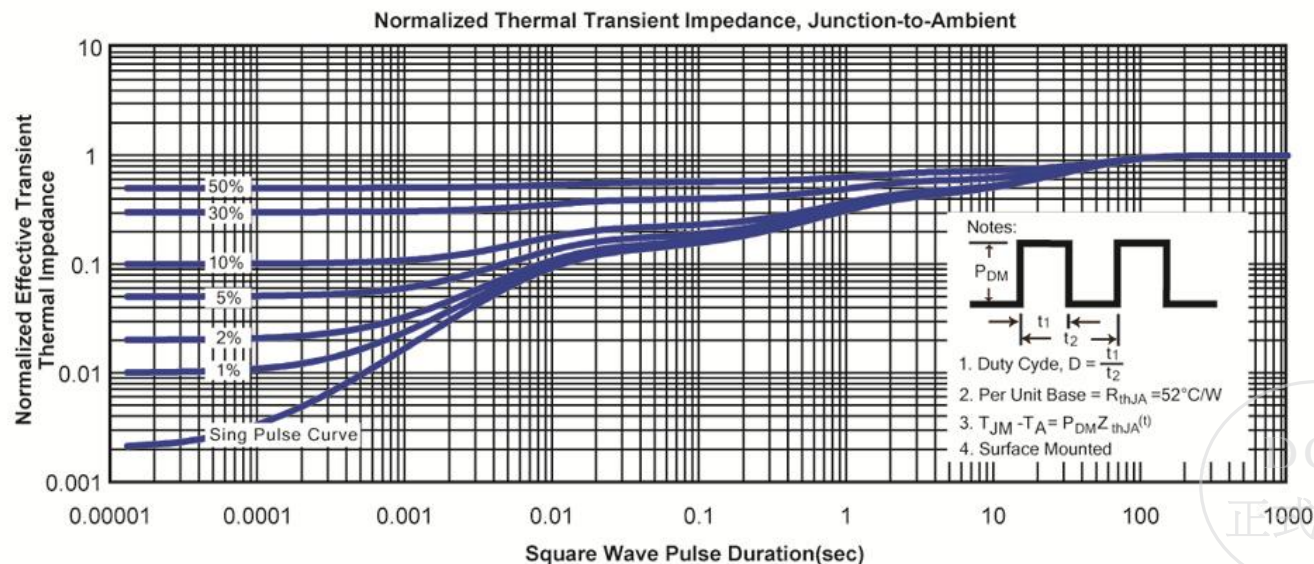
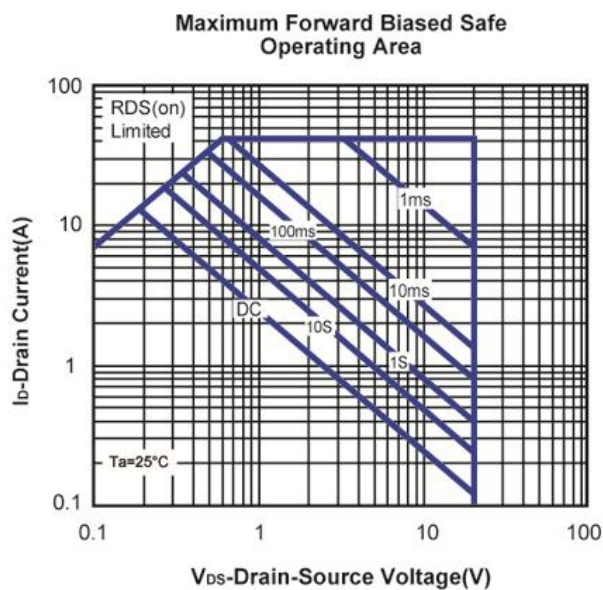
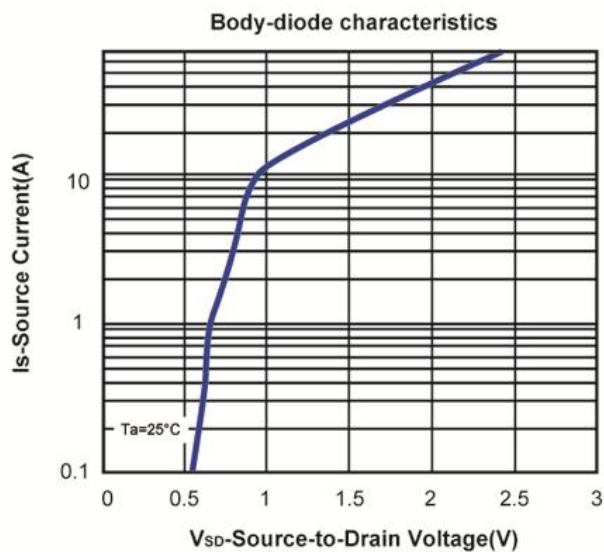
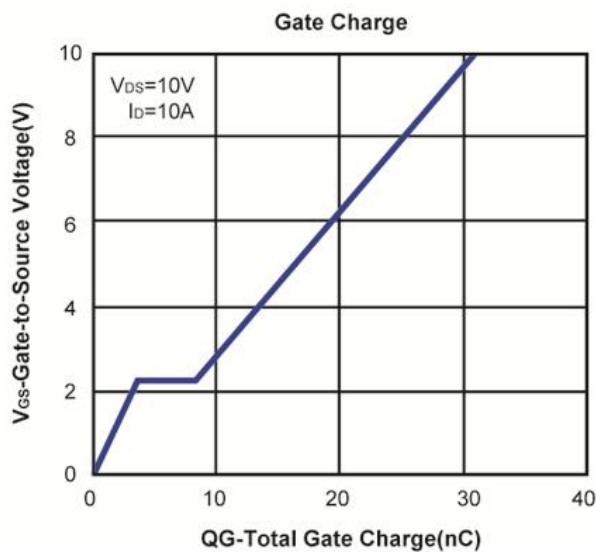
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Typical Characteristics (T_J =25°C Noted)

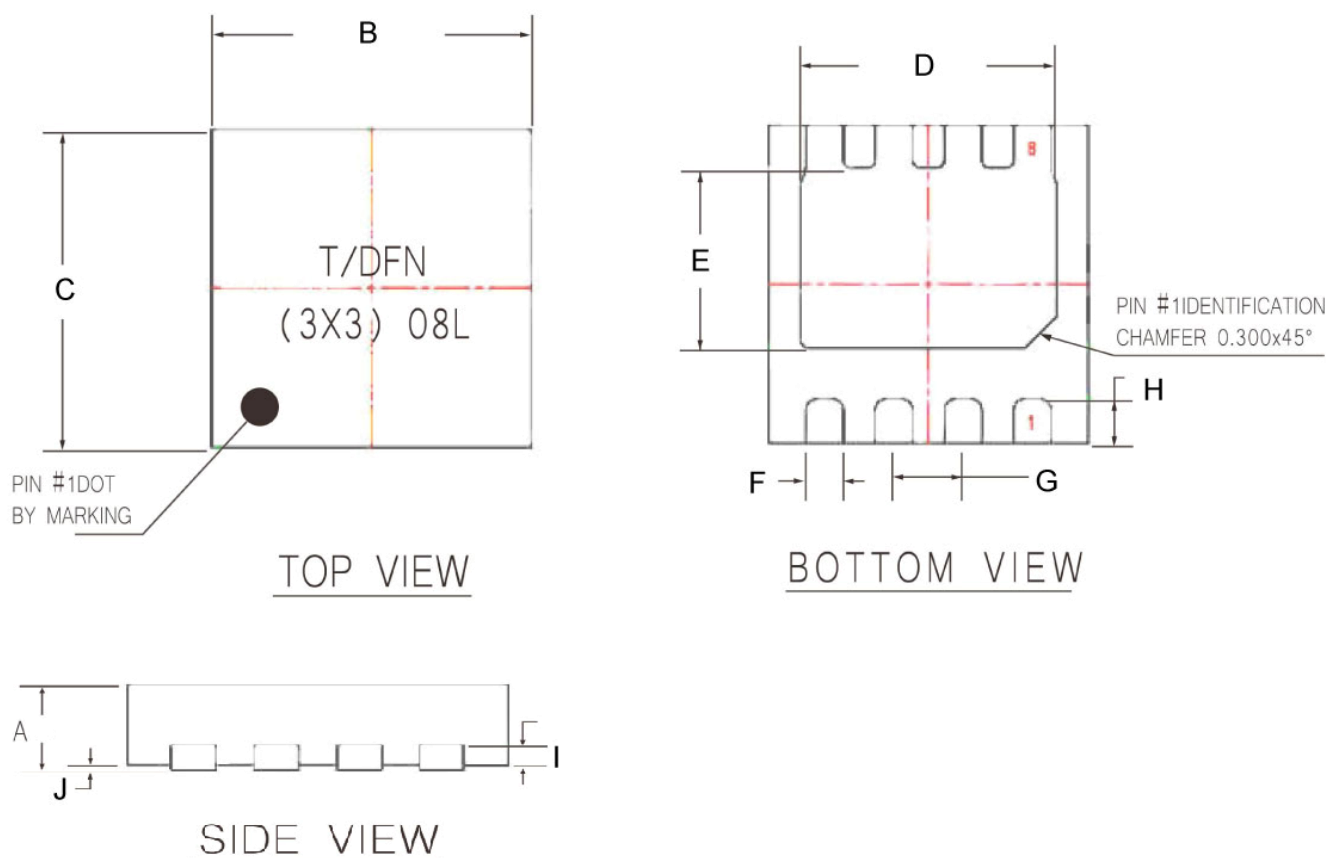


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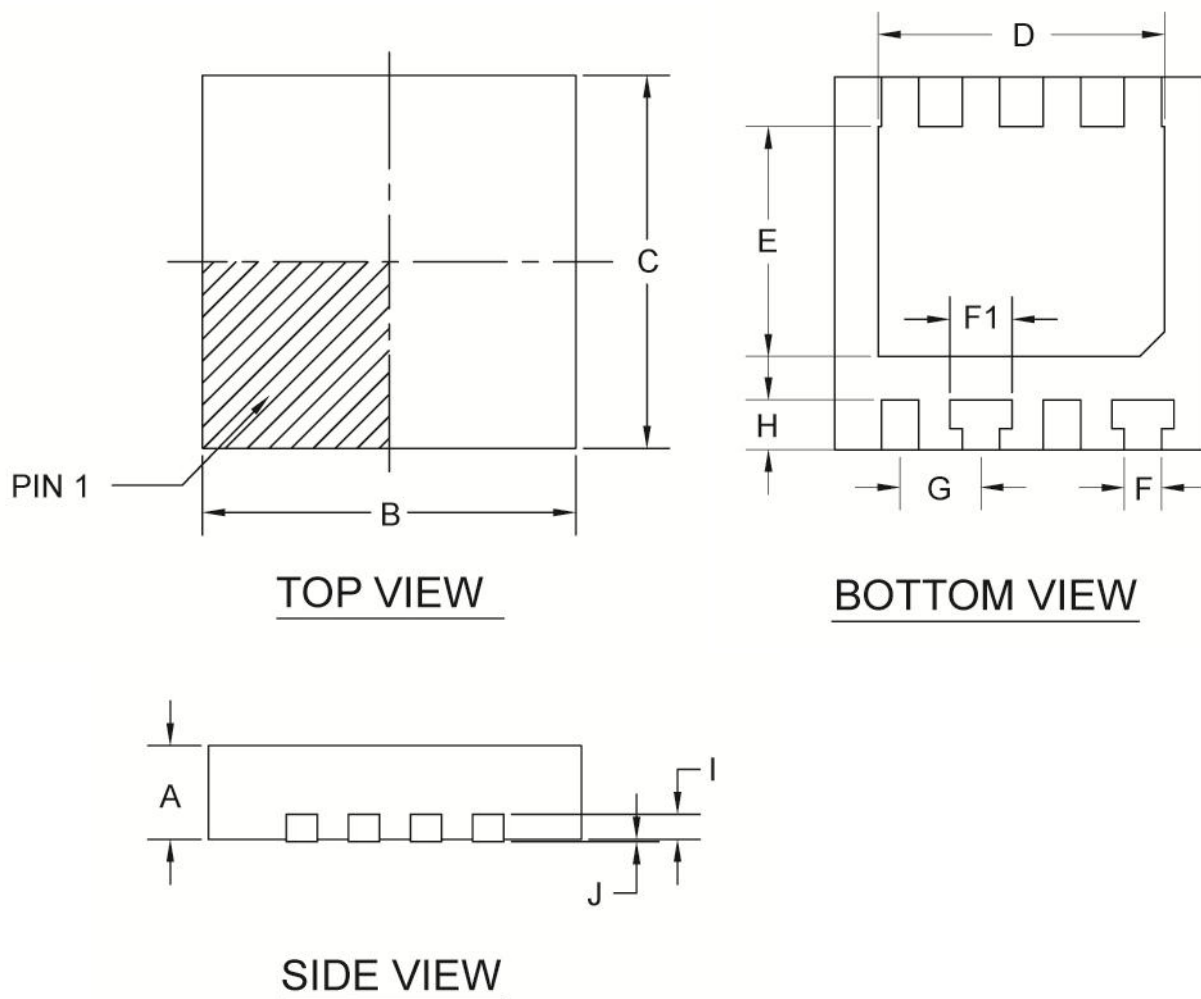
DFN 3x3 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.700	0.900
B	2.900	3.100
C	2.900	3.100
D	2.350	2.450
E	1.650	1.750
F	0.300	0.400
G	0.65BSC	
H	0.370	0.470
I	0.195	0.211
J	0.000	0.050

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DFN 3x3 (II) Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.70	0.80
B	3.00 BSC	
C	3.00 BSC	
D	2.20	2.40
E	1.75	1.95
F	0.25	0.35
F1	0.42	0.58
G	0.65 BSC	
H	0.30	0.50
I	0.20 REF	
J	0.00	0.05

