ME80N08AH/ME80N08AH-G

80V N-Channel Enhancement Mode

GENERAL DESCRIPTION

The ME80N08AH is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

FEATURES

- $R_{DS(ON)} \leqq 5m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

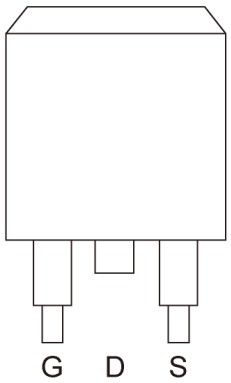
APPLICATIONS

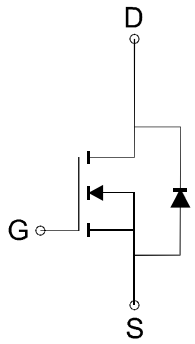
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(TO-263-2L)

Top View





N-Channel MOSFET

Ordering Information: ME80N08AH (Pb-free)

ME80N08AH-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	T_C=25℃	I_D	129	A
	T_C=70℃		108	
Pulsed Drain Current[a]		I_{DM}	516	A
Power Dissipation	T_C=25℃	P_D	150	W
	T_C=70℃		105	
Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	℃
Thermal Resistance-Junction to Case**		$R_{\theta JC}$	1	℃/W

* Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 80A.

** The device mounted on 1in^2 FR4 board with 2 oz copper.

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Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	80			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
I_{GSS}	Gate-Body Leakage	V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=80A		3.9	5	mΩ
V_{SD}	Diode Forward Voltage *	I_S=40A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DD}=40V, V_{GS}=10V, I_D=80A		217		nC
Qg	Total Gate Charge	V_{DD}=40V, V_{GS}=4.5V, I_D=80A		60.3		
Qgs	Gate-Source Charge			65.4		
Qgd	Gate-Drain Charge			52.9		
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		1788		pF
Coss	Output Capacitance			592		
Crss	Reverse Transfer Capacitance			2208		
$t_{d(on)}$	Turn-On Delay Time	V_{GS} =10V, R_L=20Ω V_{DD}=40V, R_G=3.3Ω		51.5		ns
t_r	Turn-On Rise Time			36.3		
$t_{d(off)}$	Turn-Off Delay Time			197		
t_f	Turn-Off Fall Time			56.6		

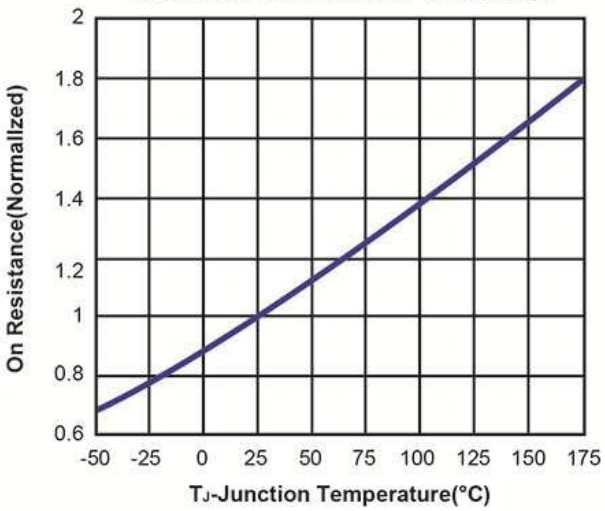
Notes: a. pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

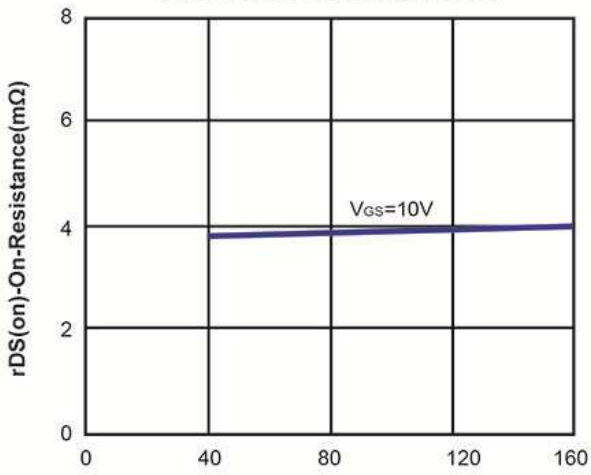
80V N-Channel Enhancement Mode

Typical Characteristics (T_J =25℃ Noted)

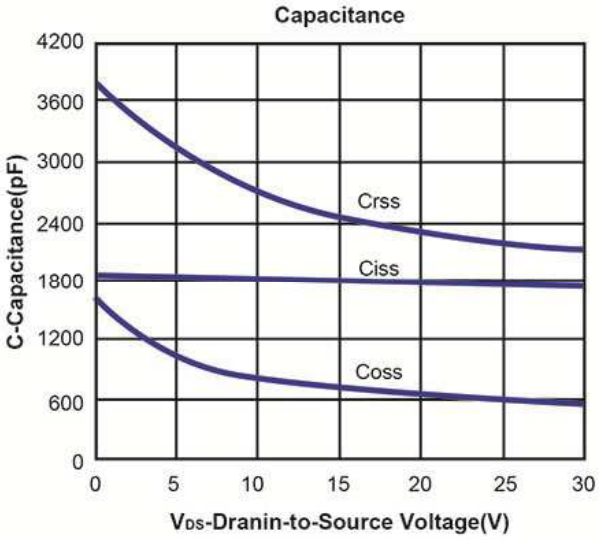
On Resistance vs. Junction Temperature



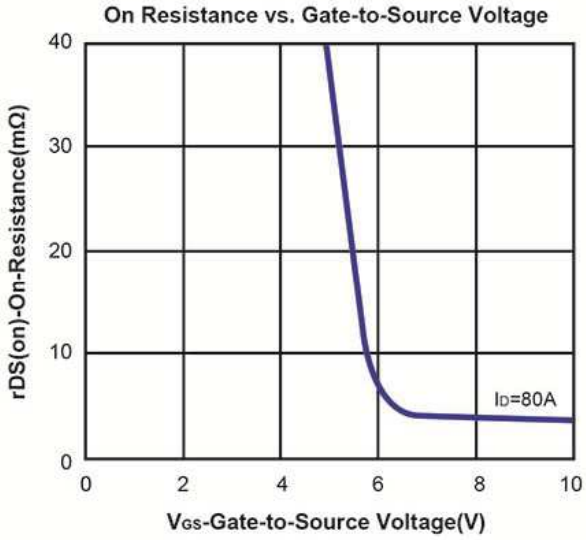
On Resistance vs. Drain Current



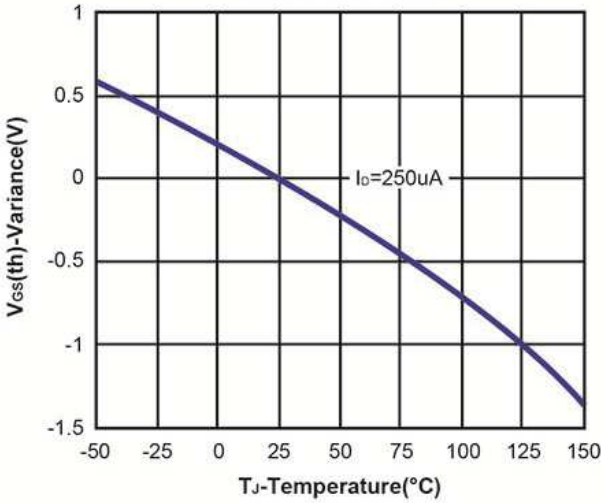
Capacitance



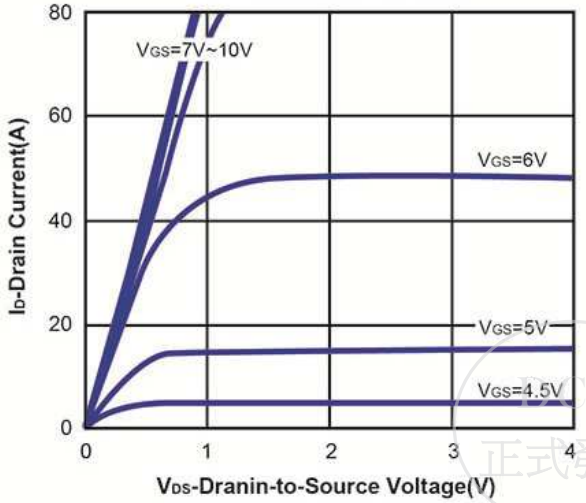
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



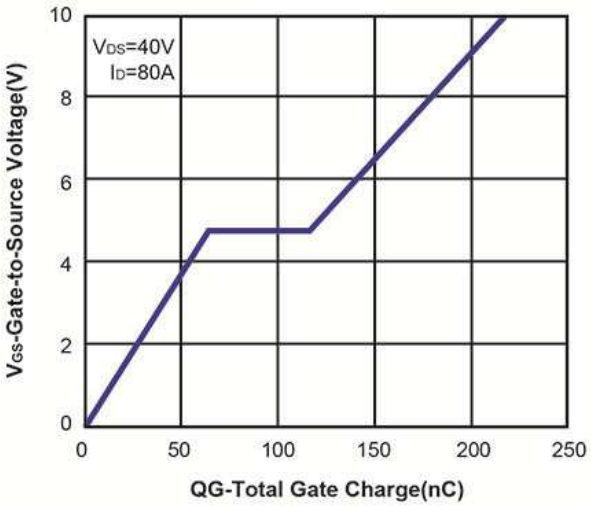
On-Region Characteristics



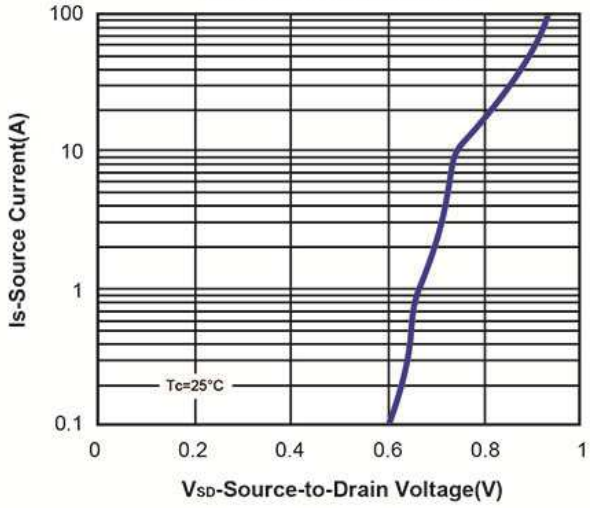
80V N-Channel Enhancement Mode

Typical Characteristics (T_J =25℃ Noted)

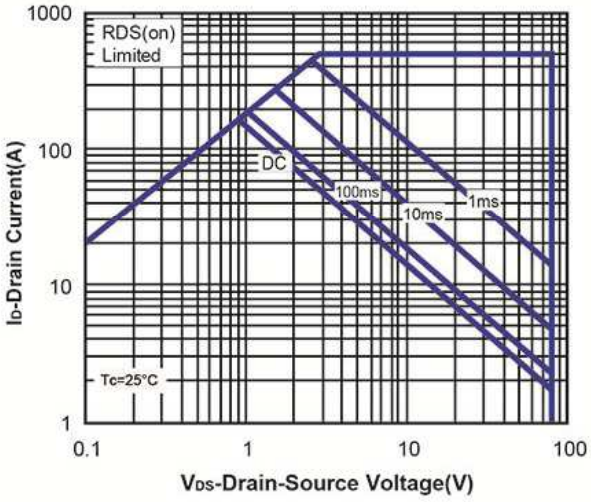
Gate Charge



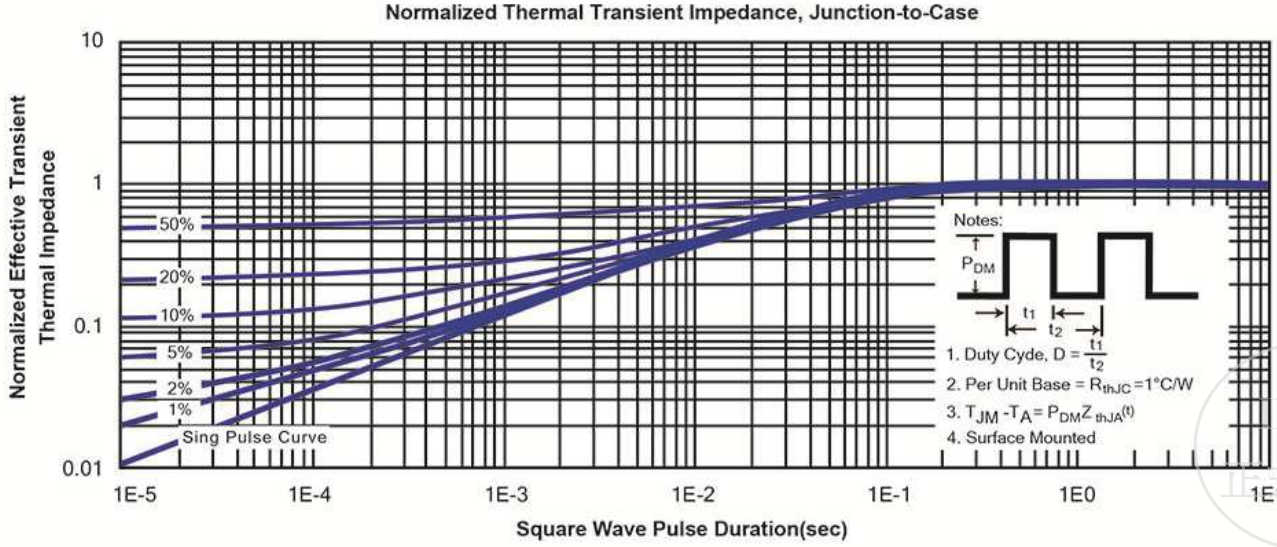
Body-diode characteristics



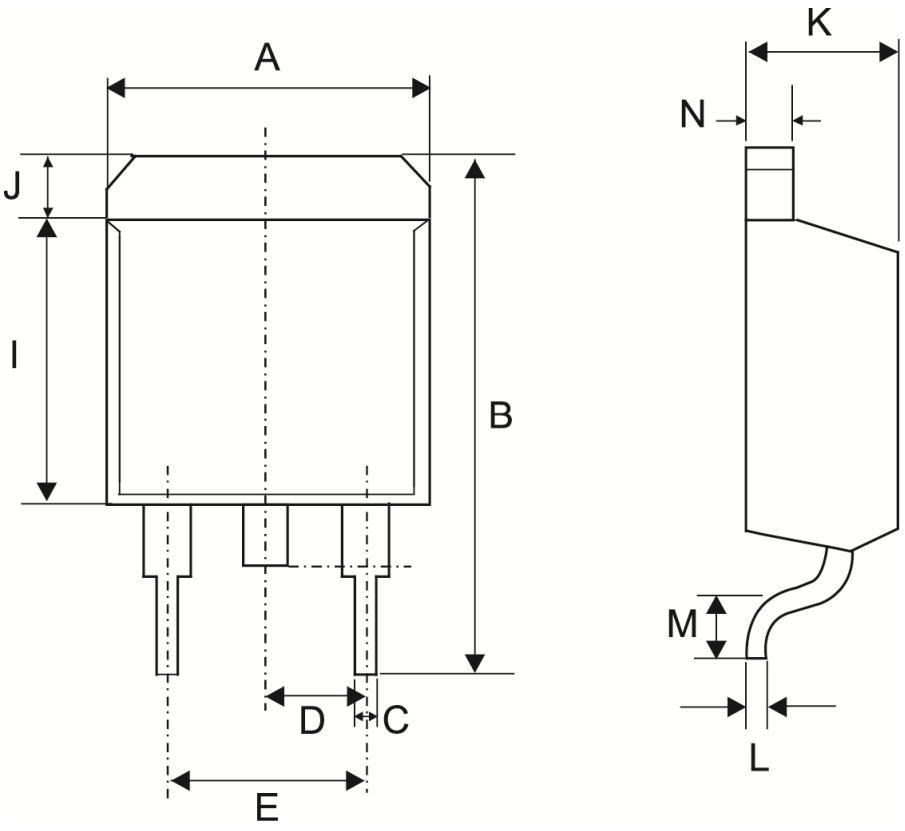
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO-263-2L Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	9.60	10.30
B	15.00	15.80
C	0.70	0.95
D	2.54 BSC	
E	4.98	5.18
I	8.50	9.40
J	1.02	1.55
K	4.30	4.75
L	0.33	0.65
M	1.94	2.79
N	1.15	1.40