

N- Channel 75-V (D-S) MOSFET

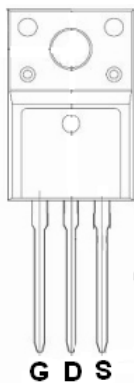
GENERAL DESCRIPTION

The ME80N75F is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

PIN CONFIGURATION

(TO-220F)

Top View

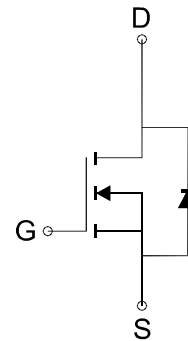


FEATURES

- $R_{DS(ON)} \leq 10m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter
- Load Switch



N-Channel MOSFET

Ordering Information: ME80N75F (Pb-free)

ME80N75F-G (Green product-Halogen free)

Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	75	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	Tc=25°C	55.7
		Tc=70°C	46.6
Pulsed Drain Current	I_{DM}	223	A
Single pulse Avalanche Current L=0.3mH	I_{AS}	Tc=25°C	40
		Tc=70°C	33.5
Single pulse Avalanche Energy L=0.3mH	E_{AS}	Tc=25°C	240
		Tc=70°C	168
Maximum Power Dissipation	P_D	Tc=25°C	61.9
		Tc=70°C	43.4
Junction and Storage Temperature Range	T_J	-55 to 175	°C
Thermal Resistance-Junction to Case*	$R_{\theta JC}$	2.42	°C/W

* The device mounted on 1in² FR4 board with 2 oz copper.

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Electrical Characteristics (T_c =25°C Unless Otherwise Specified)

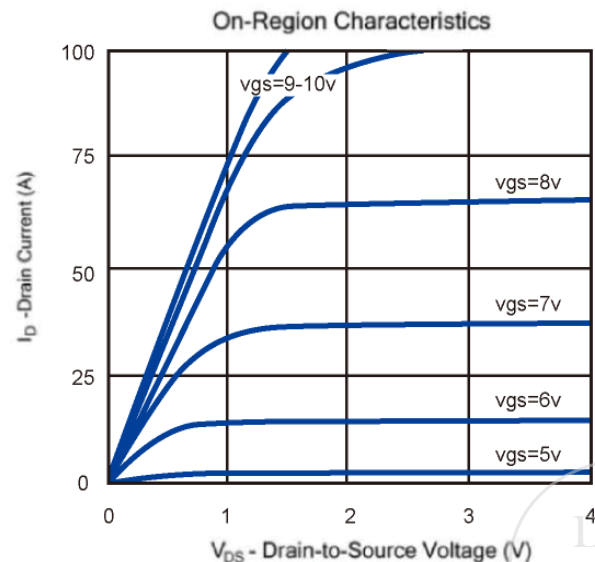
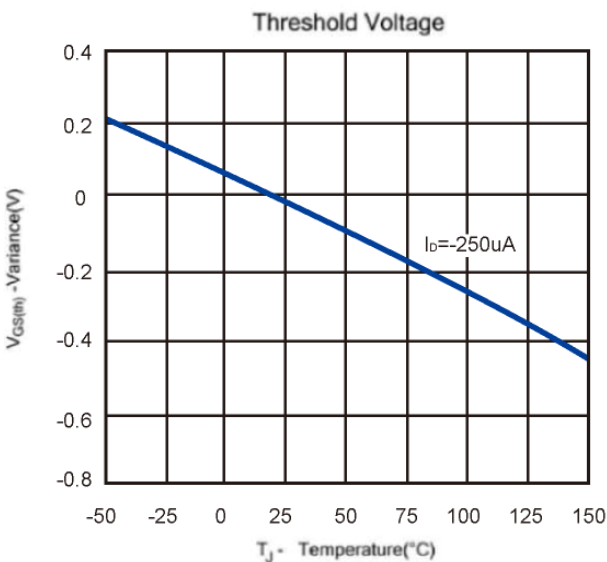
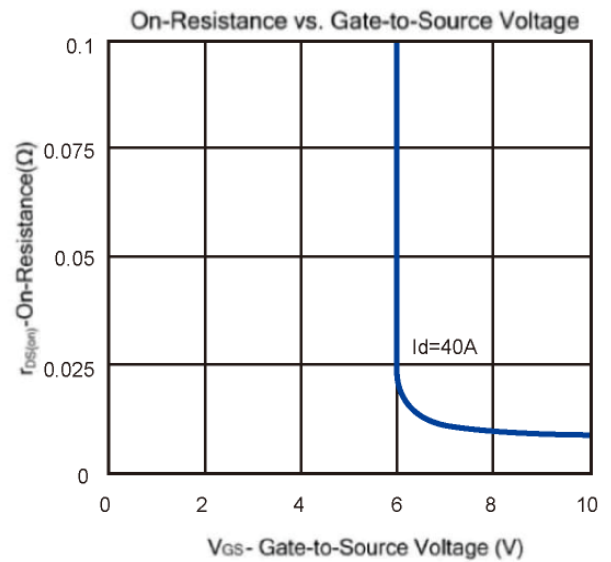
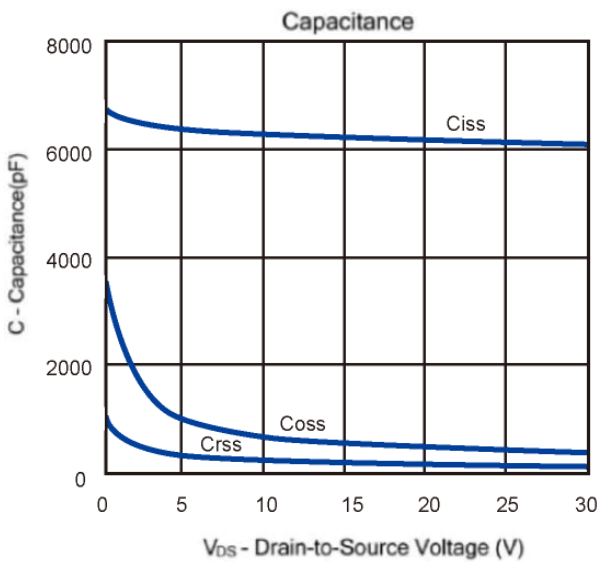
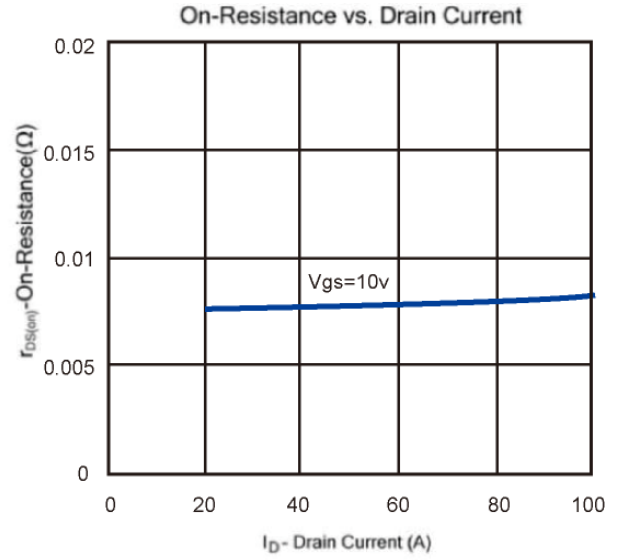
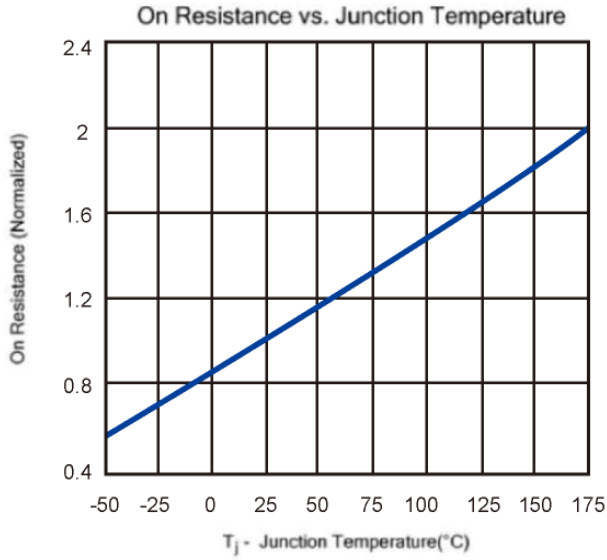
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	75			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	2.0		4.0	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} =±25V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =75V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance*	V _{GS} =10V, I _D =40A		8	10	mΩ
V _{SD}	Diode Forward Voltage *	I _S =40A, V _{GS} =0V		0.9	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DD} =60V, V _{GS} =10V, I _D =75A		137		nC
Q _g	Total Gate Charge	V _{DD} =60V, V _{GS} =4.5V, I _D =75A		27.9		
Q _{gs}	Gate-Source Charge			36.2		
Q _{gd}	Gate-Drain Charge			52.1		
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		1		Ω
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz		6160		pF
C _{oss}	Output Capacitance			435		
C _{rss}	Reverse Transfer Capacitance			146		
t _{d(on)}	Turn-On Delay Time	V _{GS} =10V, R _L =15Ω V _{DD} =30V, R _G =10Ω		63.6		ns
t _r	Turn-On Rise Time			40.8		
t _{d(off)}	Turn-Off Delay Time			167		
t _f	Turn-Off Fall Time			47.7		

Notes: a. pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

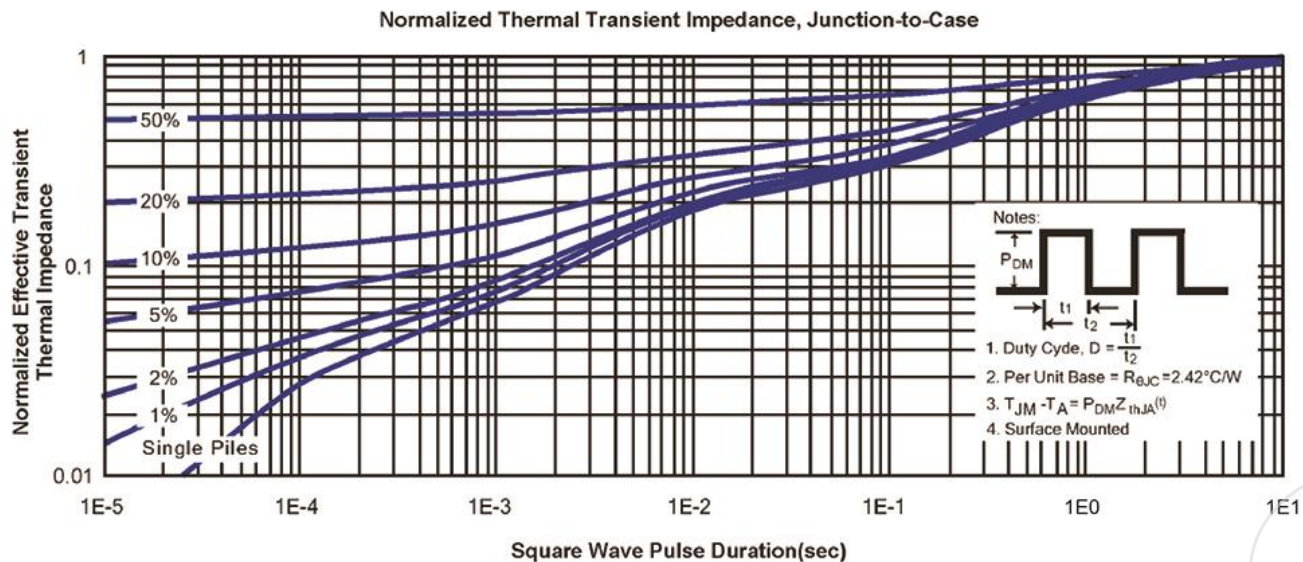
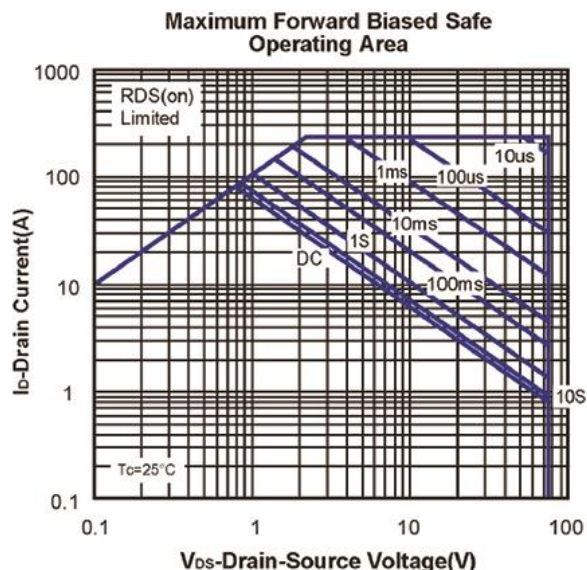
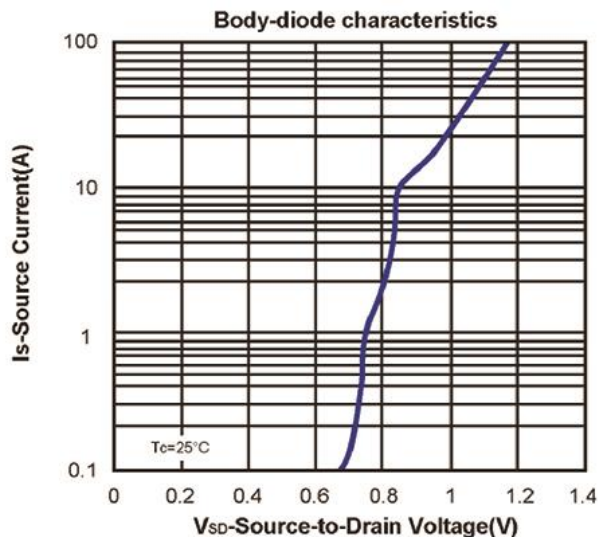
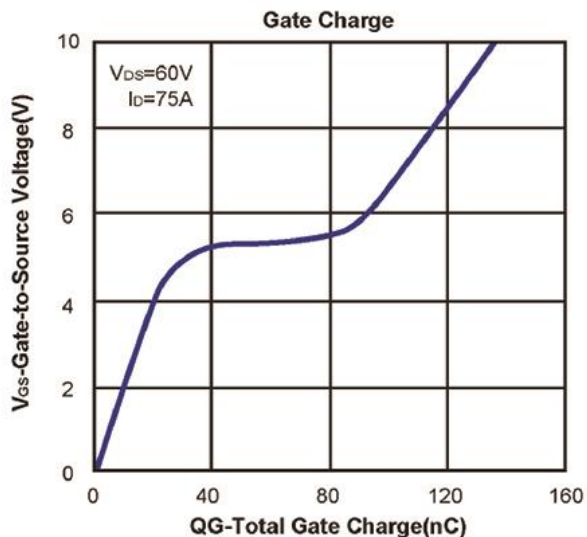
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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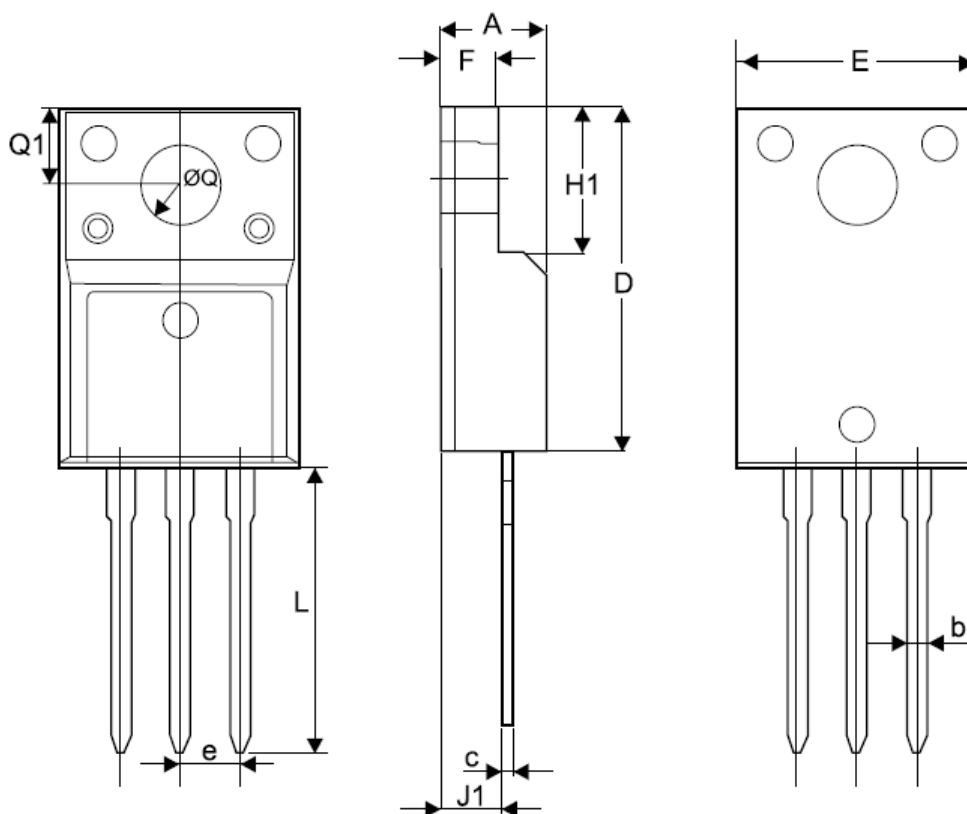
Typical Characteristics (T_J =25°C Noted)



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Typical Characteristics (T_J = 25°C Noted)



TO-220F Package Outline



Symbol	MILLIMETERS(mm)	
	MIN	MAX
A	4.40	5.00
b	0.60	1.00
C	0.30	0.70
D	15.40	16.40
E	6.96	10.46
F	2.30	2.80
e	2.54 TYP	
H1	6.40	7.00
J1	2.45	3.05
L	12.28	13.68
ØQ	2.92	3.38
Q1	3.05	3.55