ME8205E/ME8205E-G

Dual N-Channel 20V (D-S) MOSFET

GENERAL DESCRIPTION

The ME8205E is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 22m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 23m\Omega @ V_{GS}=4.0V$
- $R_{DS(ON)} \leqq 26m\Omega @ V_{GS}=3.0V$
- $R_{DS(ON)} \leqq 29m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

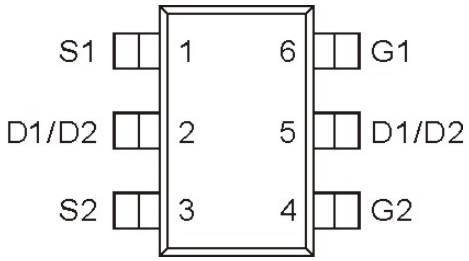
APPLICATIONS

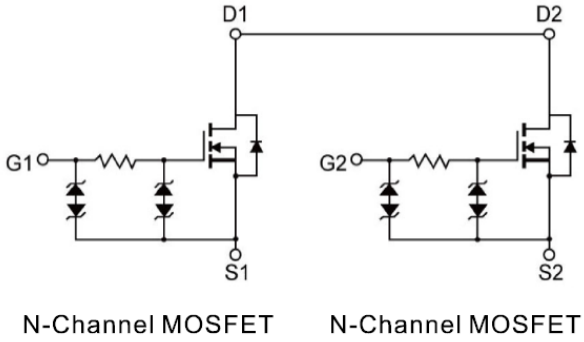
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(SOT-26)

Top View





Ordering Information:ME8205E (Pb-free)

ME8205E-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A=25℃	I_D	6	A
	T_A=70℃		4.8	
Pulsed Drain Current		I_{DM}	24	A
Maximum Power Dissipation	T_A=25℃	P_D	1.3	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	100	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

Dual N-Channel 20V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.5		1.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V			±10	μA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance [a]	V_{GS}=4.5V, I_D= 7A		15.5	22	mΩ
		V_{GS}=4V, I_D= 6.8A		16	23	
		V_{GS}=3V, I_D= 6.3A		18	26	
		V_{GS}=2.5V, I_D= 6.0A		20	29	
V_{SD}	Diode Forward Voltage	I_S=7A, V_{GS}=0V			1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=10V, I_D=6.5A		21.9		nC
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=6.5A		10.5		
Qgs	Gate-Source Charge			3.1		
Qgd	Gate-Drain Charge			2.5		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V,f=1MHz		360		pF
Coss	Output Capacitance			100		
Crss	Reverse Transfer Capacitance			31		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=10V, R_L =10Ω I_D=1A, V_{GEN}=4.5V R_G=6Ω		310		ns
t_r	Turn-On Rise Time			441		
$t_{d(off)}$	Turn-Off Delay Time			1290		
t_f	Turn-Off Fall Time			5150		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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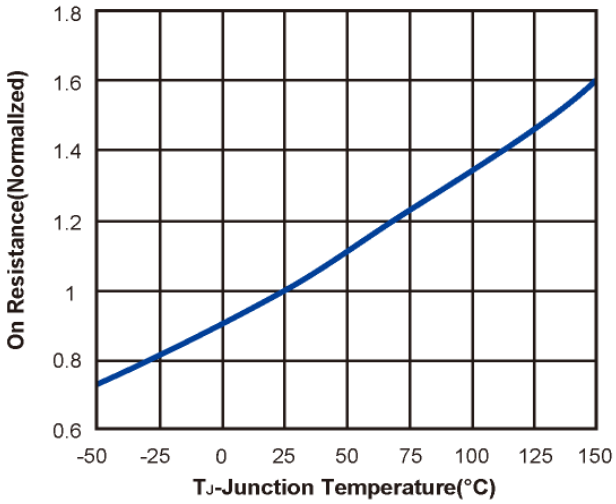
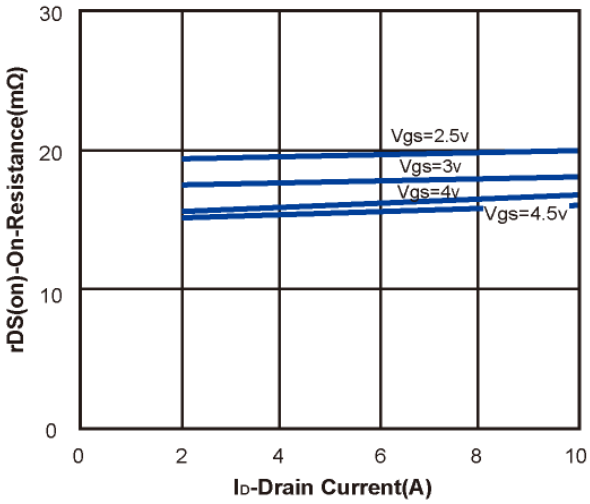
Typical Characteristics (T_J =25℃ Noted)

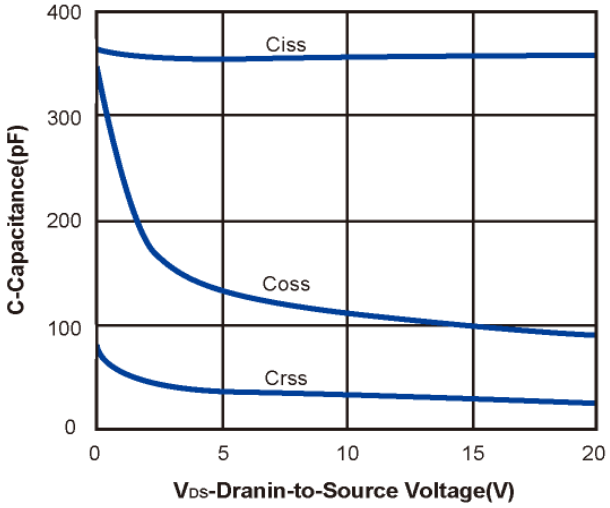
On Resistance vs. Junction Temperature



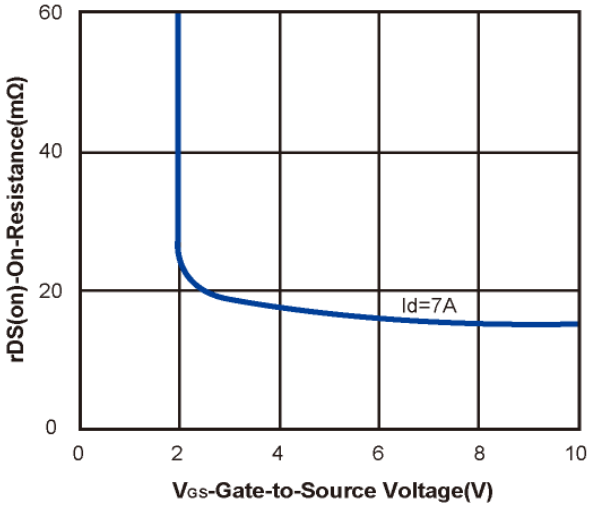
On Resistance vs. Drain Current



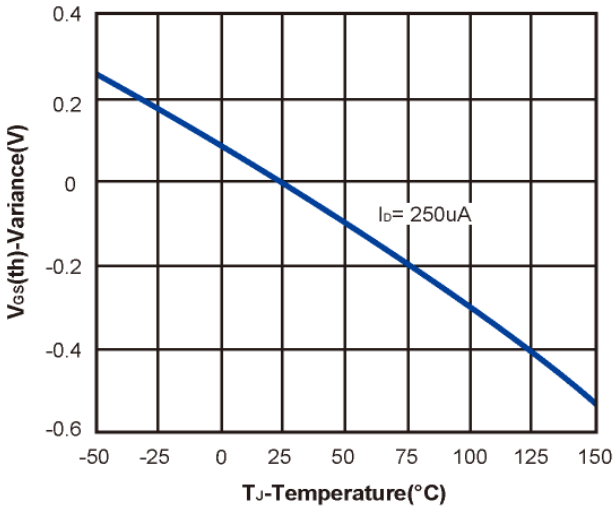
Capacitance



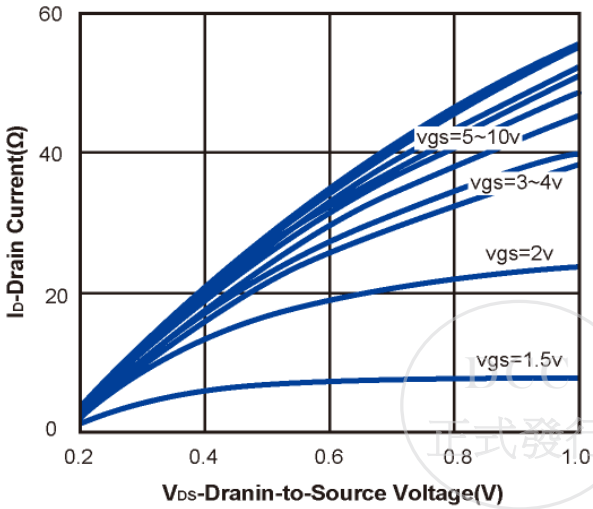
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



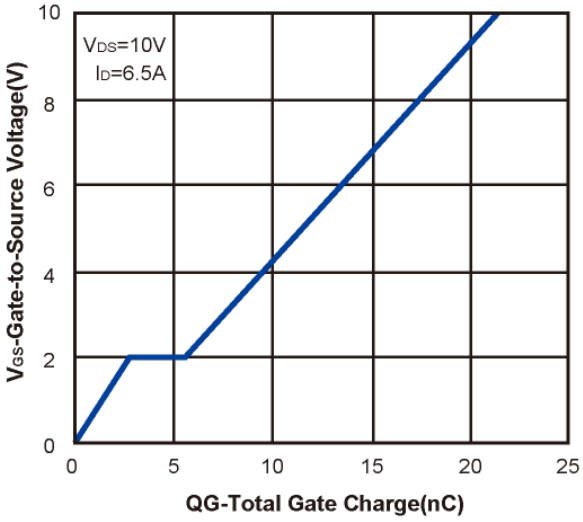
On-Region Characteristics



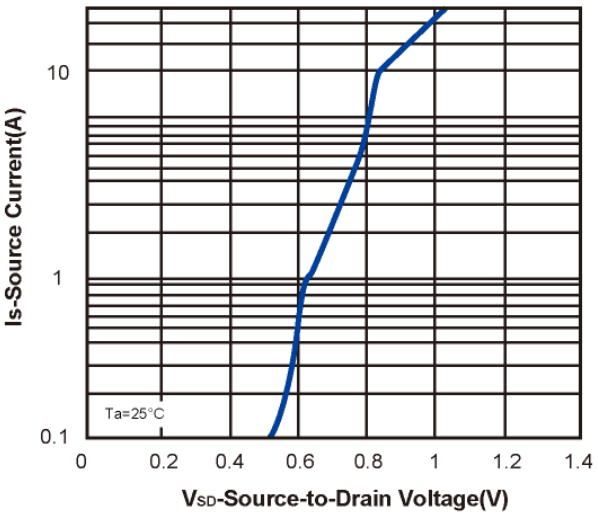
Dual N-Channel 20V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

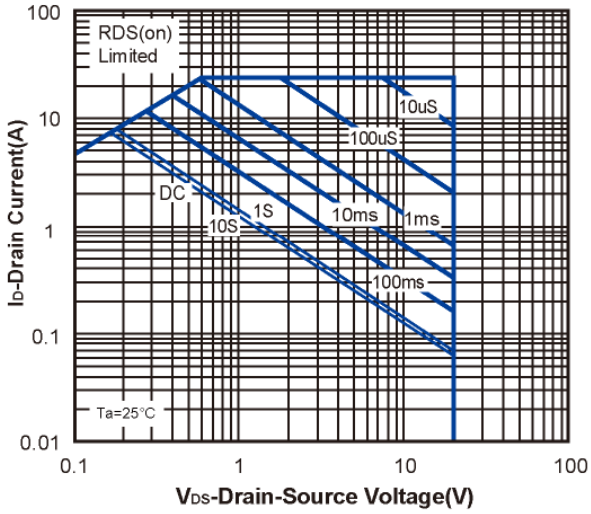
Gate Charge



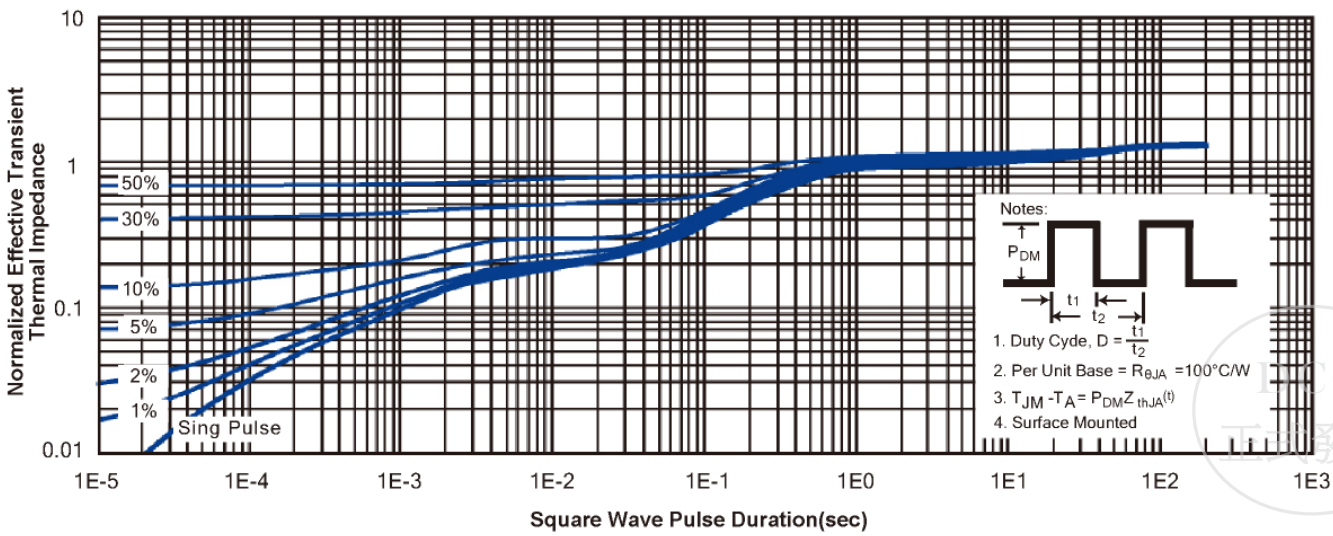
Body-diode characteristics



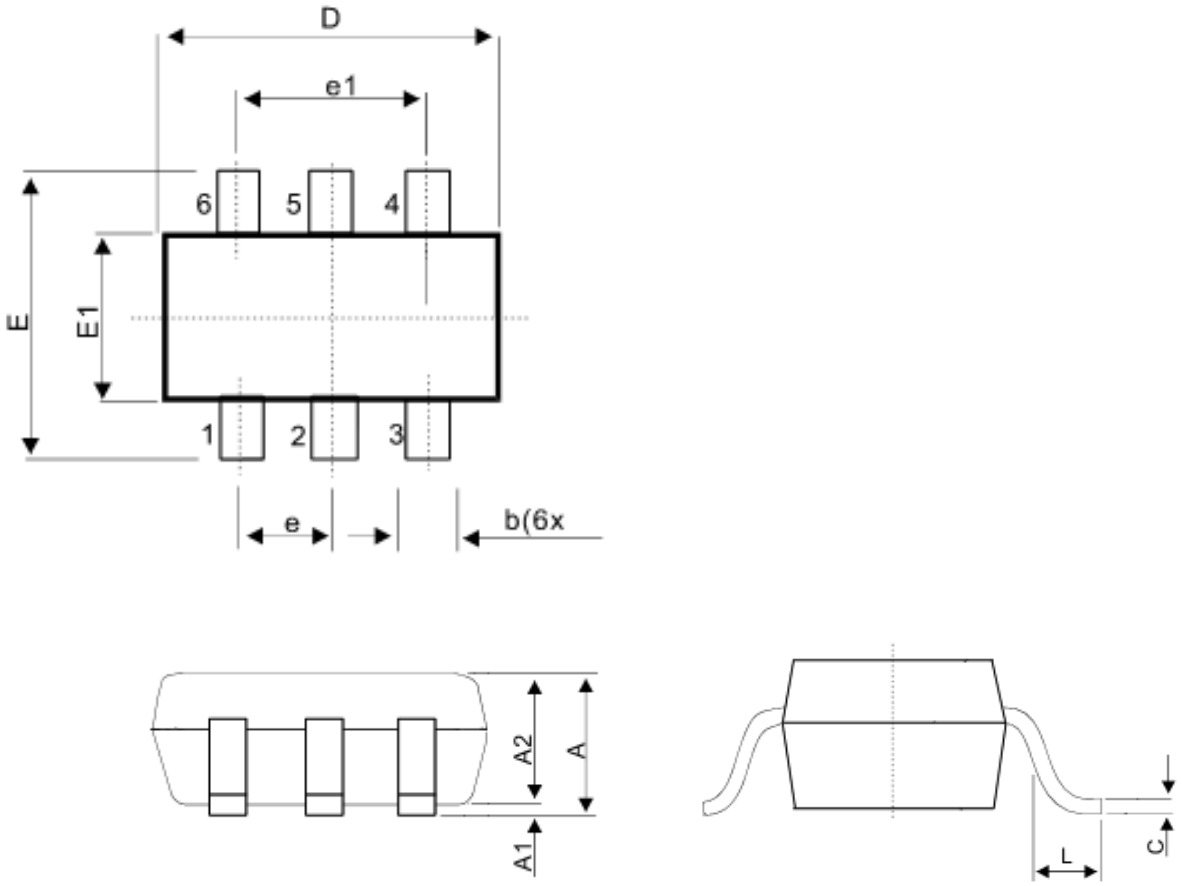
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-26 Package Outline



SYMBOL	MILLIMETERS (mm)	
	MIN	MAX
A	0.90	1.20
A1	0.01	0.10
A2	0.90	1.15
b	0.25	0.50
C	0.10	0.20
D	2.80	3.10
E	2.60	3.00
E1	1.50	1.70
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60