ME90P03/ME90P03-G

30V P-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The ME90P03 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 6.2m\Omega @ V_{GS}=-20V$
- $R_{DS(ON)} \leqq 7.6m\Omega @ V_{GS}=-10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

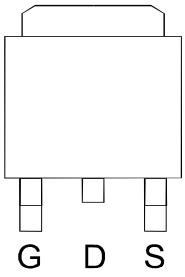
APPLICATIONS

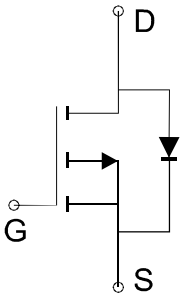
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

(TO-252)

Top View





Ordering Information: ME90P03 (Pb-free)

ME90P03-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25°C Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	-62	A
	T_C=75°C		-50	
Pulsed Drain Current		I_{DM}	-247	A
Maximum Power Dissipation	T_C=25°C	P_D	38	W
	T_C=70°C		24	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Thermal Resistance-Junction to Case		$R_{\theta JC}$	3.3	°C/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1		-3	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-20V, I_D=-20A		5.2	6.2	mΩ
		V_{GS}=-10V, I_D=-20A		6	7.6	
V_{SD}	Diode Forward Voltage	I_S=-20A, V_{GS}=0V		-0.7	-1.2	V
DYNAMIC						
Qg	Total Gate Charge (-10V)	V_{DS}=-15V, V_{GS}=-10V, I_D=-20A		102		nC
Qg	Total Gate Charge (-4.5V)			51		
Qgs	Gate-Source Charge			20		
Qgd	Gate-Drain Charge			27		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz		4510		pF
Coss	Output Capacitance			680		
Crss	Reverse Transfer Capacitance			232		
$t_{d(on)}$	Turn-On Delay Time	R_L=15Ω, V_{GEN}=-10V, I_D=1A V_{DD}=-15V, R_G=6Ω		60		ns
t_r	Turn-On Rise Time			23		
$t_{d(off)}$	Turn-Off Delay Time			163		
t_f	Turn-Off Fall Time			42		

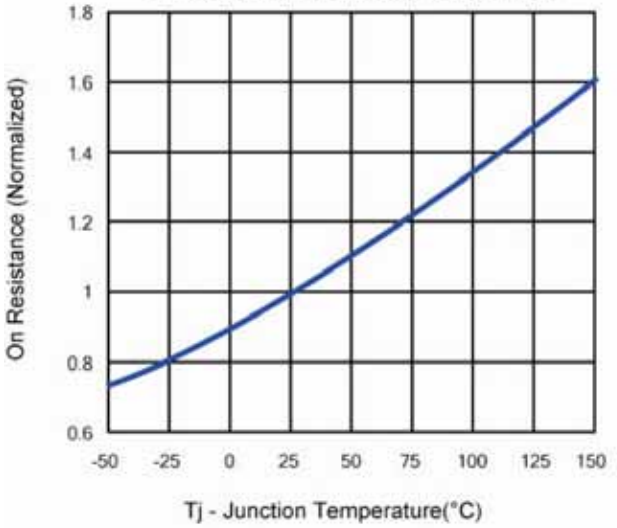
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

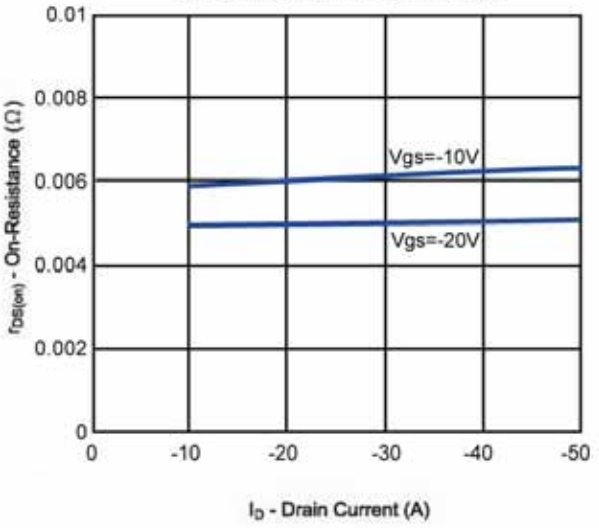
30V P-Channel Enhancement Mode MOSFET

Typical Characteristics (T_J =25℃ Noted)

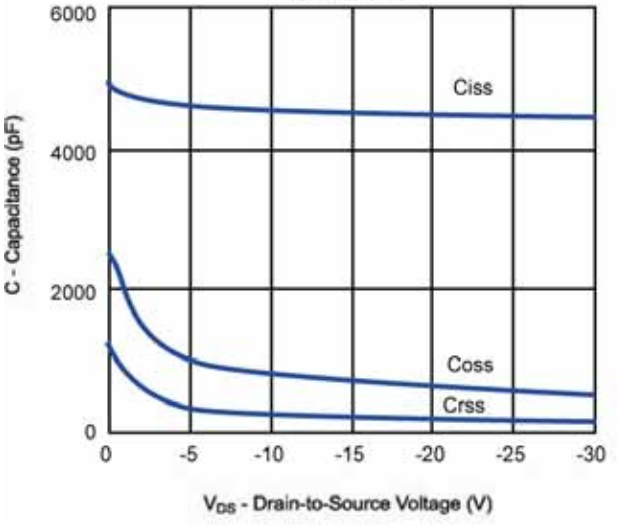
On Resistance vs. Junction Temperature



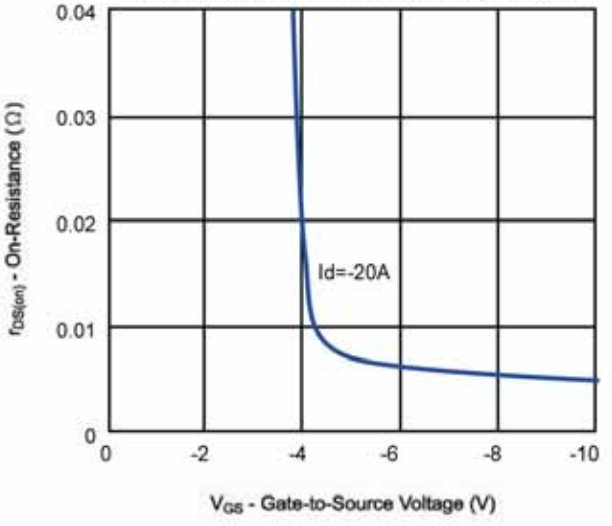
On-Resistance vs. Drain Current



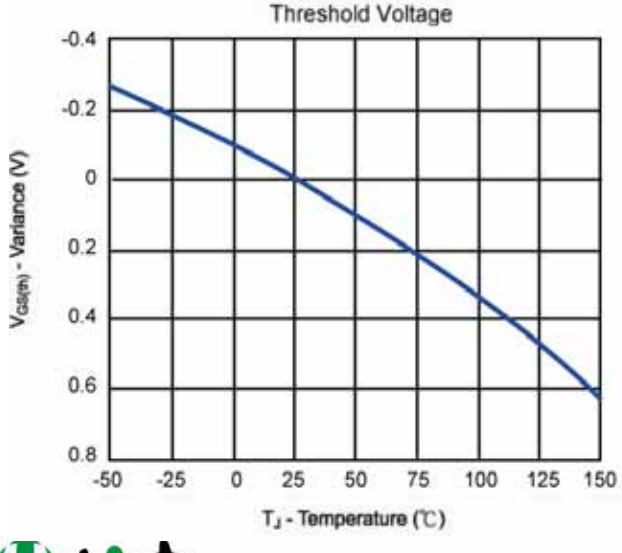
Capacitance



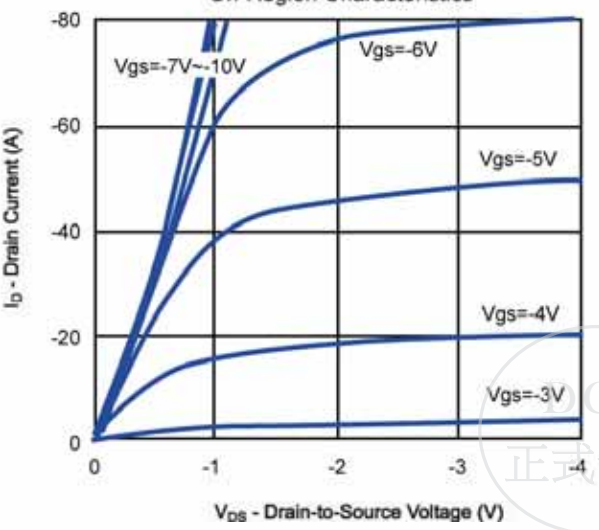
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



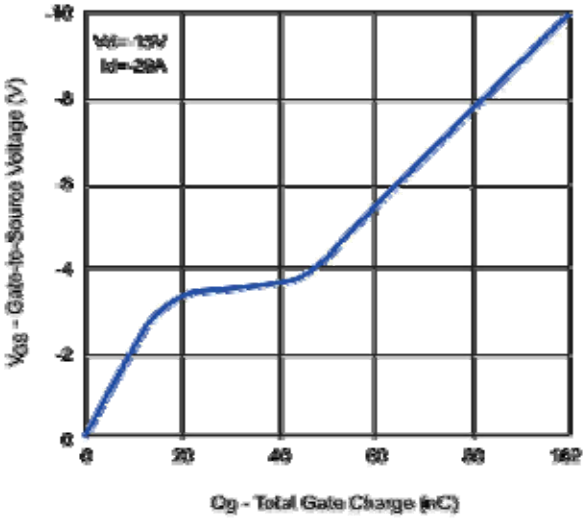
On-Region Characteristics



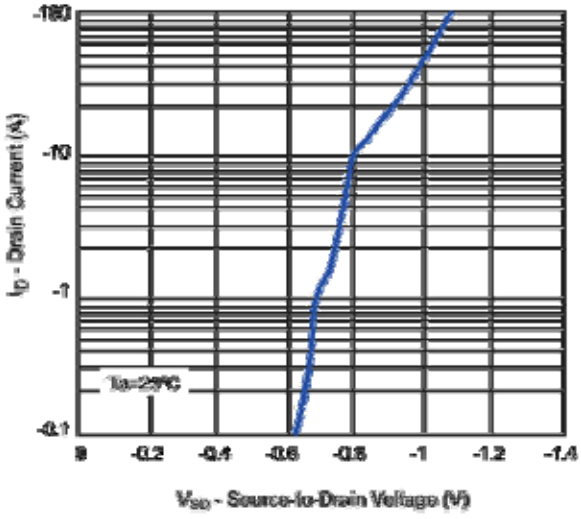
30V P-Channel Enhancement Mode MOSFET

Typical Characteristics (T_J =25℃ Noted)

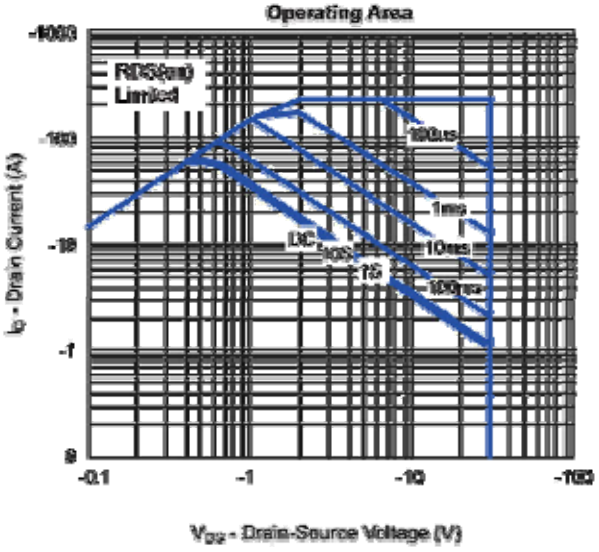
Gate Charge



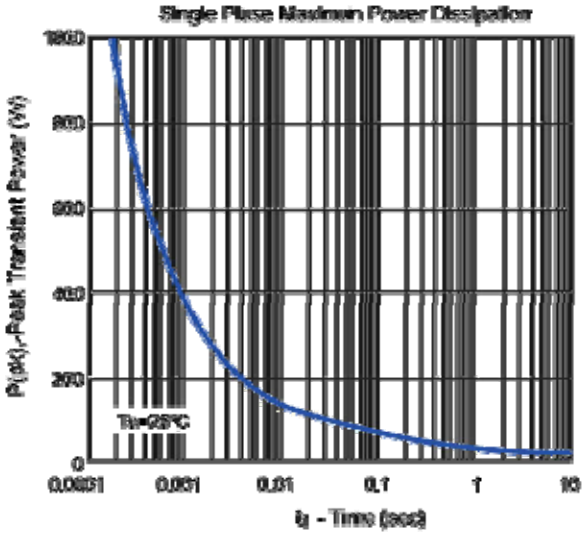
Body-diode characteristics



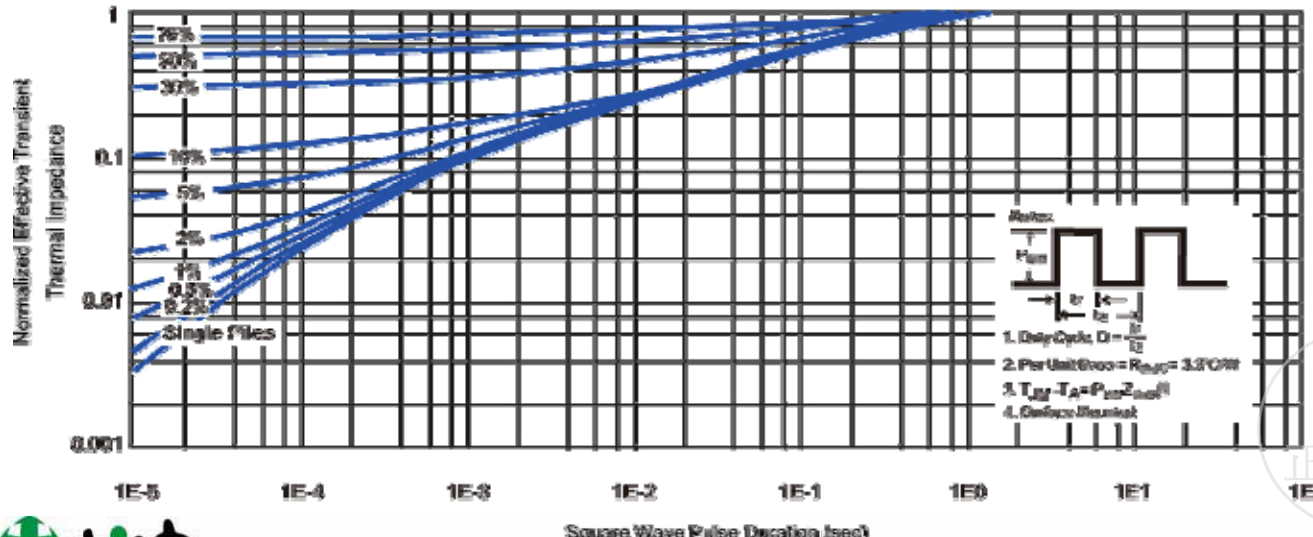
Maximum Forward Biased Safe Operating Area



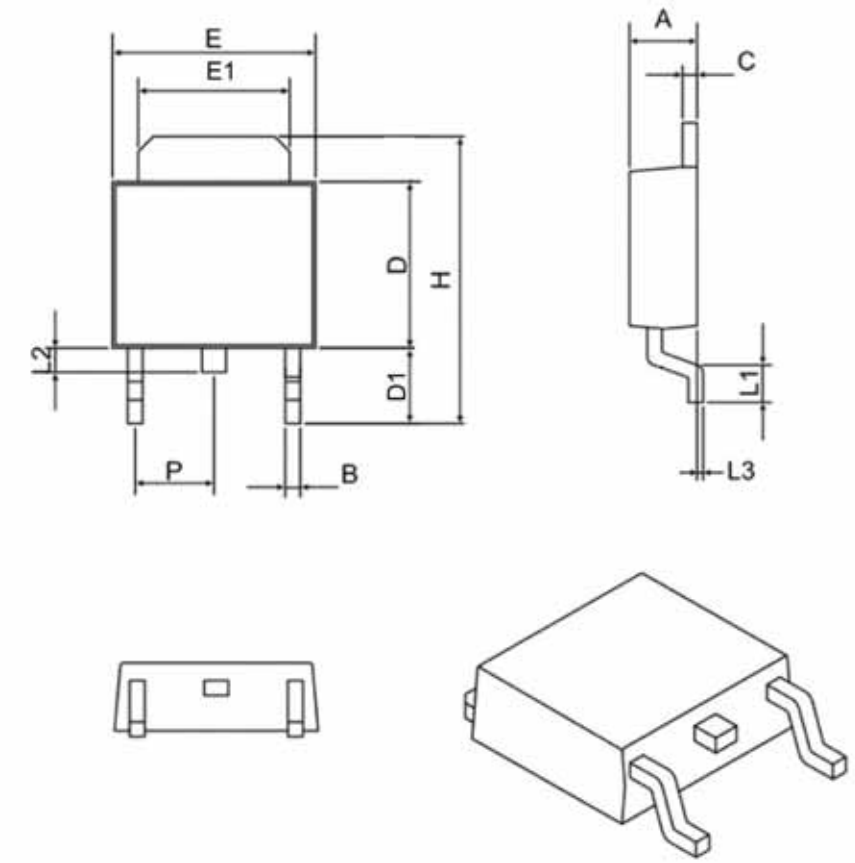
Single Pluse Maximum Power Dissipation



Normalized Thermal Transient Impedance, Junction-to-Ambient



TO-252 Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	