30V P-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The ME9435A is the P-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and lower power loss that are needed in a very small outline surface mount package.

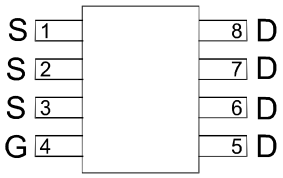
FEATURES

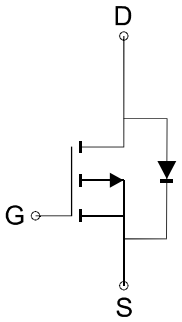
1. -30V/-5.3A, $R_{DS(ON)}$=40mΩ@V_{GS}=-10V
2. -30V/-4.2A, $R_{DS(ON)}$=60mΩ@V_{GS}=-4.5V

PIN CONFIGURATION

(SOP-8)

Top View





P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DSS}	-30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current	T_A=25℃	I_D	-5.3		A
Pulsed Drain Current [1]		I_{DM}	-20		A
Maximum Power Dissipation	T_A=25℃	P_D	2.5		W
Operating Junction Temperature		T_J	-55 to 150		℃
Junction-to-Case Thermal Resistance		$R_{\theta JC}$	28		℃/W
Junction-to-Ambient Thermal Resistance*		$R_{\theta JA}$	T≦10 sec	34	℃/W
			Steady State	62	

*The device mounted on 1in2 FR4 board with 2 oz copper

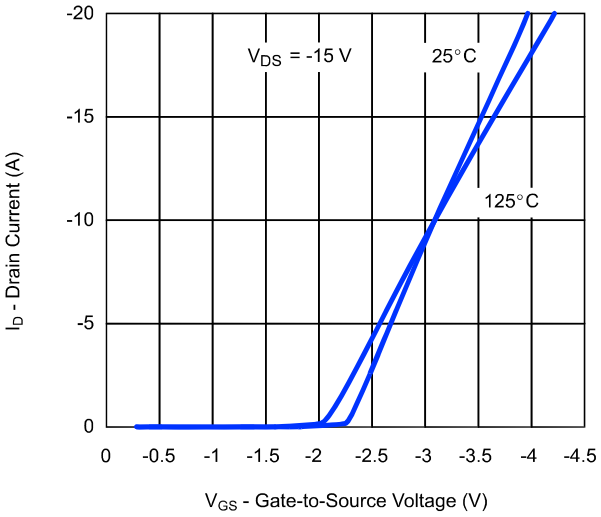
30V P-Channel Enhancement Mode MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

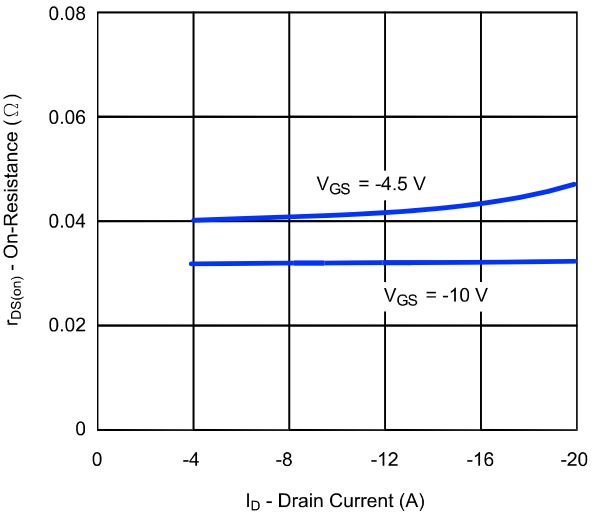
Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.0	-2.2	-3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24 V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=-10V, I_D= -5.3A		31	40	mΩ
		V_{GS}=-4.5V, I_D= -4.2A		40	60	
G_{FS}	Forward Transconductance	V_{DS}=-15, I_D=-5.3A	5	11		S
DYNAMIC						
Rg	Gate resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		5.5		Ω
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, f=1.0MHz		840	960	pF
Coss	Output Capacitance			120		
Crss	Reverse Transfer Capacitance			35		
Qg	Total Gate Charge	V_{DS}=-15V, V_{GS}=-5.3V, I_D=-10A		21	25	nC
Qgs	Gate-Source Charge			6		
Qgd	Gate-Drain Charge			5.4		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, R_L =15Ω I_D=-1A, V_{GEN}=-10V R_G=6Ω		32	40	ns
tr	Turn-On Rise Time			13	16	
$t_{d(off)}$	Turn-Off Delay Time			58	75	
t_f	Turn-Off Fall Time			6	9	

Typical Characteristics (T_J =25℃ Noted)

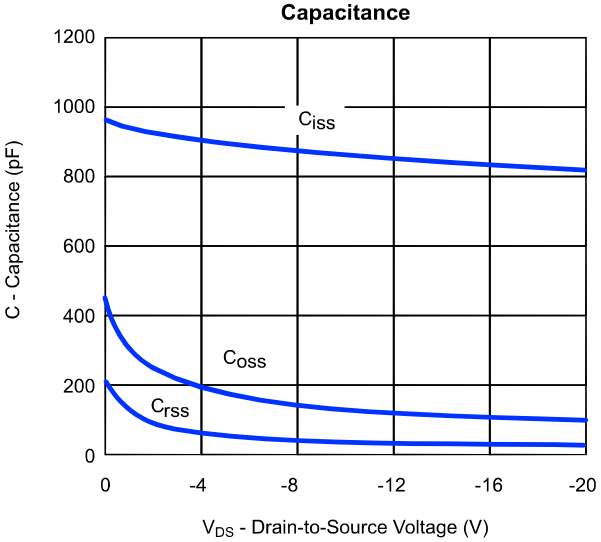
Transfer Characteristics



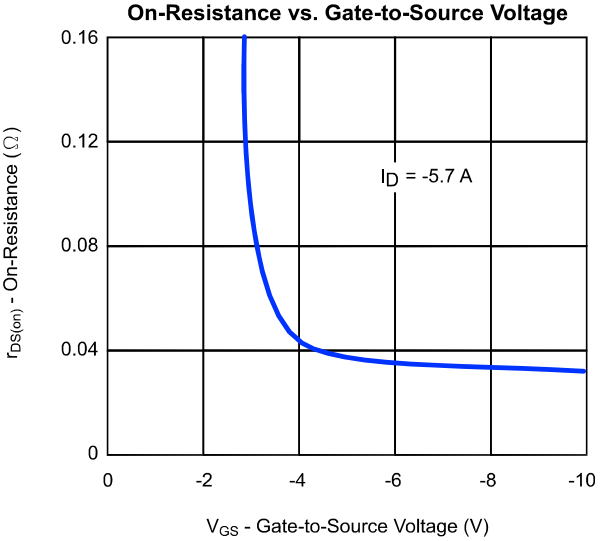
On-Resistance vs. Drain Current



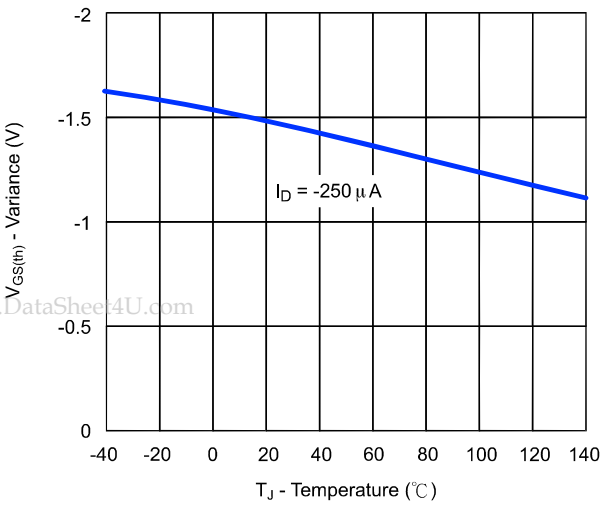
Capacitance



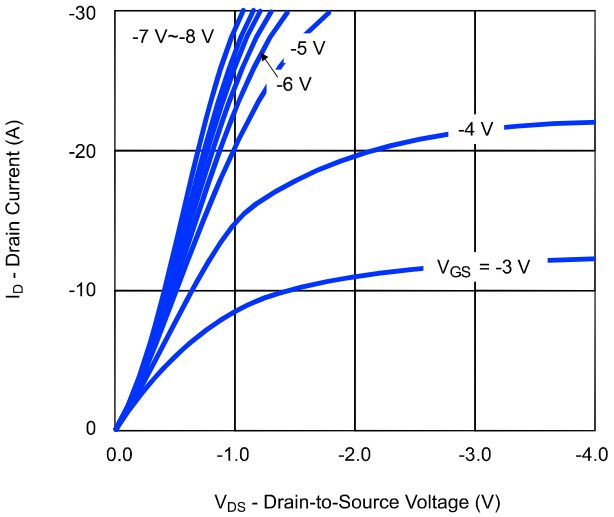
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

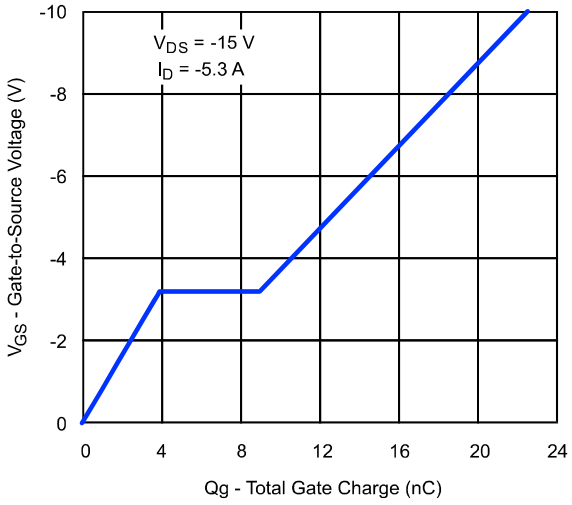


On-Region Characteristics

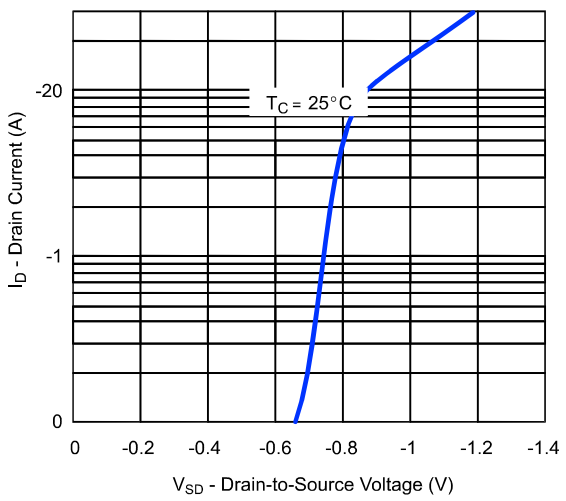


Typical Characteristics (T_J =25℃ Noted)

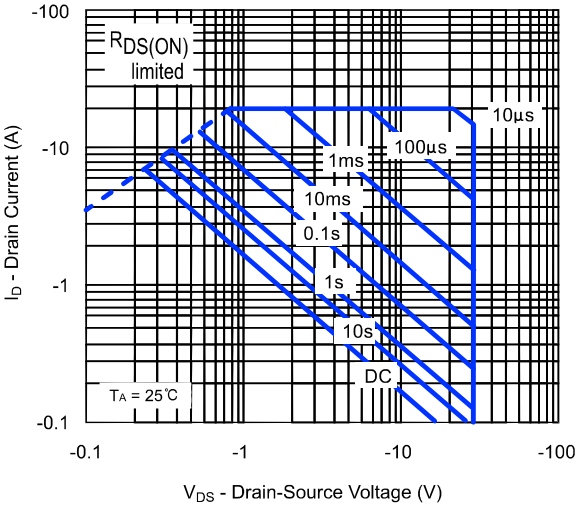
Gate Charge



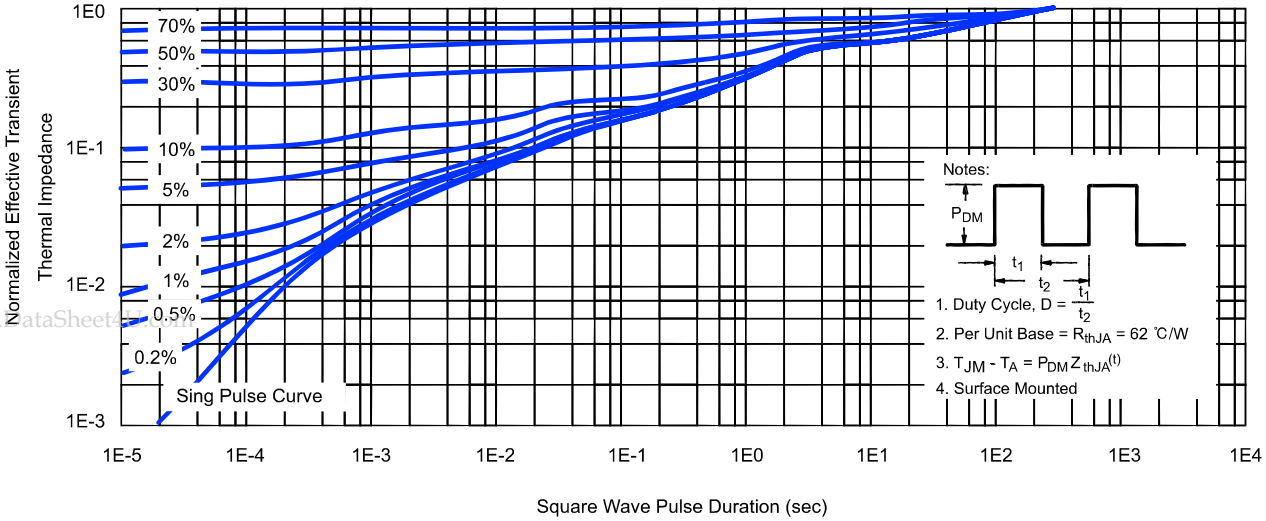
On-Resistance vs. Drain Current



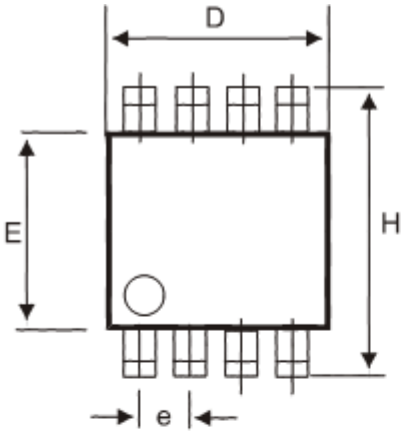
Maximum Forward Biased Safe Operating Area

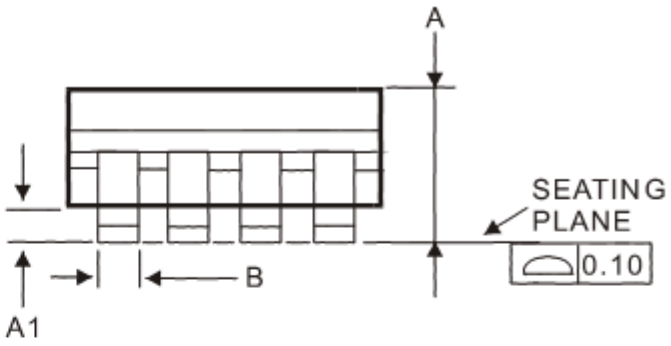


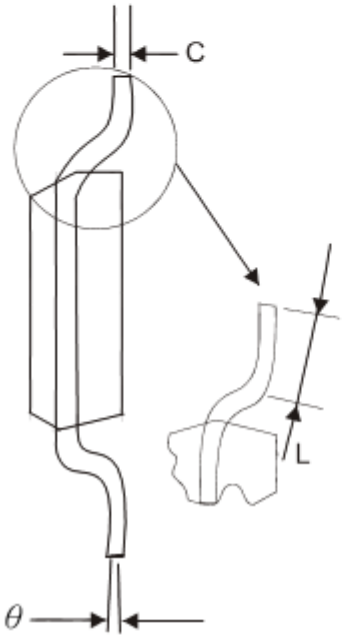
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°