30V P-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The ME9435 is the P-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and in-lin power loss that are needed in a very small outline surface mount package.

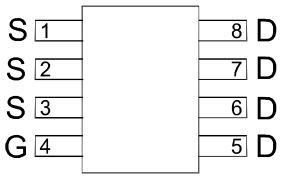
FEATURES

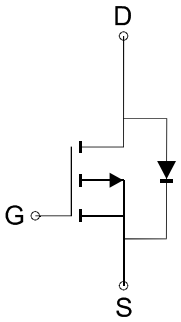
1. -30V/-5.3A, $R_{DS(ON)}$=60mΩ@V_{GS}=-10V
2. -30V/-4.2A, $R_{DS(ON)}$=100mΩ@V_{GS}=-4.5V

PIN CONFIGURATION

(SOP-8)

Top View





P-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DSS}	-30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current	T_A=25℃	I_D	-5.3		A
Pulsed Drain Current [1]		I_{DM}	-20		A
Maximum Power Dissipation	T_A=25℃	P_D	2.5		W
Operating Junction Temperature		T_J	-55 to 150		℃
Junction-to-Case Thermal Resistance		$R_{\theta JC}$	30		℃/W
Junction-to-Ambient Thermal Resistance (PCB mounted) [2]		$R_{\theta JA}$	50		℃/W

Notes: 1. Maximum DC current limited by the package; 2. 1-in^2 2oz PCB board

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.0	-2.2	-3.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24 V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=-10V, I_D= -5.3A		50	65	mΩ
		V_{GS}=-4.5V, I_D= -4.2A		90	110	
G_{FS}	Forward Transconductance	V_{DS}=-15, I_D=-5.3A	4	7		S
DYNAMIC						
Rg	Gate resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		3.5		Ω
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, f=1.0MHz		450	490	`pF
Coss	Output Capacitance			70		
Crss	Reverse Transfer Capacitance			20		
Qg	Total Gate Charge	V_{DS}=-15V, V_{GS}=-10V, I_D=-5.3A		12	15	nC
Qgs	Gate-Source Charge			2.7		
Qgd	Gate-Drain Charge			3.7		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V, R_L =15Ω I_D=-1A, V_{GEN}=-10V R_G=6Ω		35	44	ns
t_r	Turn-On Rise Time			18	22	
$t_{d(off)}$	Turn-Off Delay Time			37	46	
t_f	Turn-Off Fall Time			3.5	5	

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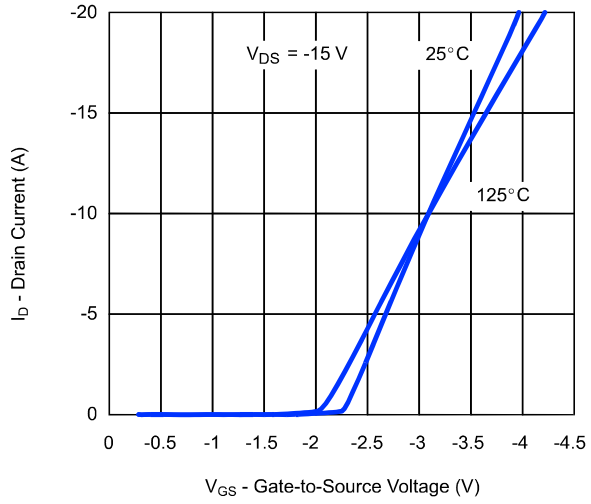
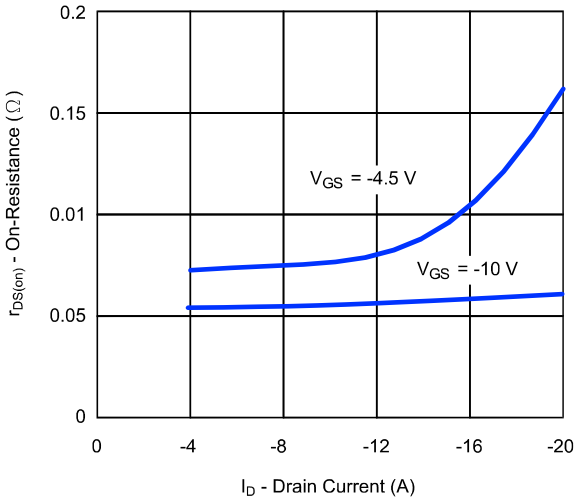
Typical Characteristics (T_J =25℃ Noted)

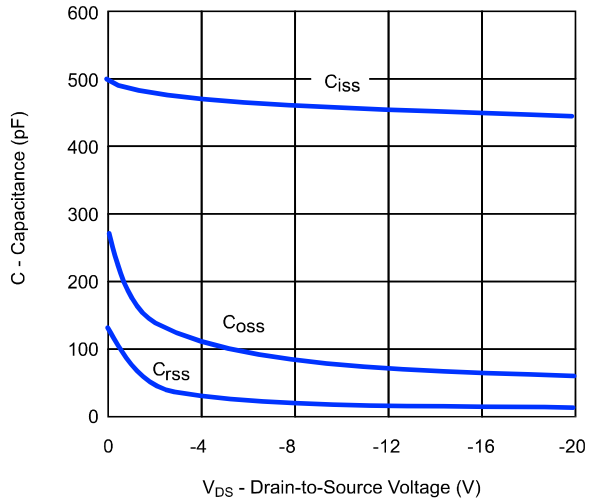
Transfer Characteristics



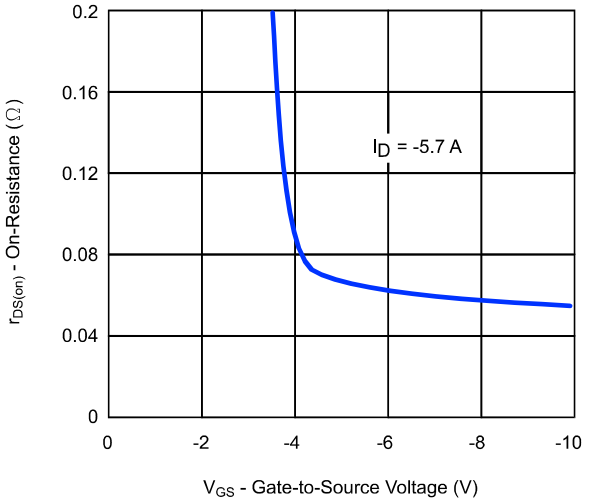
On-Resistance vs. Drain Current



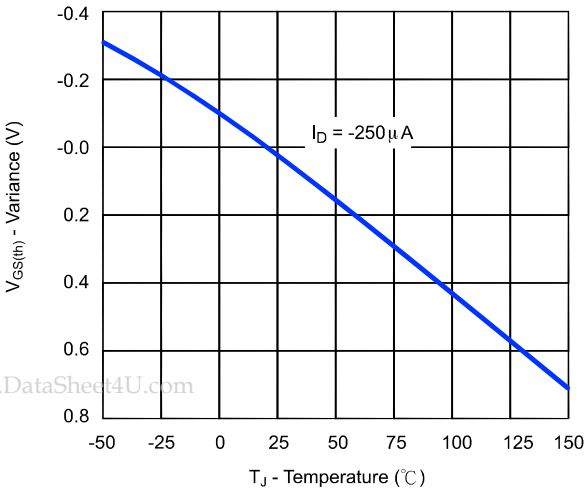
Capacitance



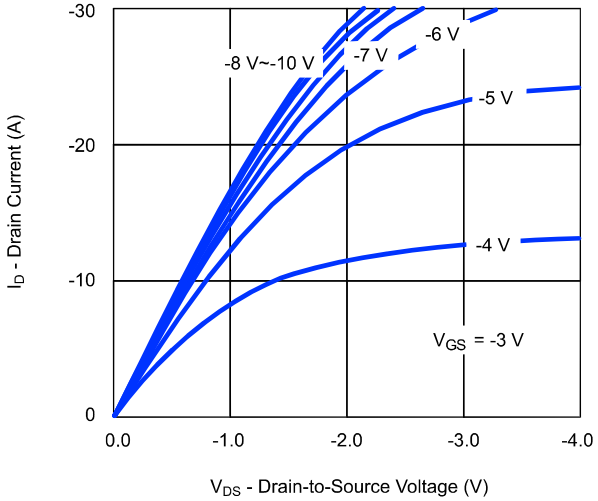
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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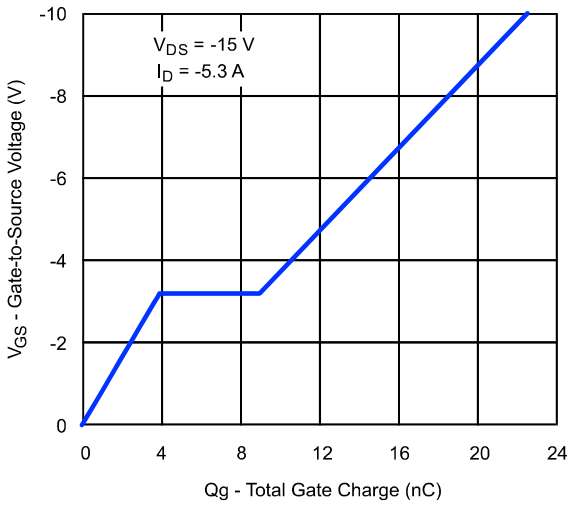
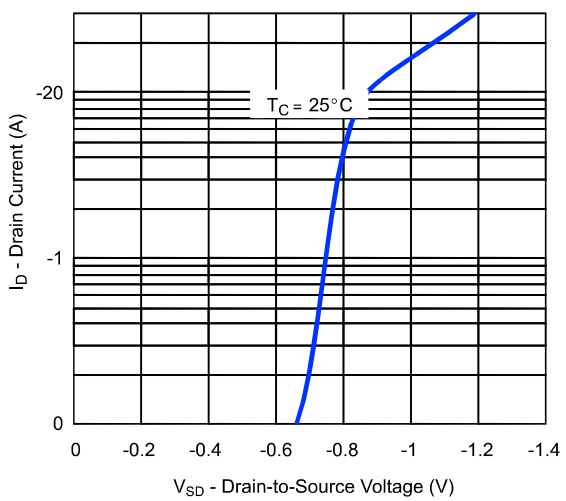
Typical Characteristics (T_J =25℃ Noted)

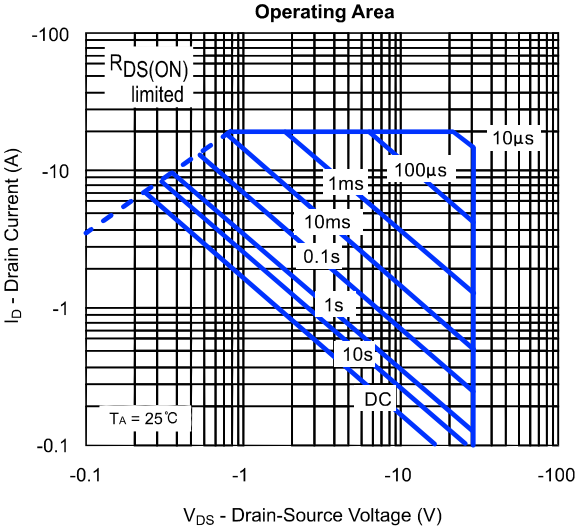
Gate Charge



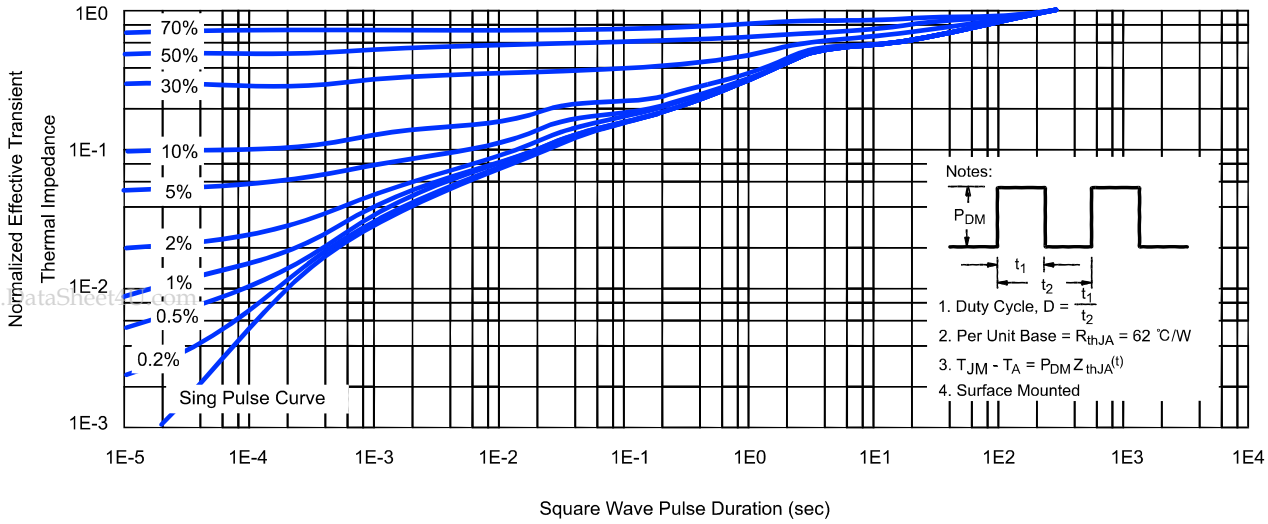
On-Resistance vs. Drain Current



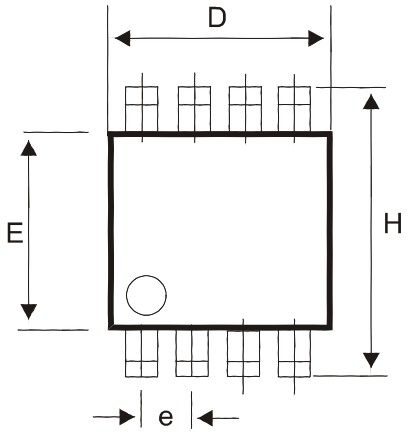
Maximum Forward Biased Safe Operating Area

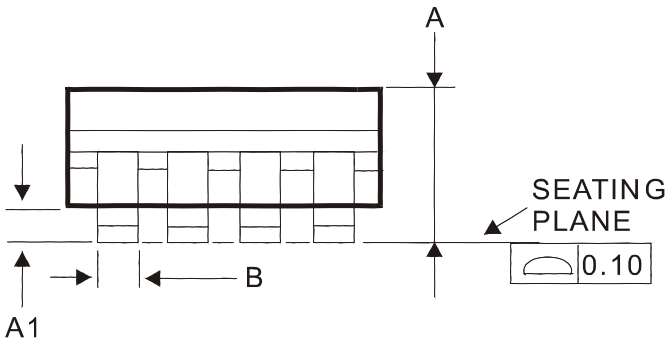


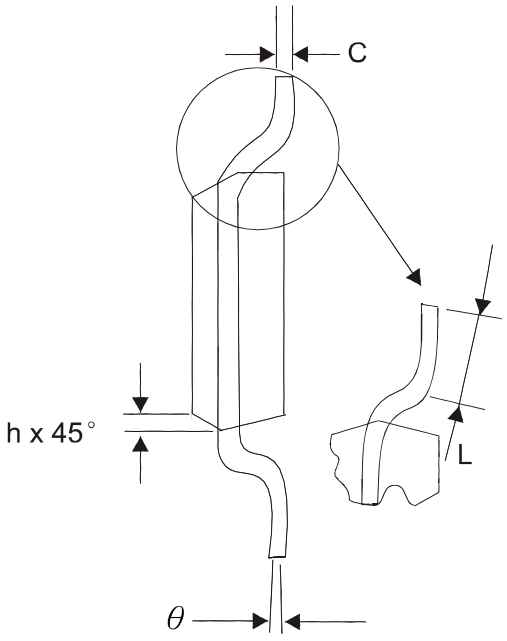
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°