N-Channel 40V(D-S) Enhancement MOSFET

GENERAL DESCRIPTION

The ME95N04 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as notebook computer power management and other battery powered circuits where Low-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 4.3m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 5.7m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

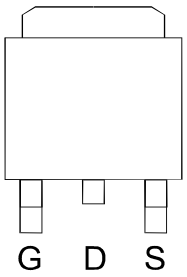
APPLICATIONS

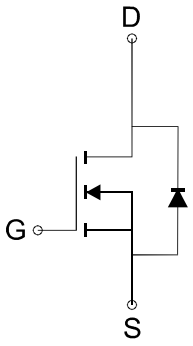
- Power Management in Note book
- NB/MB Vcore Low side switching
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

(TO-252-3L)

Top View





N-Channel MOSFET

Ordering Information: ME95N04 (Pb-free)

ME95N04-G (Green product-Halogen free)

Absolute Maximum Ratings (T_C=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current*	Tc=25℃	ID	95.3	A
	Tc=70℃		76.3	
Pulsed Drain Current		I_{DM}	381	A
Maximum Power Dissipation*	Tc=25℃	P_D	62.5	W
	Tc=70℃		40	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	2	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

N-Channel 40V(D-S) Enhancement MOSFET

Electrical Characteristics (T_J=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	40			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D=25A		3.6	4.3	mΩ
		V_{GS}=4.5V, I_D=19A		4.4	5.7	
V_{SD}	Diode Forward Voltage	I_S=25A, V_{GS}=0V		0.8	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=20A		88.9		nC
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=4.5V, I_D=20A		41.4		
Qgs	Gate-Source Charge			14.8		
Qgd	Gate-Drain Charge			16.2		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V,F=1MHz		4800		pF
Coss	Output Capacitance			327		
Crss	Reverse Transfer Capacitance			281		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L=15Ω I_D=1A, V_{GEN}=10V R_G=6Ω		27.3		ns
t_r	Turn-On Rise Time			20.2		
$t_{d(off)}$	Turn-Off Delay Time			108		
t_f	Turn-Off Fall Time			18.4		

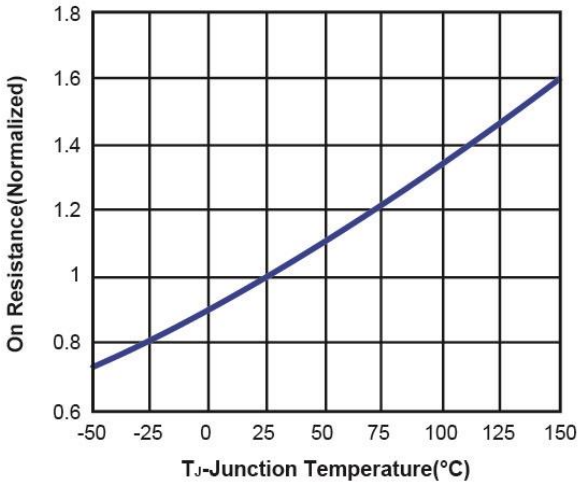
Note: a.Pulse test: pulse width≦300us, duty cycle≦2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

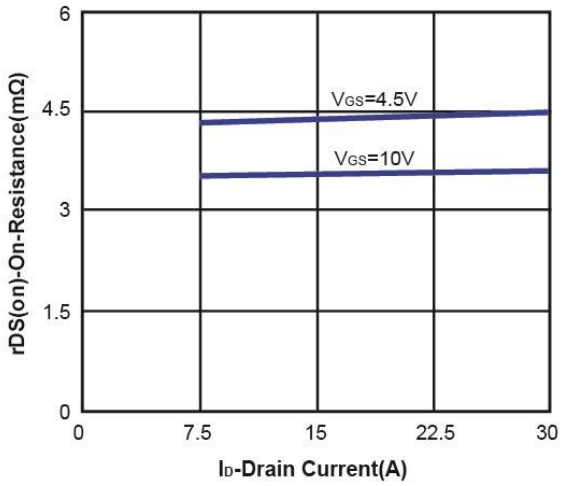
N-Channel 40V(D-S) Enhancement MOSFET

Typical Characteristics (T_J =25℃ Noted)

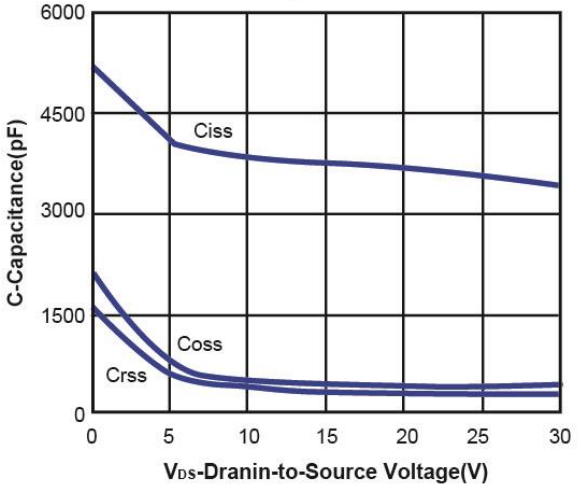
On Resistance vs. Junction Temperature



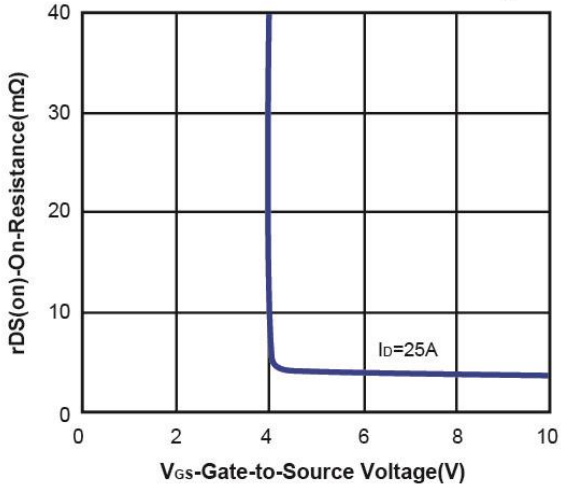
On Resistance vs. Drain Current



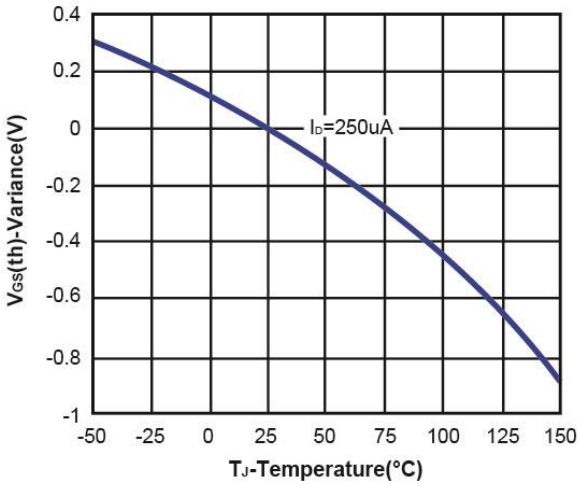
Capacitance



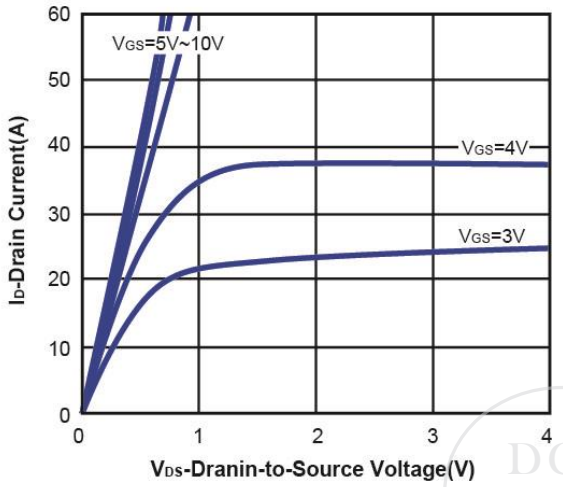
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



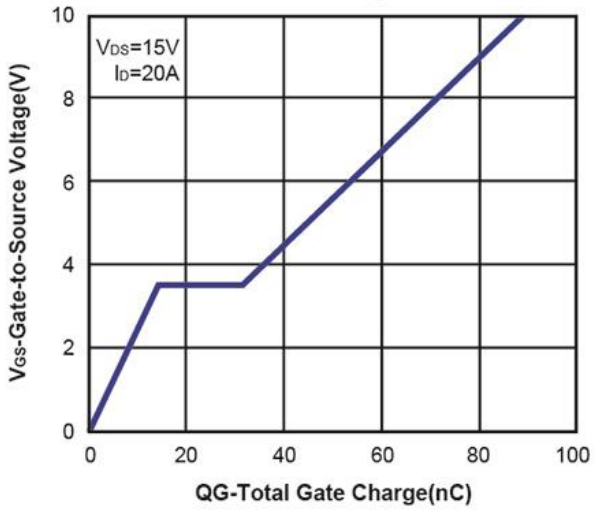
On-Region Characteristics



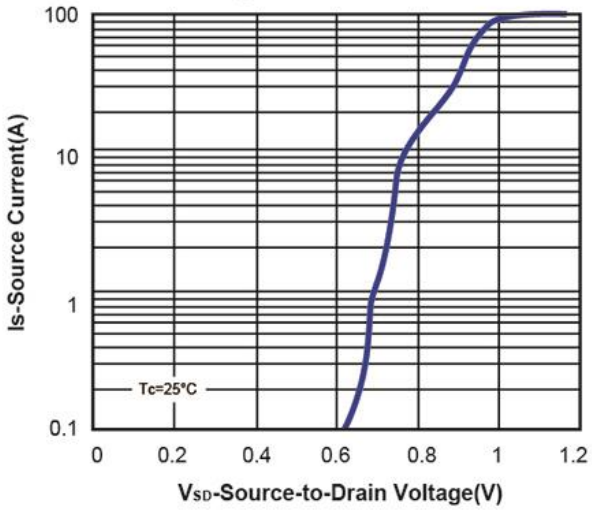
N-Channel 40V(D-S) Enhancement MOSFET

Typical Characteristics (T_J =25℃ Noted)

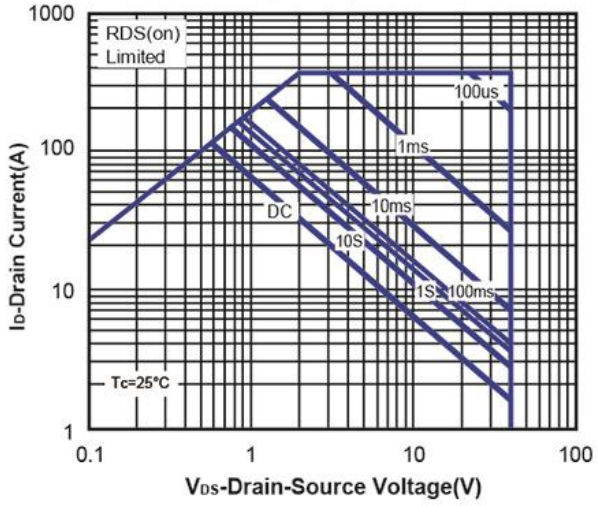
Gate Charge



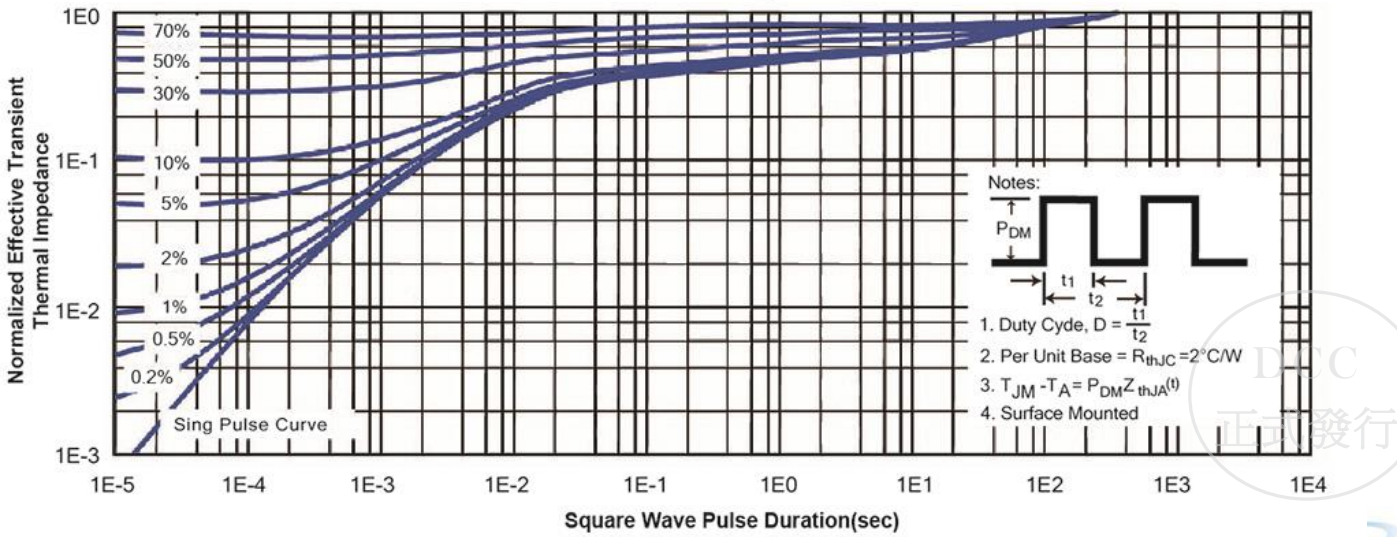
Body-diode characteristics



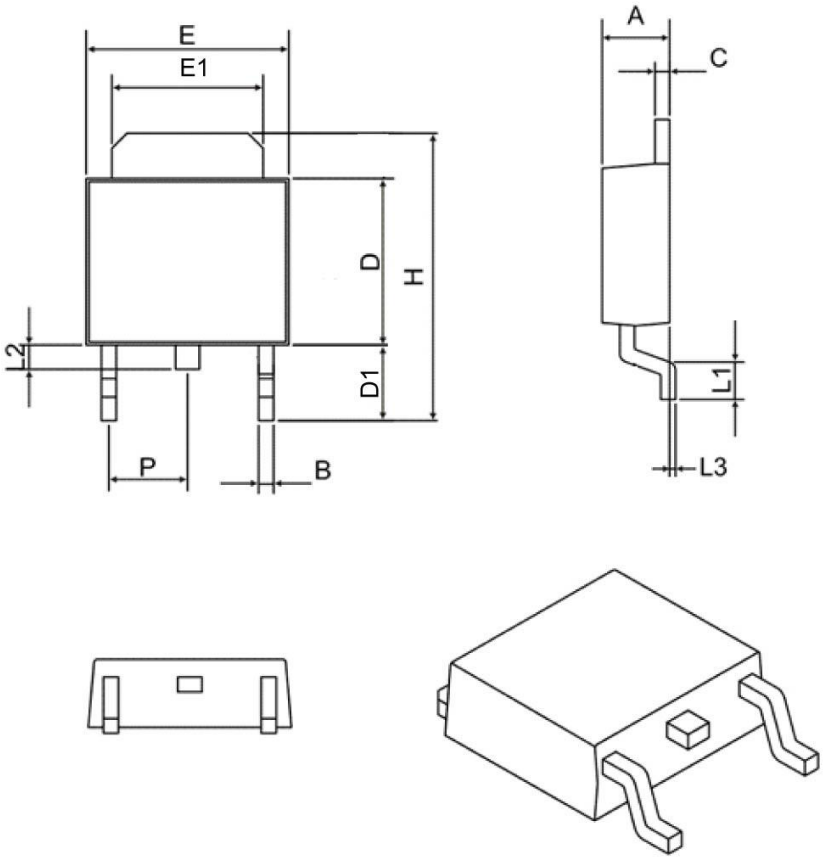
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO-252 Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	