ME95N10T/ME95N10T-G

N-Channel 100-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME95N10T is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance.

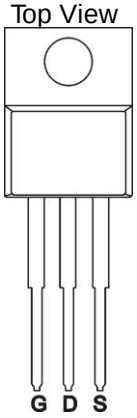
FEATURES

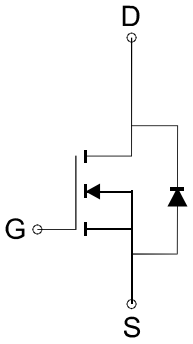
- $R_{DS(ON)} \leqq 8.5m\Omega$ @V_{GS}=10V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

PIN CONFIGURATION

(TO-220)

Top View





N-Channel MOSFET

Ordering Information: ME95N10T (Pb-free)

ME95N10T-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current*	T_C=25℃	I_D	124	A
	T_C=70℃		104	
Pulsed Drain Current		I_{DM}	496	A
Maximum Power Dissipation	T_C=25℃	P_D	300	W
	T_C=70℃		210	
Junction and Storage Temperature Range		TJ, Tstg	-55 to 175	℃
Thermal Resistance-Junction to Case**		$R_{\theta JC}$	0.5	℃/W

* Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 80A.

** The device mounted on 1in^2 FR4 board with 2 oz copper.

N-Channel 100-V (D-S) MOSFET

Electrical Characteristics (T_J =25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2		4	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D= 50A		6.5	8.5	mΩ
V_{SD}	Diode Forward Voltage	I_S=50A, V_{GS}=0V		0.87	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=50V, V_{GS}=10V, I_D=75A		212		nC
Qg	Total Gate Charge	V_{DS}=50V, V_{GS}=4.5V, I_D=75A		57		
Qgs	Gate-Source Charge			67		
Qgd	Gate-Drain Charge			50		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		12600		pF
Coss	Output Capacitance			868		
Crss	Reverse Transfer Capacitance			285		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=50V, R_L =5Ω, V_{GS}=10V, R_G=25Ω		209		ns
tr	Turn-On Rise Time			126		
$t_{d(off)}$	Turn-Off Delay Time			588		
tf	Turn-Off Fall Time			158		

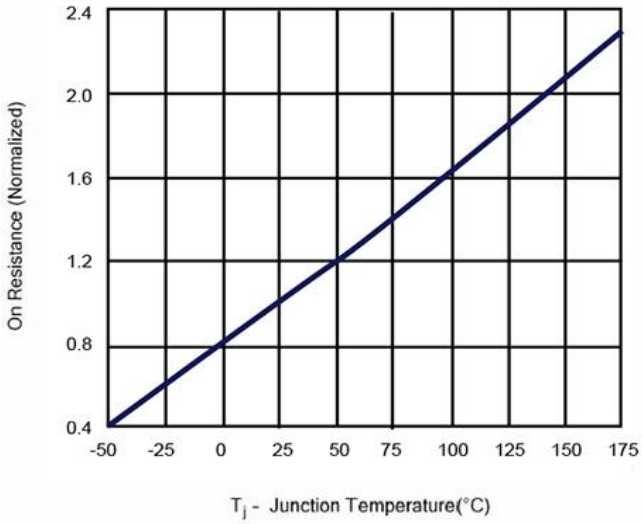
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

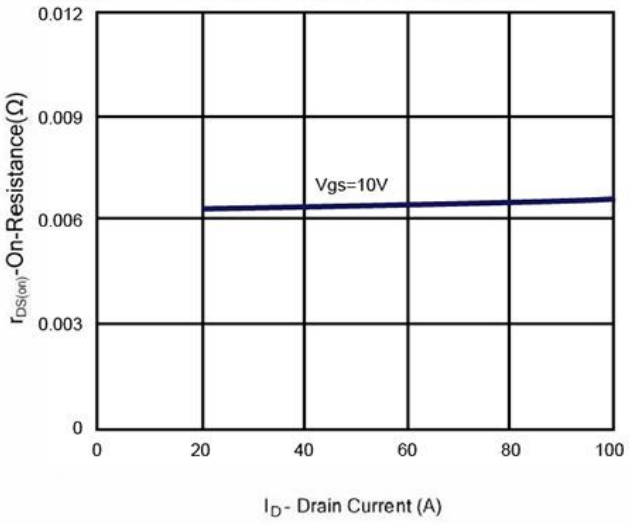
N-Channel 100-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

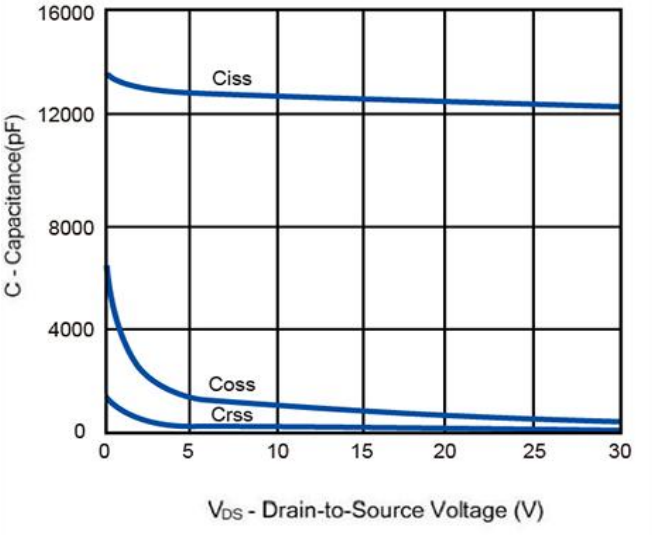
On Resistance vs. Junction Temperature



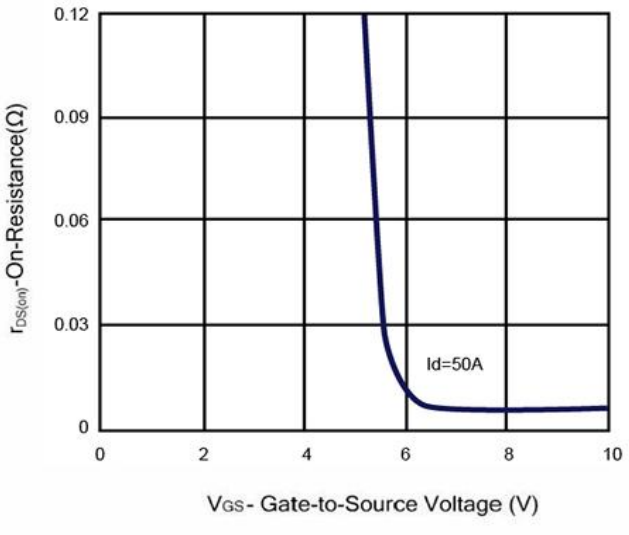
On-Resistance vs. Drain Current



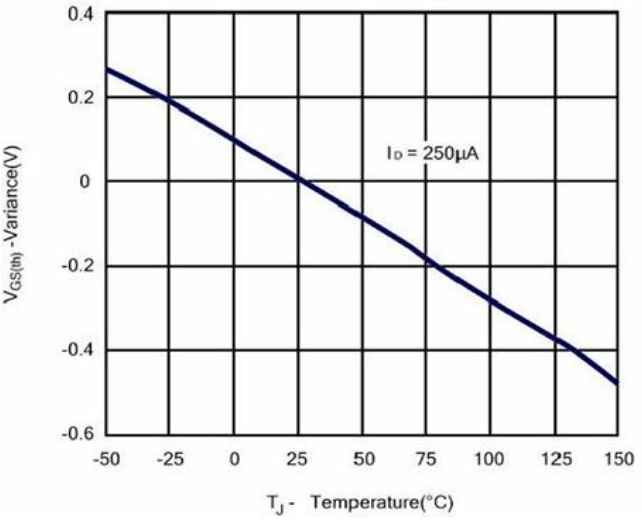
Capacitance



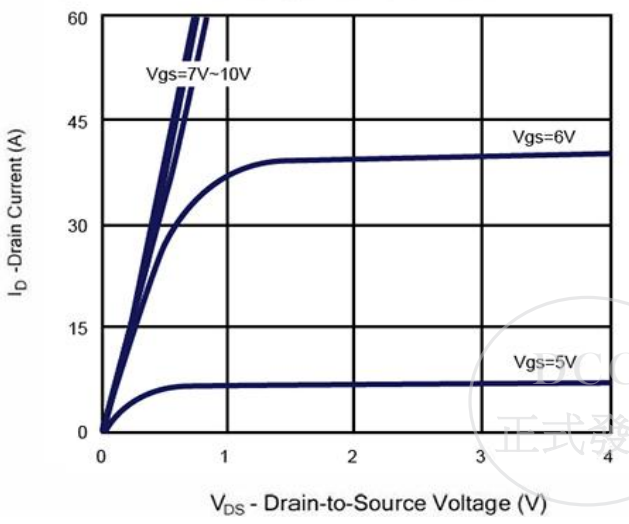
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



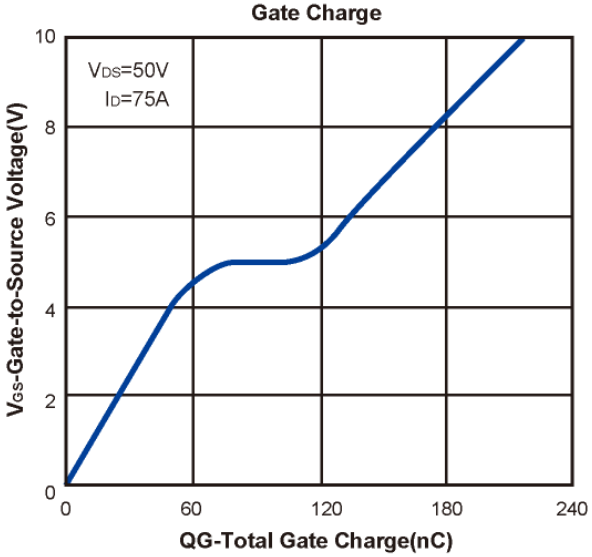
On-Region Characteristics



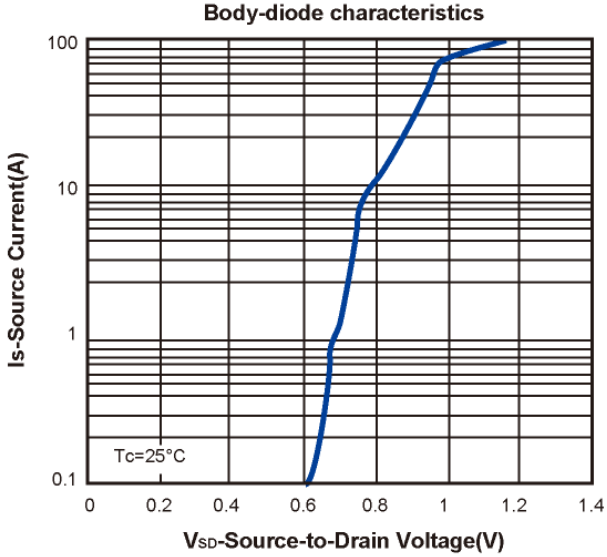
N-Channel 100-V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

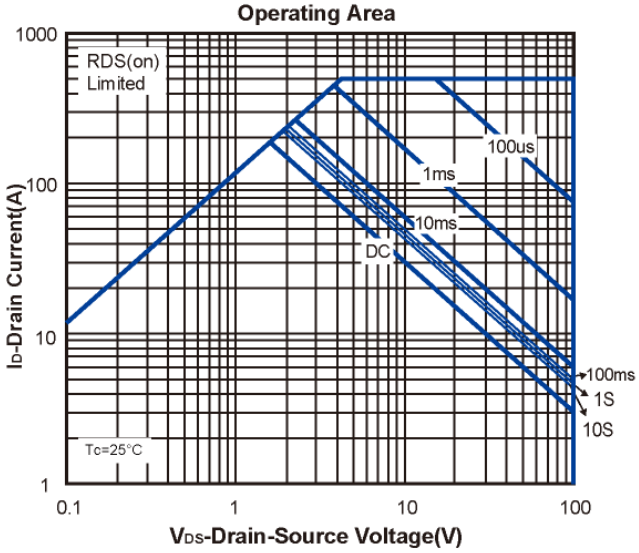
Gate Charge



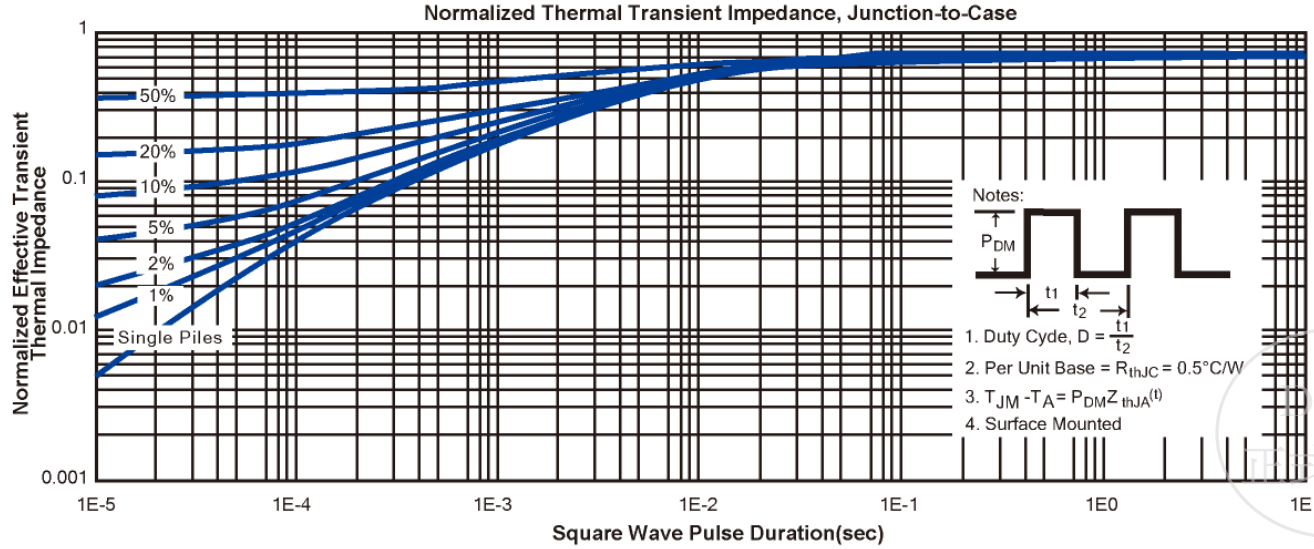
Body-diode characteristics



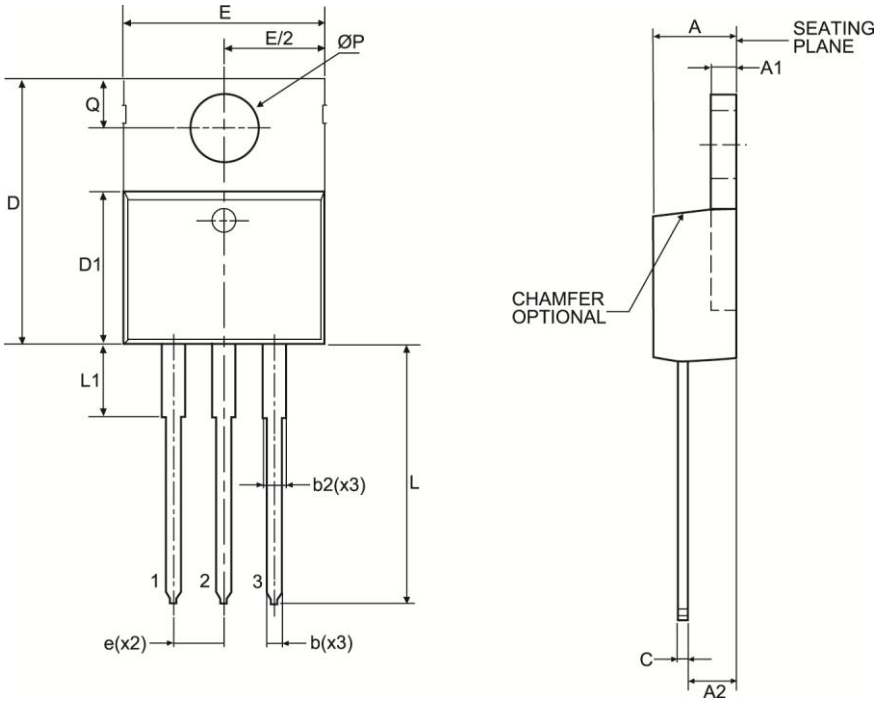
Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



TO-220 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	3.50	4.90
A1	1.00	1.40
A2	2.00	3.00
b	0.70	1.40
c	0.35	0.65
D	14.00	16.50
D1	8.30	9.50
E	9.60	10.70
e	2.54 BSC	
L	12.50	15.00
ØP	3.60 TYP	
Q	2.50	3.10
b2	1.10	1.80
L1	2.40	3.20