Dual N-Channel 20V (D-S) MOSFET

GENERAL DESCRIPTION

The ME9926 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 29m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leqq 42m\Omega @ V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

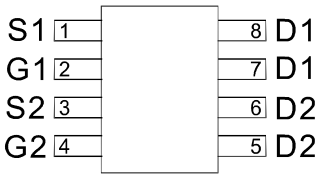
APPLICATIONS

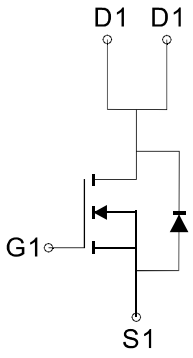
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

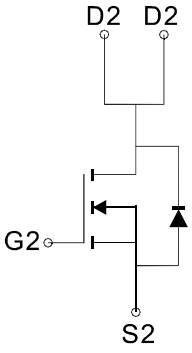
(SOP-8)

Top View





N-Channel MOSFET



N-Channel MOSFET

Ordering Information: ME9926 (Pb-free)

ME9926-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	10sec		SteadyState		Unit
Drain-Source Voltage		V_{DSS}	20				V
Gate-Source Voltage		V_{GSS}	±12				V
Continuous Drain Current*	T_A=25℃	I_D	6.6		5.2		
	T_A=70℃		5.2		4.2		A
Pulsed Drain Current		I_{DM}	30				A
Maximum Power Dissipation*	T_A=25℃	P_D	2.0		1.25		W
	T_A=70℃		1.2		0.8		
Operating Junction Temperature		T_J	-55 to 150				℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	Typ	45	Typ	80	℃/W
			Max	62.5	Max	100	

* The device mounted on 1in^2 FR4 board with 2 oz copper

Dual N-Channel 20V (D-S) MOSFET

Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0, I_D=250μA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.4		0.9	V
I_{GSS}	Gate Body Leakage	V_{DS}=0V, V_{GS}=±12V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=4.5V, I_D= 6.0A		22	29	mΩ
		V_{GS}=2.5V, I_D= 5.2A		28	42	
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.72	1.2	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5V, I_D=6.0A		8		nC
Qgs	Gate-Source Charge			2.1		
Qgd	Gate-Drain Charge			2.3		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=10V,I_D=1.0A, V_{GEN}=4.5V R_G=6Ω		14		ns
t_r	Turn-On Rise Time			17		
$t_{d(off)}$	Turn-Off Delay Time			43		
t_f	Turn-Off Fall Time			5		
Ciss	Input capacitance	V_{DS}=15V, V_{GS}=0V, f=1.0MHz		550		pF
Coss	Output Capacitance			130		
Crss	Reverse Transfer Capacitance			40		

Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

b. Matsuki reserves the right to improve product design, functions and reliability without notice.

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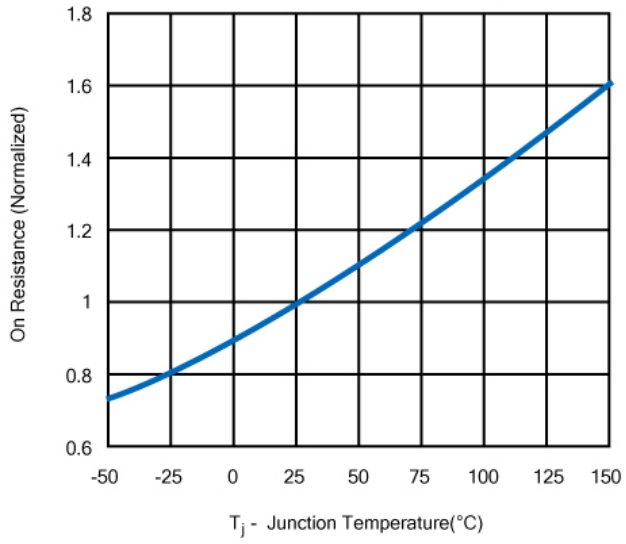
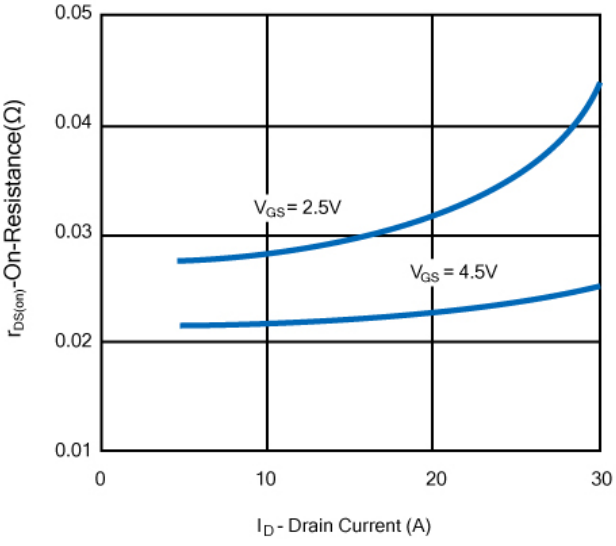
Typical Characteristics (T_J =25℃ Noted)

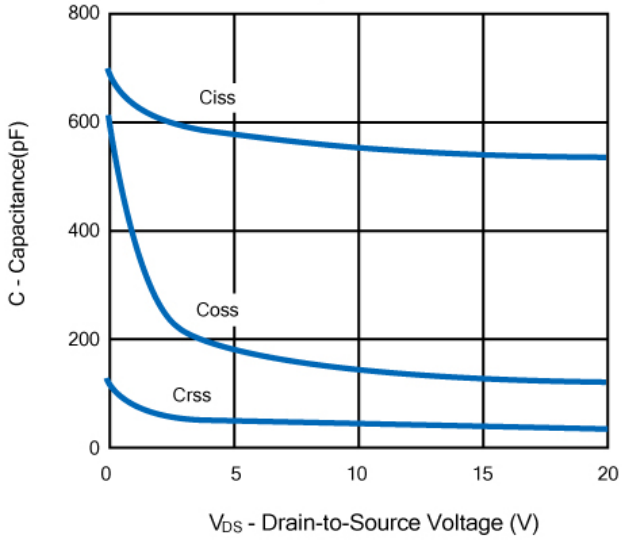
On Resistance vs. Junction Temperature



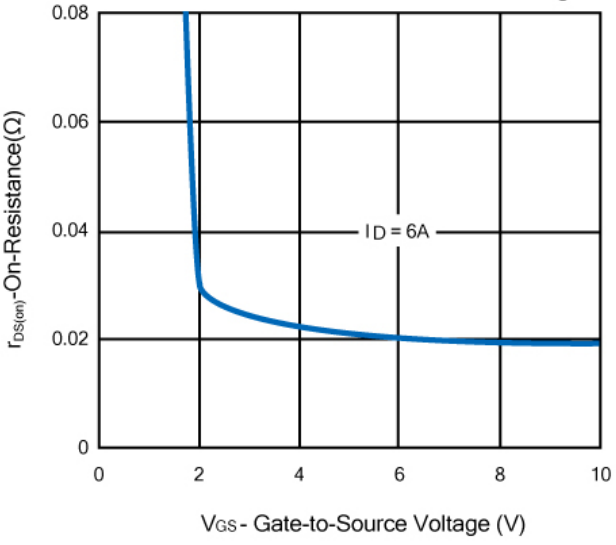
On-Resistance vs. Drain Current



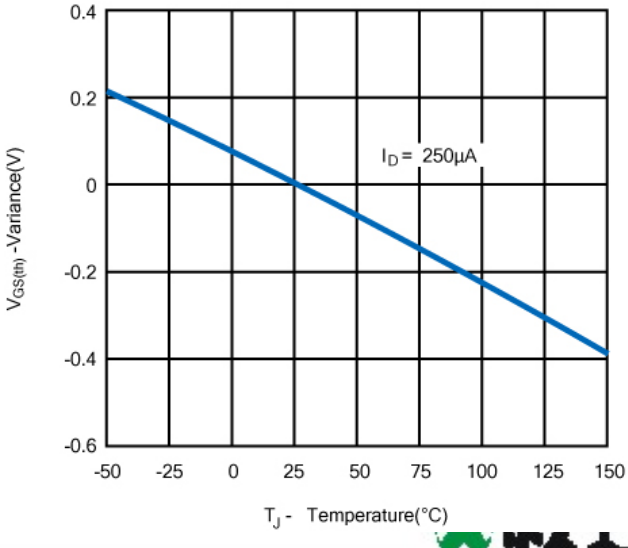
Capacitance



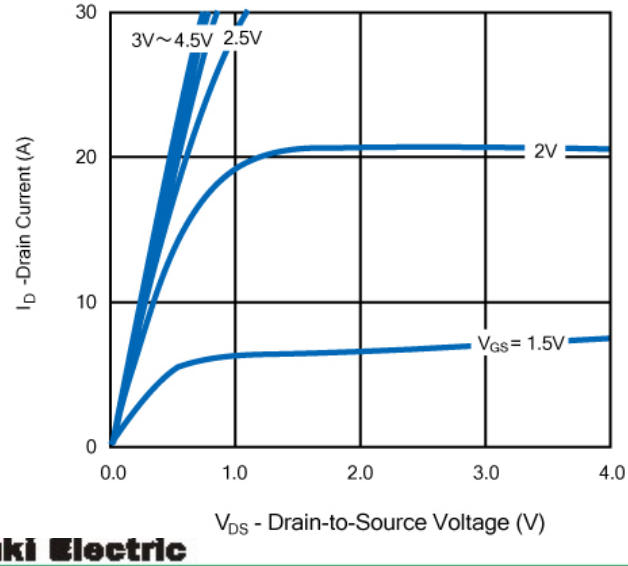
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



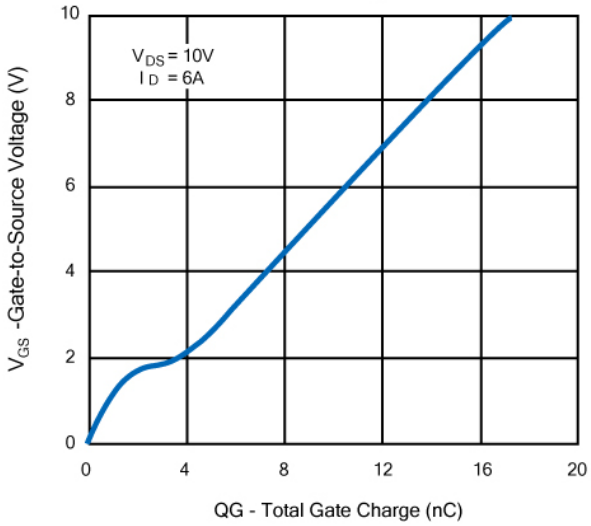
On-Region Characteristics



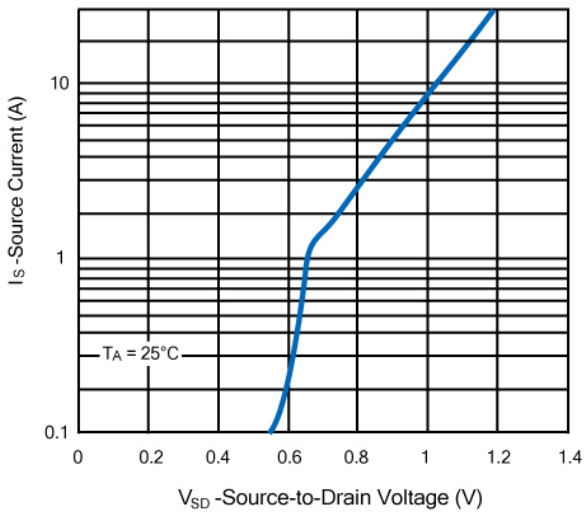
Dual N-Channel 20V (D-S) MOSFET

Typical Characteristics (T_J =25℃ Noted)

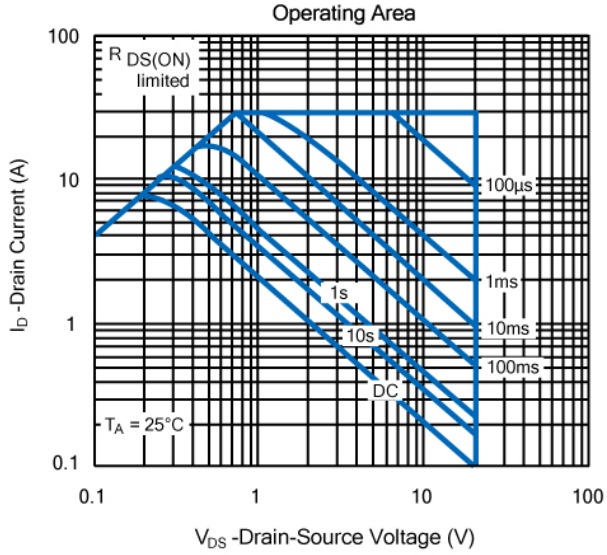
Gate Charge



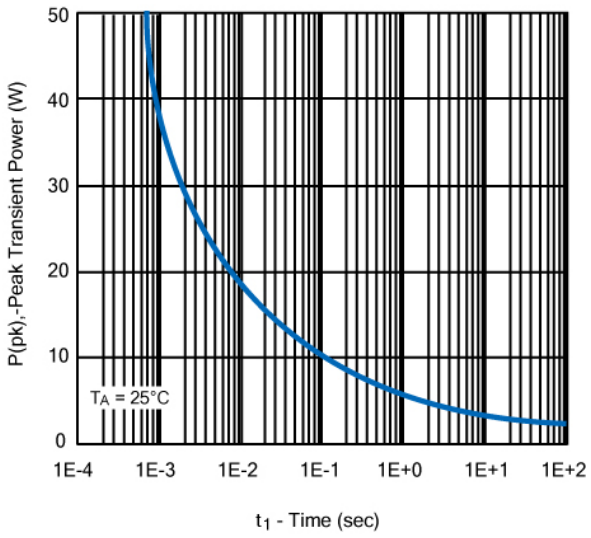
Source to Drain Diode Forward Voltage



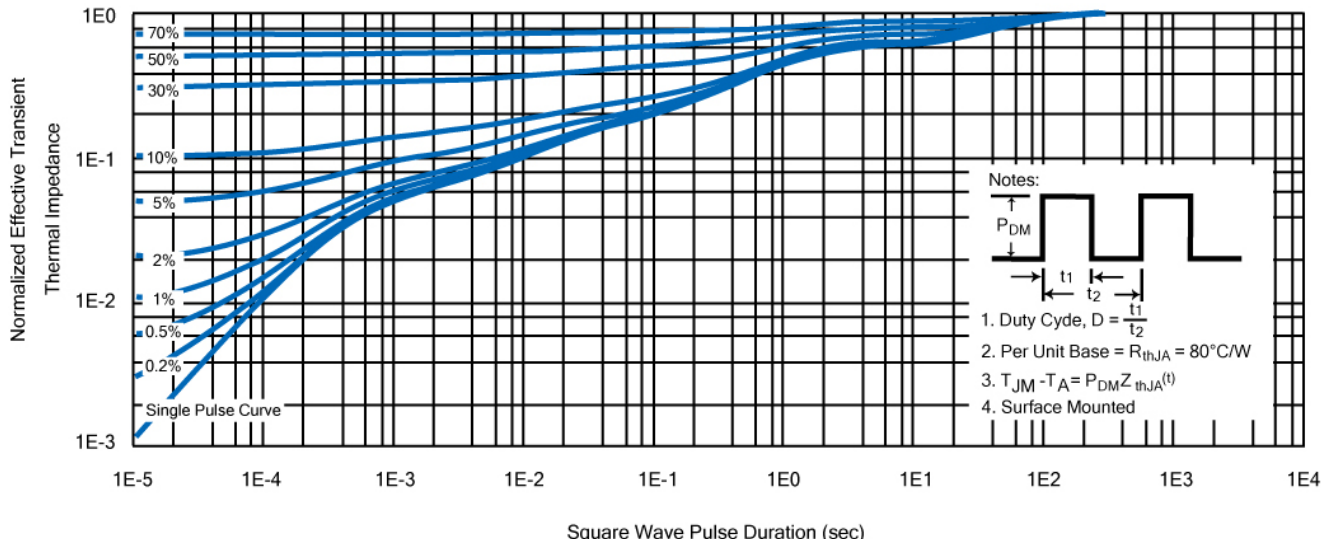
Maximum Forward Biased Safe Operating Area



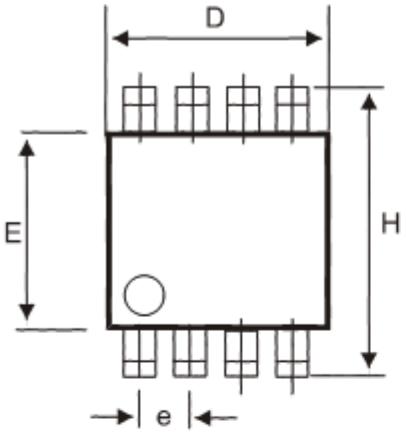
Single Pulse Maximum Power Dissipation

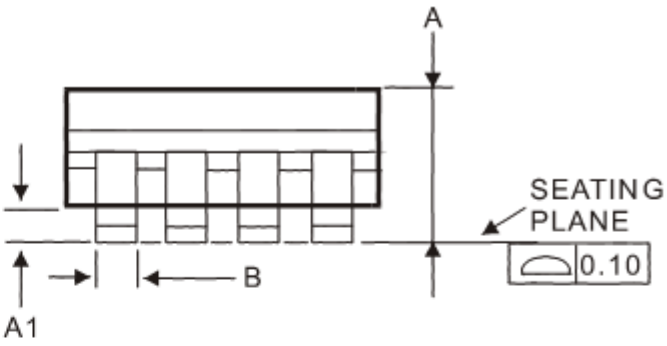


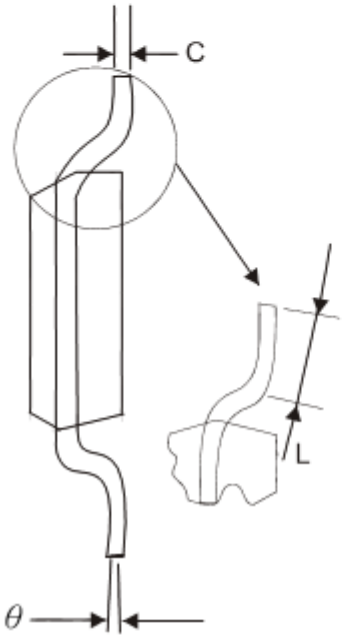
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

Note: 1. Refer to JEDEC MS-012AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs . Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per side.