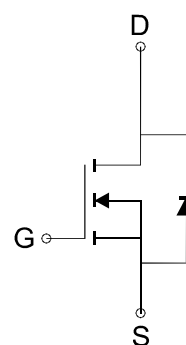
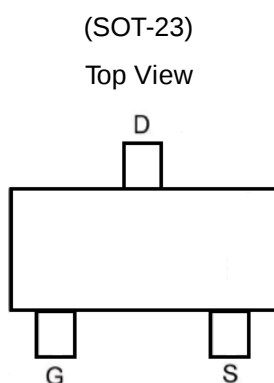


N - Channel 100-V (D-S) MOSFET

GENERAL DESCRIPTION

The MEBSS123 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION



N-Channel MOSFET

FEATURES

- $R_{DS(ON)} \leq 6\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 10\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

Ordering Information: MEBSS123 (Pb-free)

MEBSS123-G (Green product-Halogen free)

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain	$T_A=25^\circ\text{C}$	I_D	0.17	A
Pulsed Drain Current		I_{DM}	0.7	A
Maximum Power Dissipation	$T_A=25^\circ\text{C}$	P_D	0.36	W
Operating Junction Temperature		T_J	-55 to 150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	350	$^\circ\text{C/W}$

* The device mounted on 1in^2 FR4 board with 2 oz copper

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N - Channel 100-V (D-S) MOSFET

Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μ A	100			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =1mA	0.8		2.0	V
I _{GSS}	Gate-Body Leakage	V _{DS} =0V, V _{GS} = $\pm$ 20V			$\pm$ 100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V			1	μ A
R _{DS(ON)}	Drain-Source On-Resistance*	V _{GS} =10V, I _D =100mA		3	6	Ω
		V _{GS} =4.5V, I _D =100mA		3	10	
V _{SD}	Diode Forward Voltage *	I _S =0.34A, V _{GS} =0V		0.9	1.3	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =10V, V _{GS} =10V, I _D =0.22A		6.32		nC
Q _{gs}	Gate-Source Charge			1.55		
Q _{gd}	Gate-Drain Charge			0.68		
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		42.7		pF
C _{oss}	Output Capacitance			14		
C _{rss}	Reverse Transfer Capacitance			3		
t _{d(on)}	Turn-On Delay Time	V _{DD} =30V, R _L =107 Ω I _D =0.28A, V _{GS} =10V, R _{GEN} =50 Ω		5.53		ns
t _r	Turn-On Rise Time			21.7		
t _{d(off)}	Turn-Off Delay Time			5.31		
t _f	Turn-Off Fall Time			6.38		

Notes: a, pulse test: pulse width $\leq$ 300 μ s, duty cycle $\leq$ 2%, Guaranteed by design, not subject to production testing.

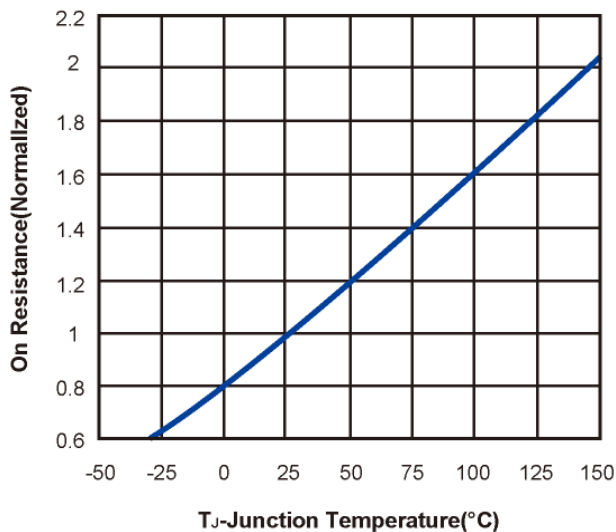
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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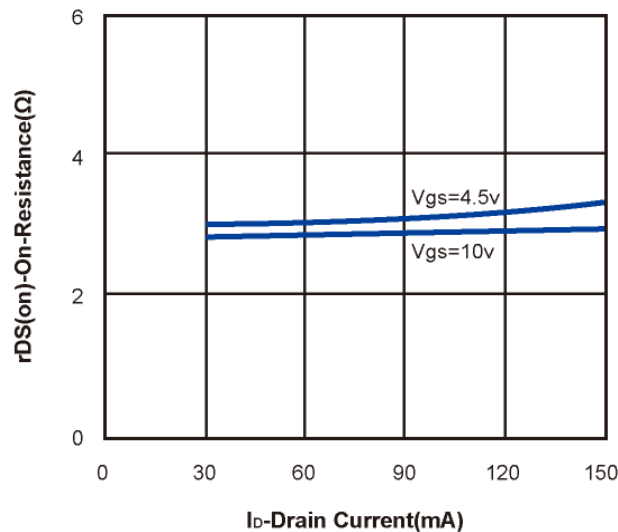
N - Channel 100-V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)

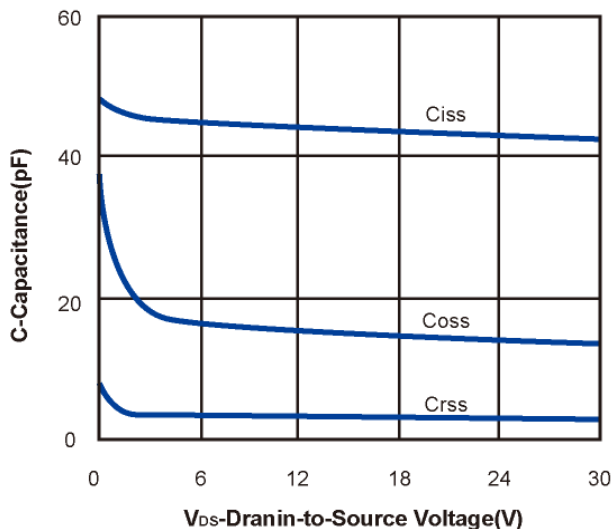
On Resistance vs. Junction Temperature



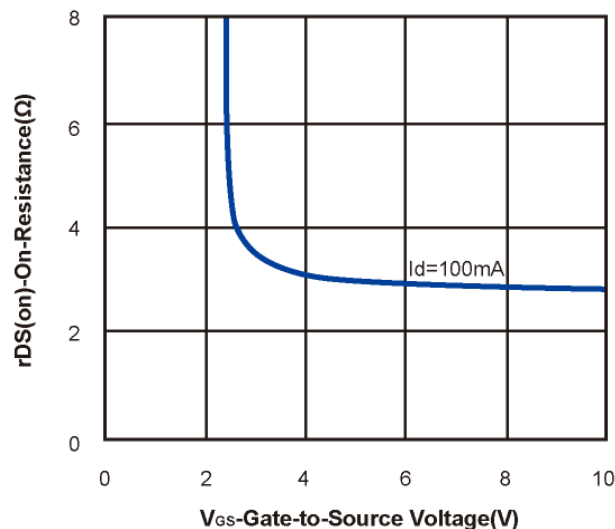
On Resistance vs. Drain Current



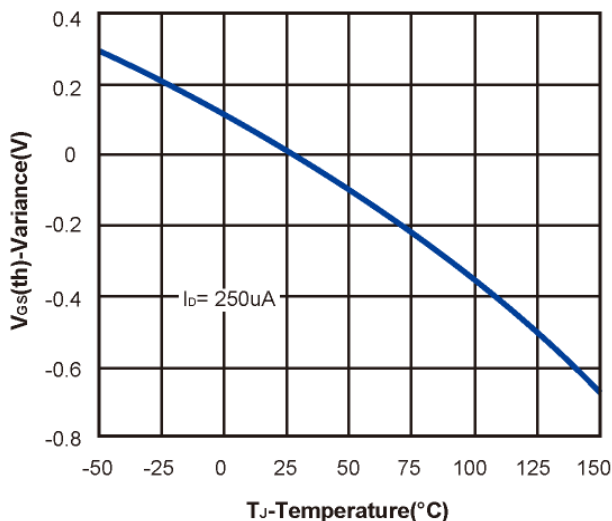
Capacitance



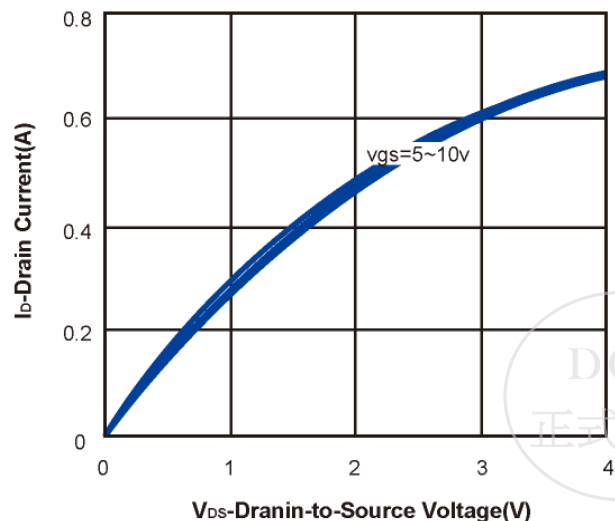
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage

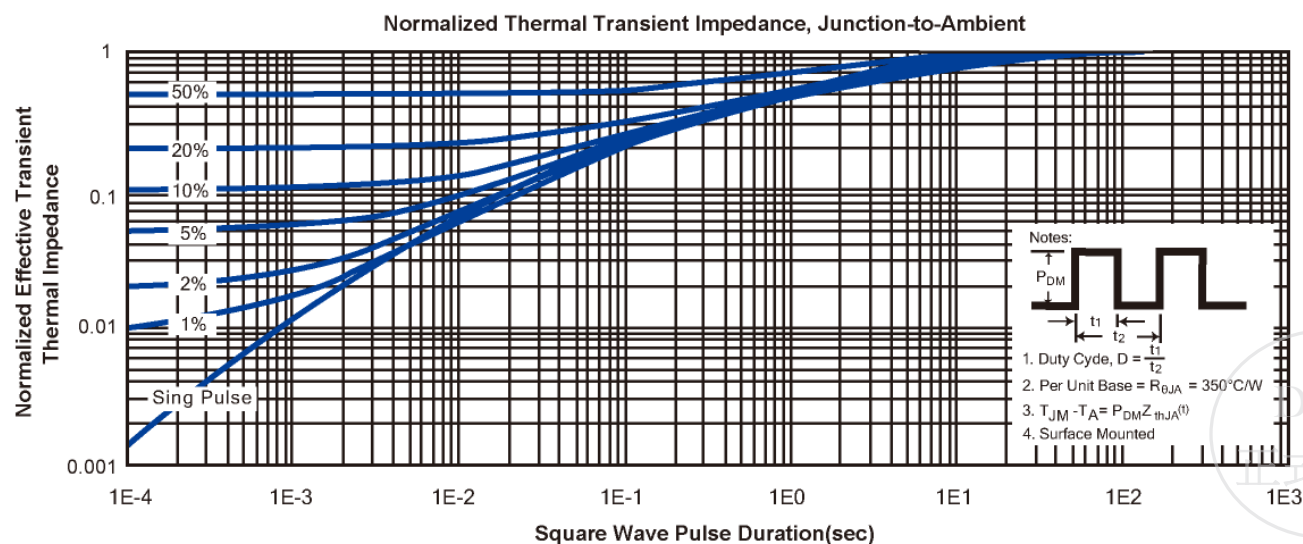
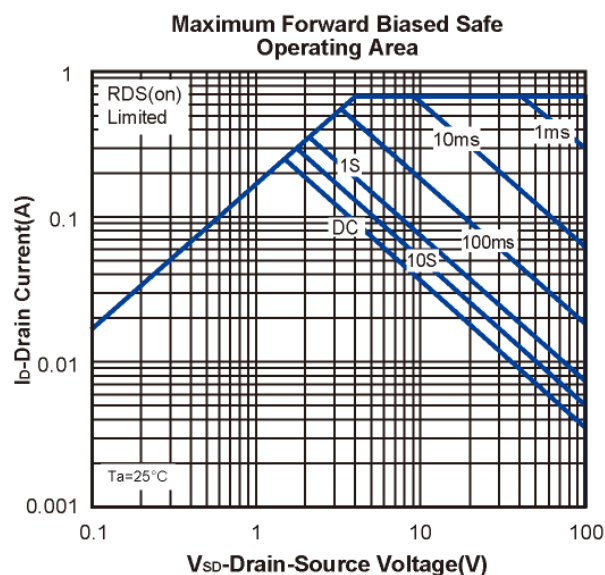
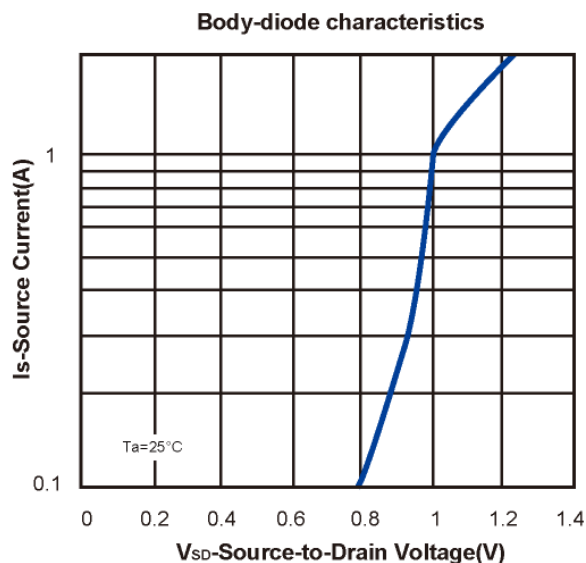
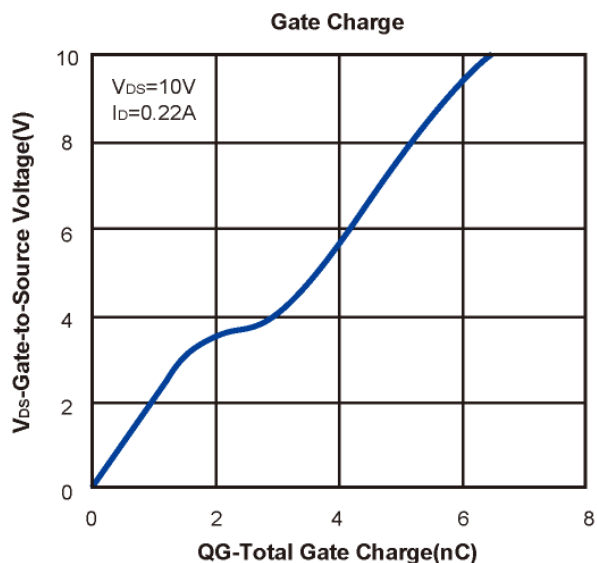


On Region Characteristics

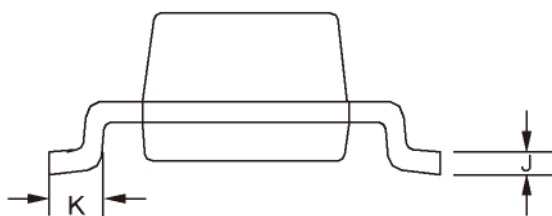
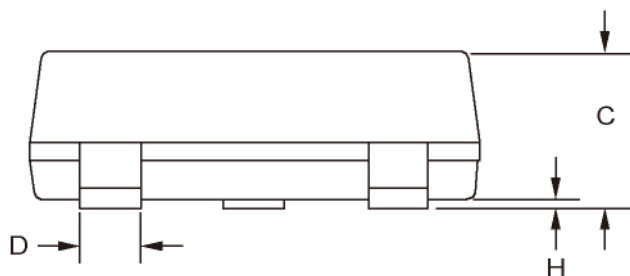
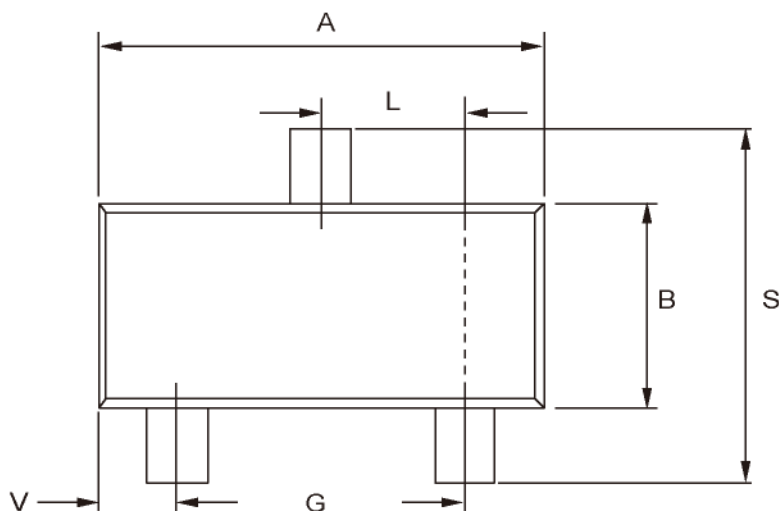


N - Channel 100-V (D-S) MOSFET

Typical Characteristics (T_J = 25°C Noted)



SOT-23 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60

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