MEBSS138/MEBSS138-G

N - Channel 50V (D-S) MOSFET

GENERAL DESCRIPTION

The MEBSS138 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 3\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 3.5\Omega @ VGS=5V$
- $R_{DS(ON)} \leqq 7\Omega @ VGS=2.75V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

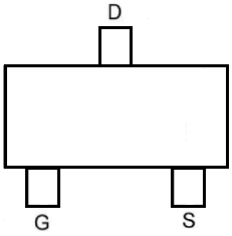
APPLICATIONS

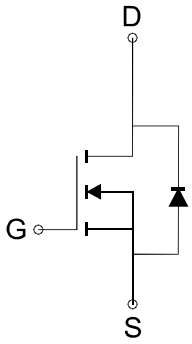
- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

PIN CONFIGURATION

(SOT-23)

Top View





N-Channel MOSFET

Ordering Information: MEBSS138 (Pb-free)

MEBSS138-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	50	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain	T_A=25℃	I_D	0.3	A
Pulsed Drain Current		I_{DM}	1	A
Maximum Power Dissipation	T_A=25℃	P_D	0.36	W
Junction and Storage Temperature Range		TJ, Tstg	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	350	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	50			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=1mA	0.7		1.5	V
I_{GSS}	Gate-Body Leakage	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=50V, V_{GS}=0V			0.5	μA
$R_{DS(ON)}$	Drain-Source On-Resistance*	V_{GS}=10V, I_D=200mA		1.3	3	Ω
		V_{GS}=5V, I_D=200mA		1.4	3.5	
		V_{GS}=2.75V, I_D=200mA		1.6	7	
V_{SD}	Diode Forward Voltage *	I_S=0.44A, V_{GS}=0V		0.8	1.4	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=25V, V_{GS}=10V, I_D=0.22A		7.03		nC
Qgs	Gate-Source Charge			1.84		
Qgd	Gate-Drain Charge			0.65		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		8.7		Ω
Ciss	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1MHz		42		pF
Coss	Output Capacitance			15		
Crss	Reverse Transfer Capacitance			3		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=30V, R_L =103Ω I_D=0.29A, V_{GS}=10V, R_{GEN}=6Ω		4.63		ns
t_r	Turn-On Rise Time			6.8		
$t_{d(off)}$	Turn-Off Delay Time			18.9		
t_f	Turn-Off Fall Time			11.4		

Notes: a, pulse test: pulse width≦ 300us, duty cycle≦ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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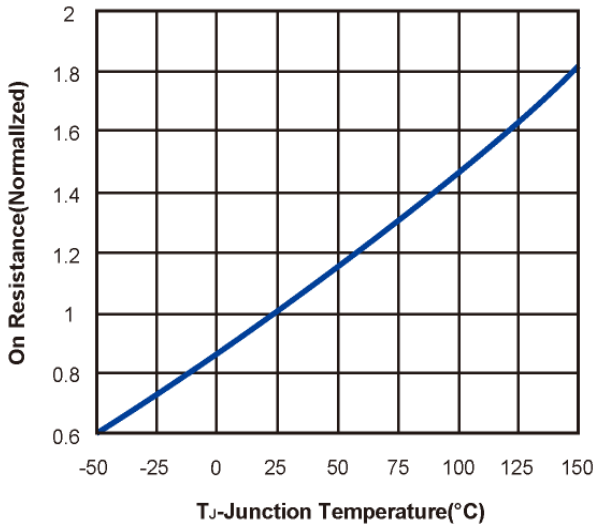
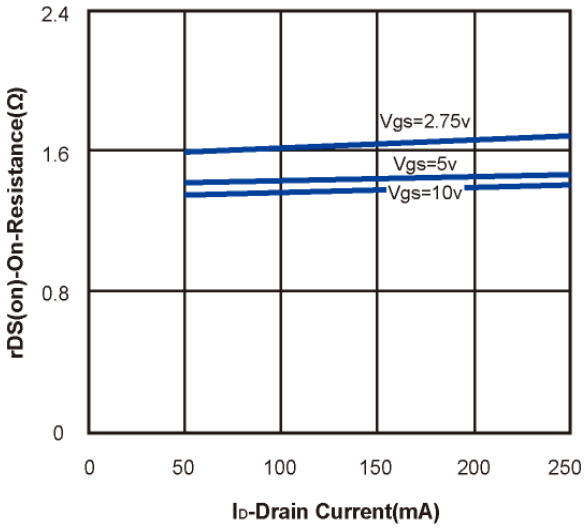
Typical Characteristics (T_J =25℃ Noted)

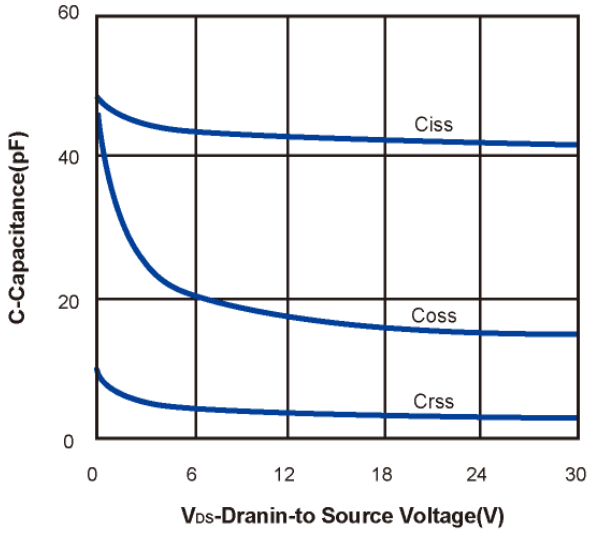
On Resistance vs. Junction Temperature



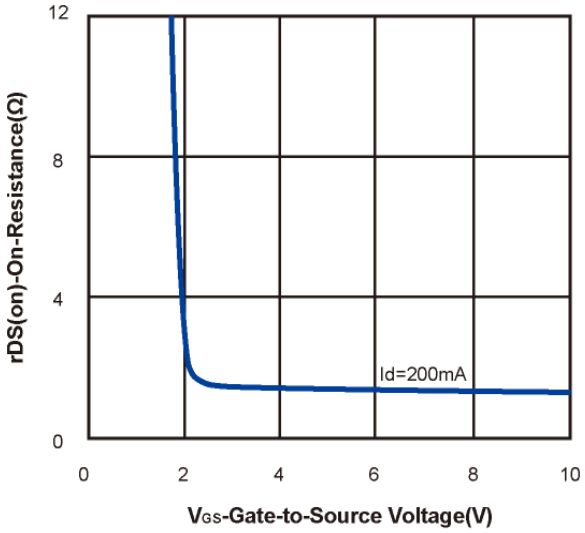
On Resistance vs. Drain Current



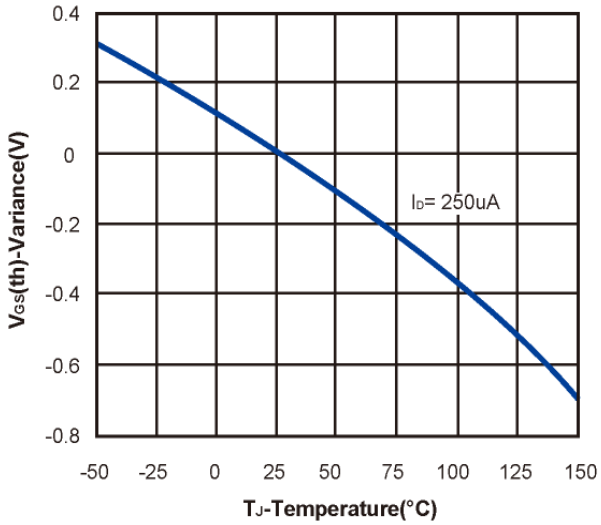
Capacitance



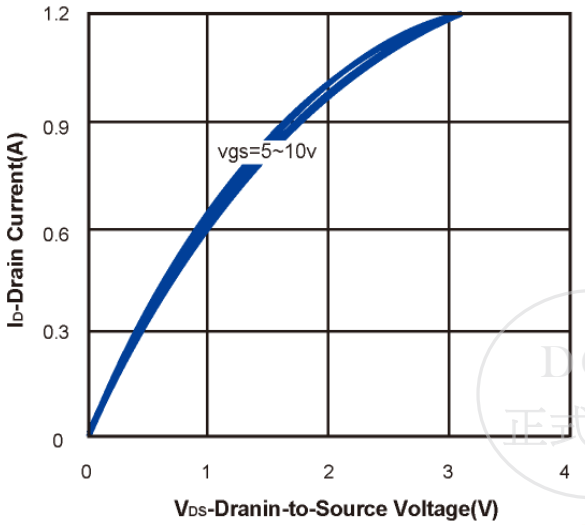
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



On-Region Characteristics



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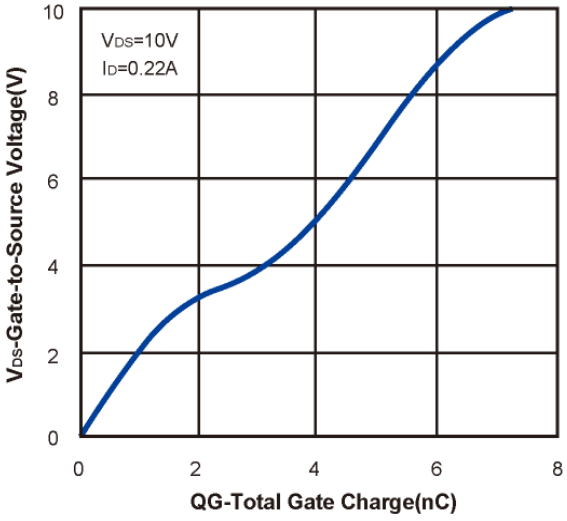
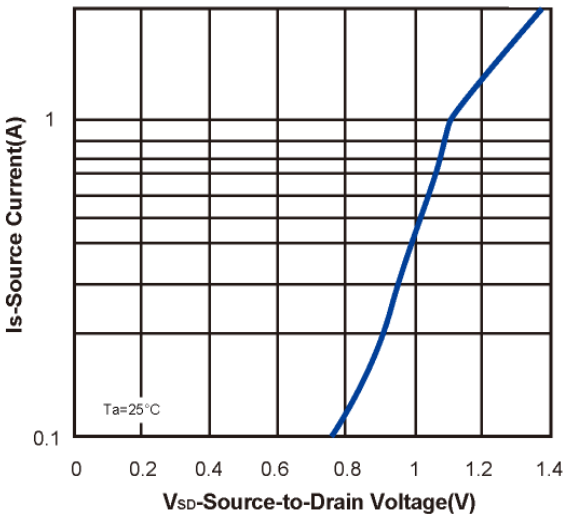
Typical Characteristics (T_J =25℃ Noted)

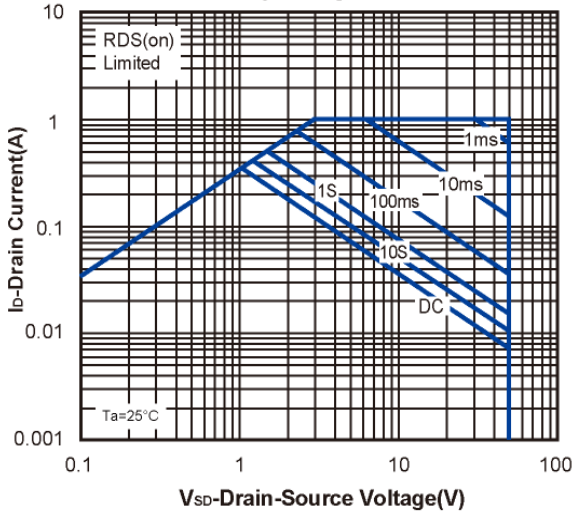
Gate Charge



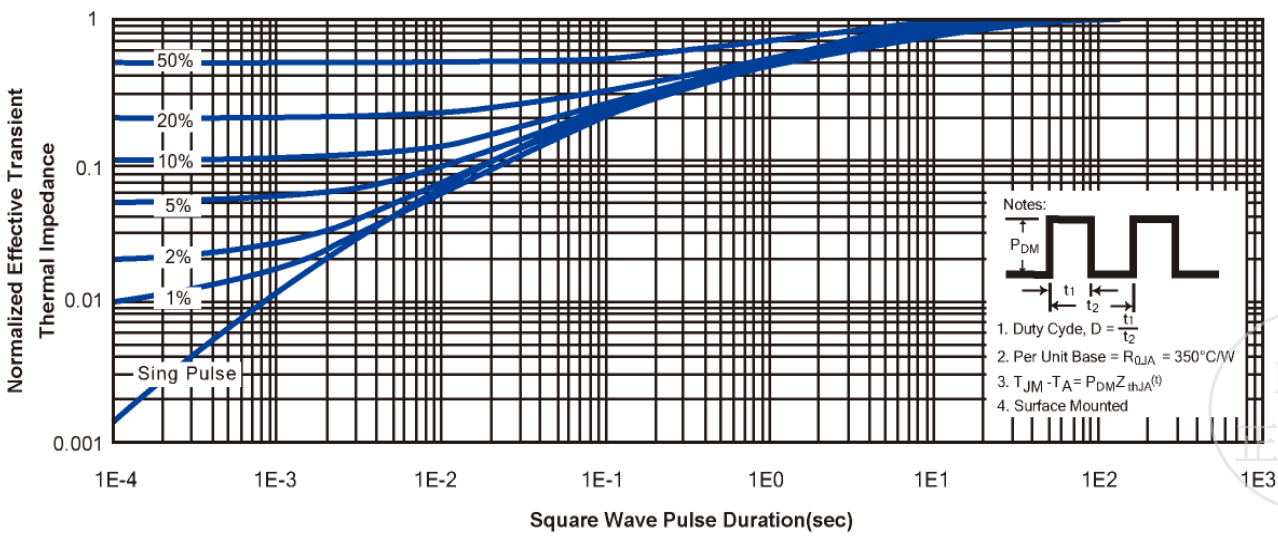
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



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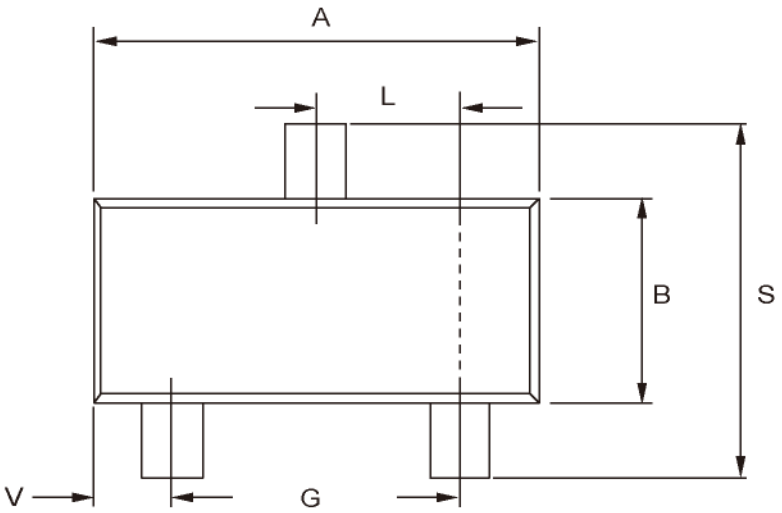
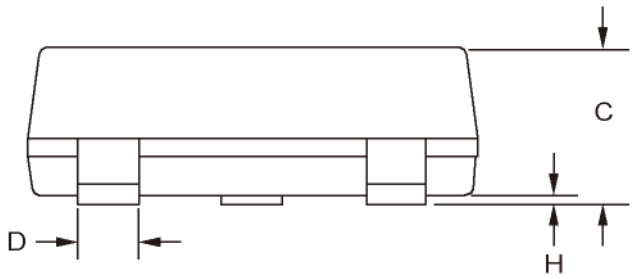
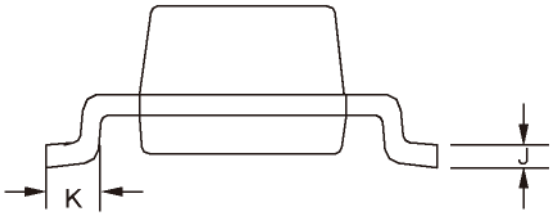
SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60