MEBSS84/ MEBSS84-G

P-Channel 50V Enhancement Mode

GENERAL DESCRIPTION

The MEBSS84 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)} \leqq 5\Omega @ V_{GS}$=-10V
- $R_{DS(ON)} \leqq 6\Omega @ V_{GS}$=-5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

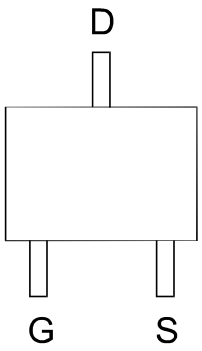
APPLICATIONS

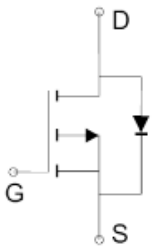
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(SOT-23)

Top View





P-Channel

Ordering Information:MEBSS84(Pb-free)

MEBSS84-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-50	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain	T_A=25℃	I_D	-0.2	A
Pulsed Drain Current		I_{DM}	-0.81	A
Maximum Power Dissipation	T_A=25℃	P_D	0.36	W
Storage Temperature Range		T_{stg}	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	350	℃/W

*The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-50			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.8		-2.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-50V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D= -100mA		2	5	Ω
		V_{GS}=-5V, I_D= -100mA		2	6	
V_{SD}	Diode Forward Voltage	I_S=-0.1A, V_{GS}=0V			-2.9	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-25V,V_{GS}=-10V,I_D=-0.5A		4.8		nC
Qg	Total Gate Charge	V_{DS}=-25, V_{GS}=-4.5V, I_D=-0.5A		1.8		
Qgs	Gate-Source Charge			2.5		
Qgd	Gate-Drain Charge			0.3		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V,f=1MHz		38		pF
Coss	Output Capacitance			4.8		
Crss	Reverse Transfer Capacitance			2.7		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-25V, R_L =50Ω R_G=25Ω, V_{GS}=-10V I_D=-0.5A		16.7		ns
t_r	Turn-On Rise Time			8.6		
$t_{d(off)}$	Turn-Off Delay Time			17.9		
t_f	Turn-Off Fall Time			5.3		

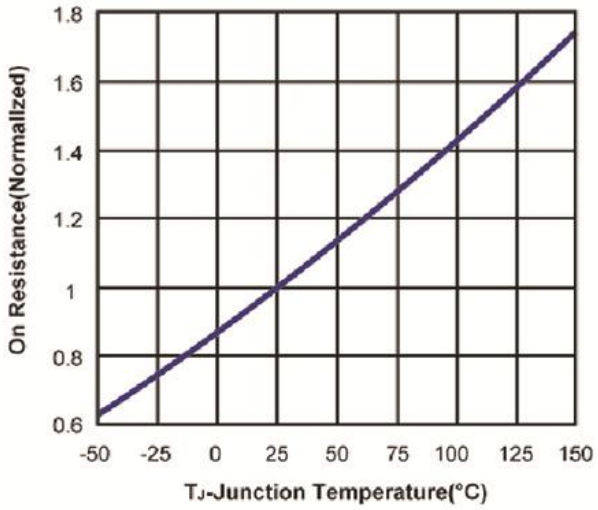
Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

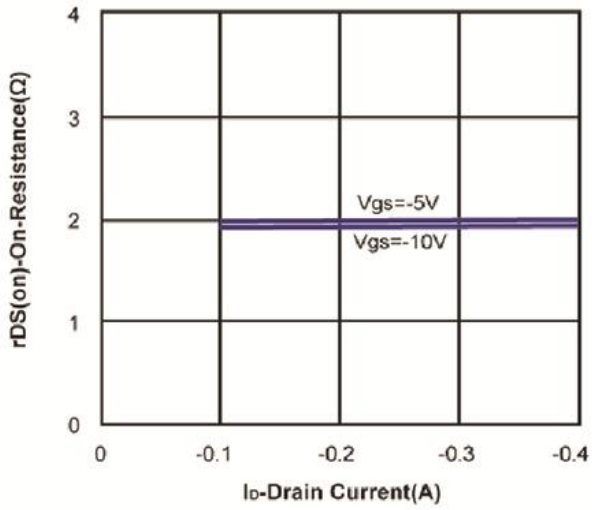
P-Channel 50V Enhancement Mode

Typical Characteristics (T_J =25℃ Noted)

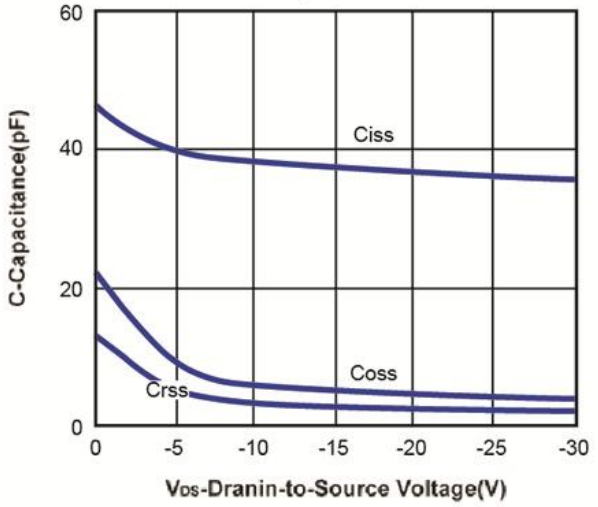
On Resistance vs. Junction Temperature



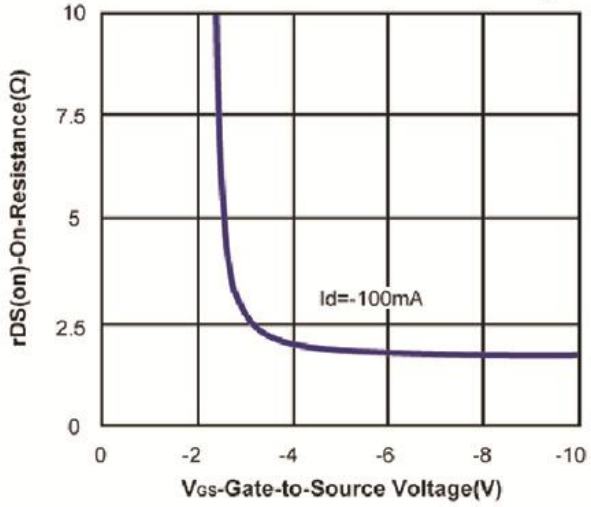
On Resistance vs. Drain Current



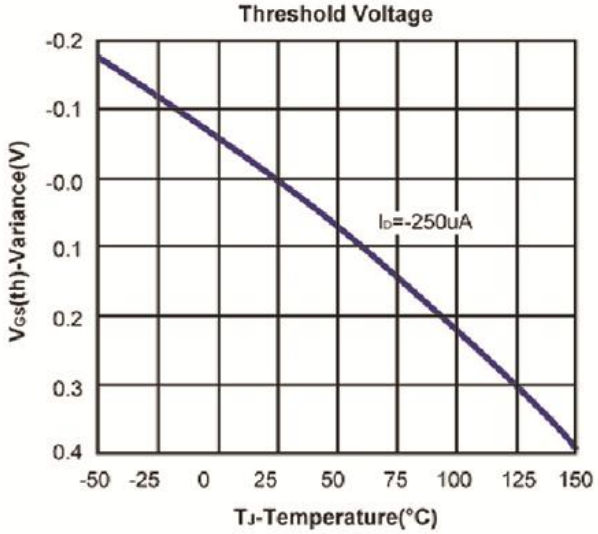
Capacitance



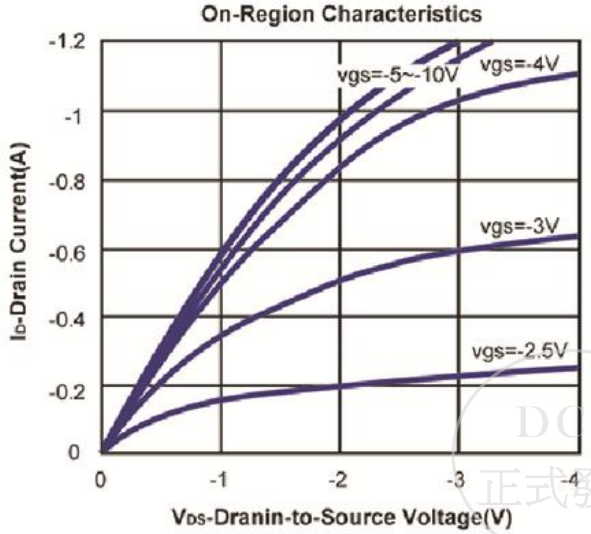
On Resistance vs. Gate-to-Source Voltage



Threshold Voltage



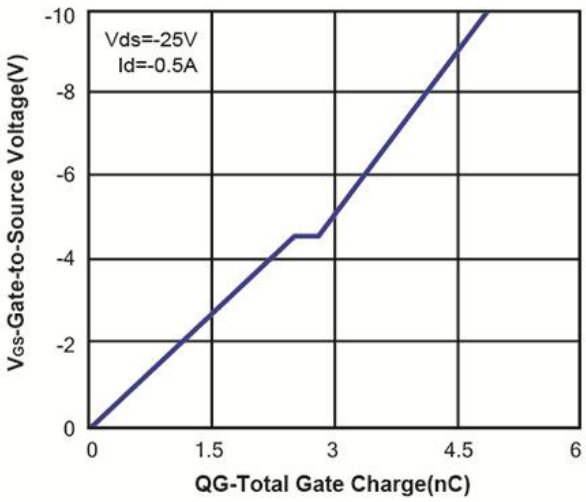
On-Region Characteristics



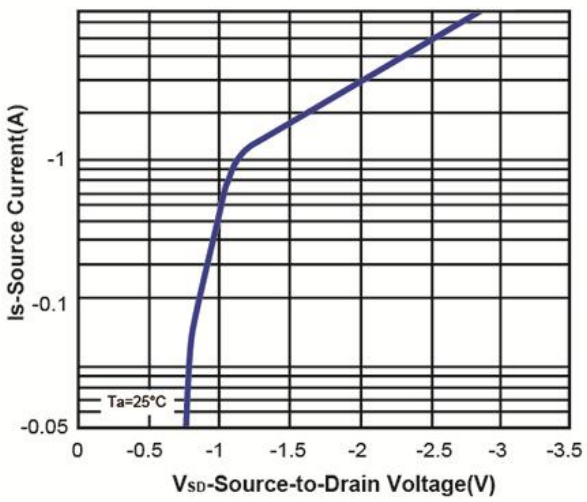
P-Channel 50V Enhancement Mode

Typical Characteristics (T_J =25℃ Noted)

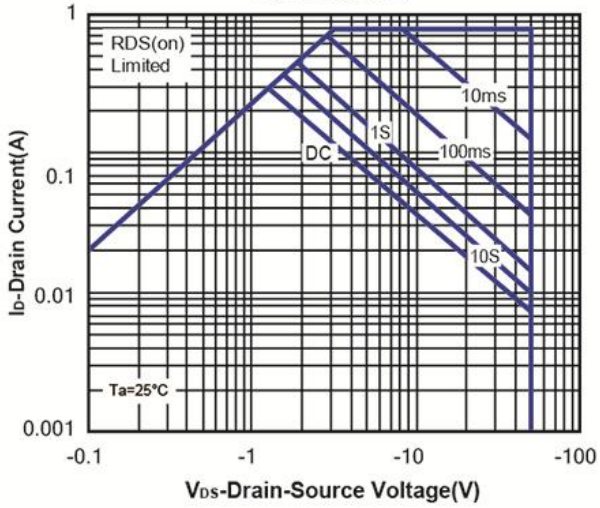
Gate Charge



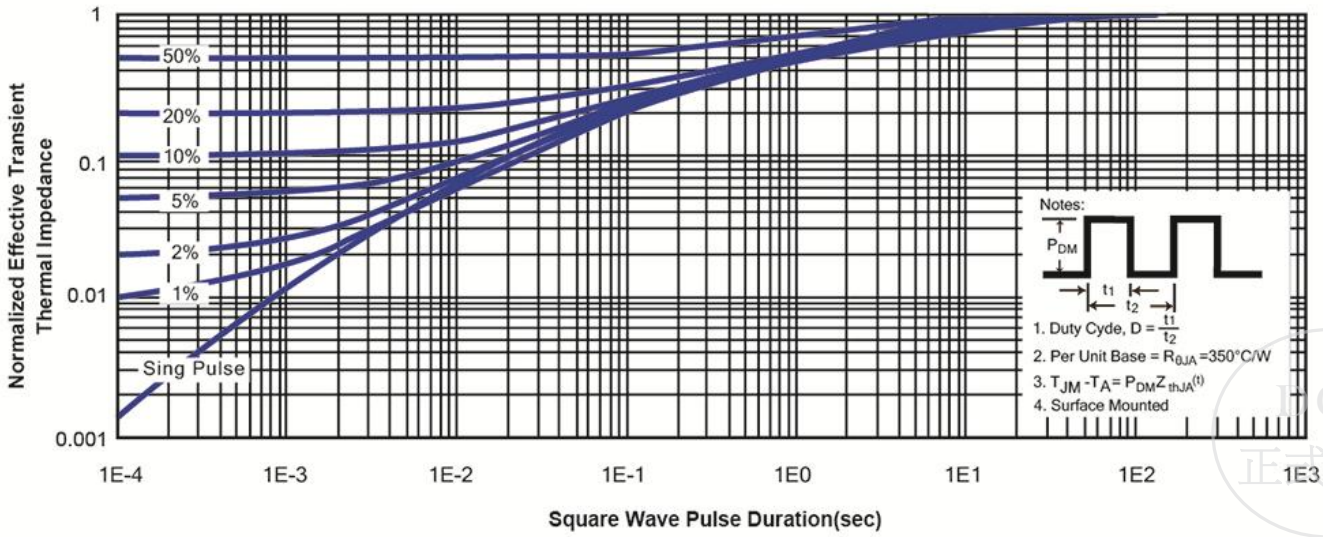
Body-diode characteristics



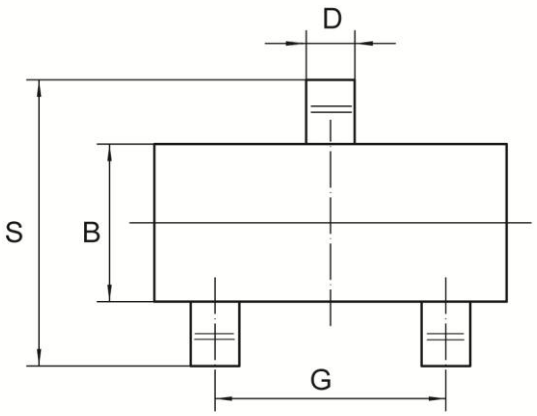
Maximum Forward Biased Safe Operating Area

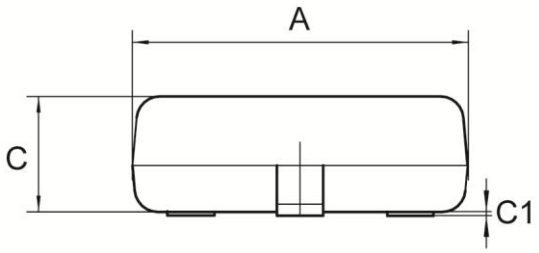


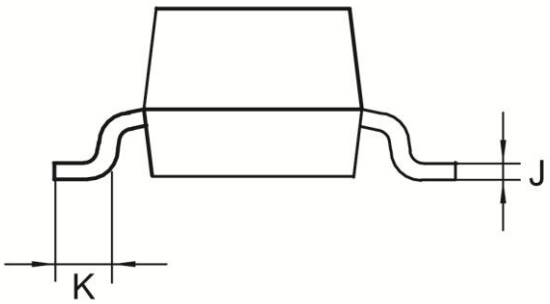
Normalized Thermal Transient Impedance, Junction-to-Ambient



小 SOT-23 Package Outline







Symbol	MILLIMETERS	
	MIN	MAX
A	2.8	3.0
B	1.2	1.4
C	0.9	1.1
C1	-	0.1
D	0.3	0.5
G	1.90 REF	
J	0.05	0.15
K	0.2	-
S	2.2	2.6