MEC1322

Keyboard and Embedded Controller for Notebook PC

Product Features

- ARM® Cortex®-M4 Processor Core
  - 32-Bit ARM v7-M Instruction Set Architecture
  - Hardware Floating Point Unit (FPU)
  - Single 4GByte Addressing Space (Von Neumann Model)
  - Little-Endian Byte Ordering
  - Bit-Banding Feature Included
  - NVIC Nested Vectored Interrupt Controller
    - Up to 240 Individually-Vectored Interrupt Sources Supported
    - 8 Levels of Priority, Individually Assignable By Vector
    - Chip-Level Interrupt Aggregator supported, to expand number of interrupt sources or reduce number of vectors
  - System Tick Timer
  - Complete ARM-Standard Debug Support
    - JTAG-Based DAP Port, Comprised of SWJ-DP and AHB-AP Debugger Access Functions
    - Full DWT Hardware Functionality: 4 Data Watchpoints and Execution Monitoring
    - Full FPB Hardware Breakpoint Functionality: 6 Execution Breakpoints and 2 Literal (Data) Breakpoints
  - Comprehensive ARM-Standard Trace Support
    - Full DWT Hardware Trace Functionality for Watchpoint and Performance Monitoring
    - Full ITM Hardware Trace Functionality for Instrumented Firmware Support and Profiling
    - Full ETM Hardware Trace Functionality for Instruction Trace
    - Full TPIU Functionality for Trace Output Communication
- 128K SRAM (Code or Data)
  - 96K Optimized for Code
  - 32K Optimized for Data
- LPC Interface
  - Supports LPC Bus frequencies of 19MHz to 33MHz
  - LPC I/O Cycles Decoded
  - LPC Memory Cycles Decoded
  - Clock Run Support
  - Serial IRQ
  - ACPI SCI interface
  - SMI# output
- Two SPI Memory Interfaces
  - 3-pin Full Duplex serial communication interface
  - Two Private and Two Shared Chip Selects
  - DMA Support
- 8042 Style Host Interface
  - Mailbox Registers Interface
    - Forty-three 8-Bit scratch registers
    - Two Register Mailbox Command Interface
    - Two Register SMI Source Interface
- Two ACPI Embedded Controller Interface
  - 1 or 4 Byte Data transfer capable
- ACPI Power Management Interface
  - SCI Event-Generating Functions
- Embedded Memory Interface
  - Host Serial IRQ Source
  - Provides Two Windows to On-Chip SRAM for Host Access
- Two Register Mailbox Command Interface
- Battery Backed (VCC0/VBAT) Resources
  - Power Fail Register
  - Power-Fail Status Register
  - Battery backed 64 byte memory
- Real Time Clock (RTC)
  - VCC0 (VBAT) Powered
  - 32KHz Crystal Oscillator
  - 32KHz Clock output available under VCC1 power
  - Time-of-Day and Calendar Registers
  - Programmable Alarms
  - Supports Leap Year and Daylight Savings Time
- Hibernation Timers
- General Purpose Analog to Digital Converter
  - 10-bit conversion precision
  - 10-bit conversion per channel is completed in less than 12us
  - 5 ADC channels
    - 10-bit Conversion with 2.9mV resolution
    - 0 to 3.3 VDC Conversion Range
  - Optional continuous sampling at a programmable rate
  - Internal Analog Voltage Reference (3.0V +/- 1%)
- Watch Dog Timer
- Four Programmable 16-bit and Two 32-bit Timers
  - Wake-capable Auto-reloading Timers
- Four Independent Hardware Driven PS/2 Ports
  - Fully functional on Main and/or Suspend Power
  - PS/2 Edge Wake Capable
- Four Programmable Pulse-Width Modulator Outputs
  - Independent Clock Rates
  - 16-Bit Duty Cycle Granularity
  - Operational in both Full on and Standby modes

- Four EC-based SMBus 2.0 Host Controllers
  - Allows Master or Dual Slave Operation
  - Controllers are Fully Operational on Standby Power
  - DMA-driven I2C Network Layer Hardware
  - I2C Datalink Compatibility Mode
  - Multi-Master Capable
  - Supports Clock Stretching
  - Programmable Bus Speeds
    - 400 KHz Fast-mode Capable
    - 1 Mbps Fast-mode Plus Capable
  - Hardware Bus Access "Fairness" Interface
  - SMBus Time-outs Interface
  - 5 Ports
  - 2 Port Flexible Multiplexing
- PECI 3.0 Interface
- Keyboard Matrix Scan Interface
  - 18 x 8 Interrupt/Wake Capable Multiplexed Keyboard Scan Matrix
  - Row Predrive Option
- Four Breathing/Blinking LED Interfaces
  - Programmable Blink Rates
  - Piecewise Linear Breathing LED Output Controller
  - Operational in EC Sleep States
- Dual Fan Tachometer Inputs
- RPM-Based Fan Speed Control Algorithm
  - Utilizes one TACH input and one PWM output
  - 3% accurate from 500 RPM to 16k RPM
  - Automatic Tachometer feedback
  - Aging Fan or Invalid Drive Detection
  - Spin Up Routine
  - Ramp Rate Control
  - RPM-based Fan Speed Control Algorithm
- Fast GATEA20 & Fast CPU_RESET
- RSMRST# Functionality Supporting System Deep Sleep
  - Compatible with south bridge SUSCLK/ RSMRST# gating rules
  - Replacement 32K distribution available when RSMRST# is asserted
- Integrated Power-on Reset Generator
  - VCC1_RST# open drain output
  - Accepts External driven Reset
- Anti-Glitch Protection on Power-on
- All Blocks Support Low Power Sleep Modes
- General Purpose Input/Output Pins
  - Low Power
  - High Configurability
- Two pin Debug Port with standard 16C550A register interface
  - Accessible from both Host and EC
- BC-Link Interconnection Bus
  - One High Speed Bus Master Controller
- Package Options
  - 128-pin VTQFP
  - 132-pin DQFN

Description

The MEC1322 incorporates a high-performance 32-bit ARM® Cortex®-M4 embedded microcontroller with 128 Kilobytes of SRAM and 32 Kilobytes of Boot ROM. It communicates with the system host using the Intel® Low Pin Count (LPC) bus.

The MEC1322 has two SPI memory interfaces that allow the EC to read its code from external SPI flash memory: private SPI and/or shared SPI. The Shared SPI interface allows for EC code to be stored in a shared SPI chip along with the system BIOS. The private SPI memory interface provides for a dedicated SPI flash that is only accessible by the EC.

The MEC1322 provides support for loading EC code from the private or shared SPI flash device on a VCC1 power-on. Before executing the EC code loaded from a SPI Flash Device, the MEC1322 validates the EC code using a digital signature encoded according to PKCS #1. The signature uses RSA-2048 encryption and SHA-256 hashing. This provides automated detection of invalid EC code that may be a result of malicious or accidental corruption. It occurs before each boot of the host processor, thereby ensuring a HW based root of trust not easily thwarted via physical replacement attack.

The MEC1322 is directly powered by two separate suspend supply planes (VBAT and VCC1) and senses the runtime power plane (VCC) to provide “Instant On” and system power management functions. It also contains an integrated VCC1 Reset Interface and a system Power Management Interface that supports low-power states and can drive state changes as a result of hardware wake events.

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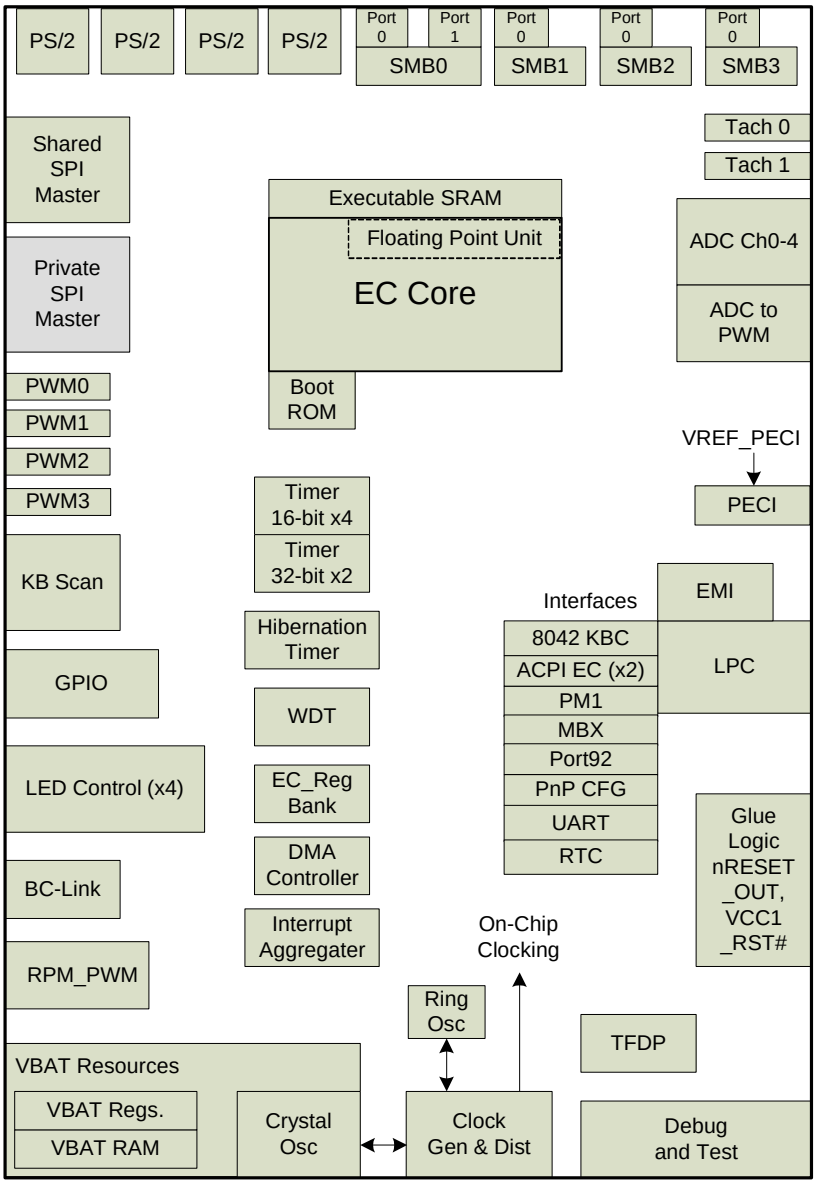
BLOCK DIAGRAM



PACKAGE OUTLINE

FIGURE 1: 128-PIN VTQFP PACKAGE OUTLINE

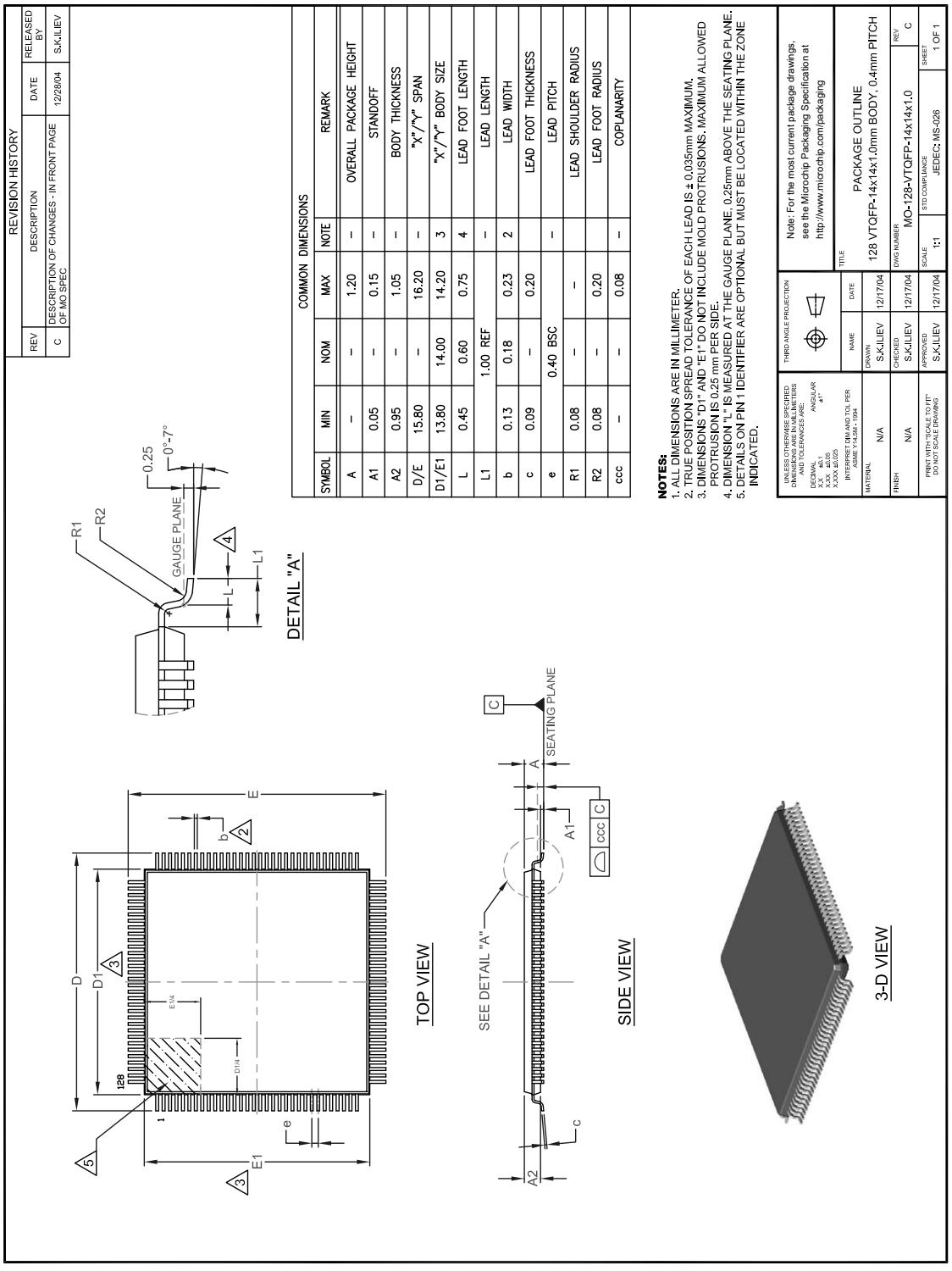


FIGURE 2: 132-PIN DQFN PACKAGE OUTLINE (1 OF 2)

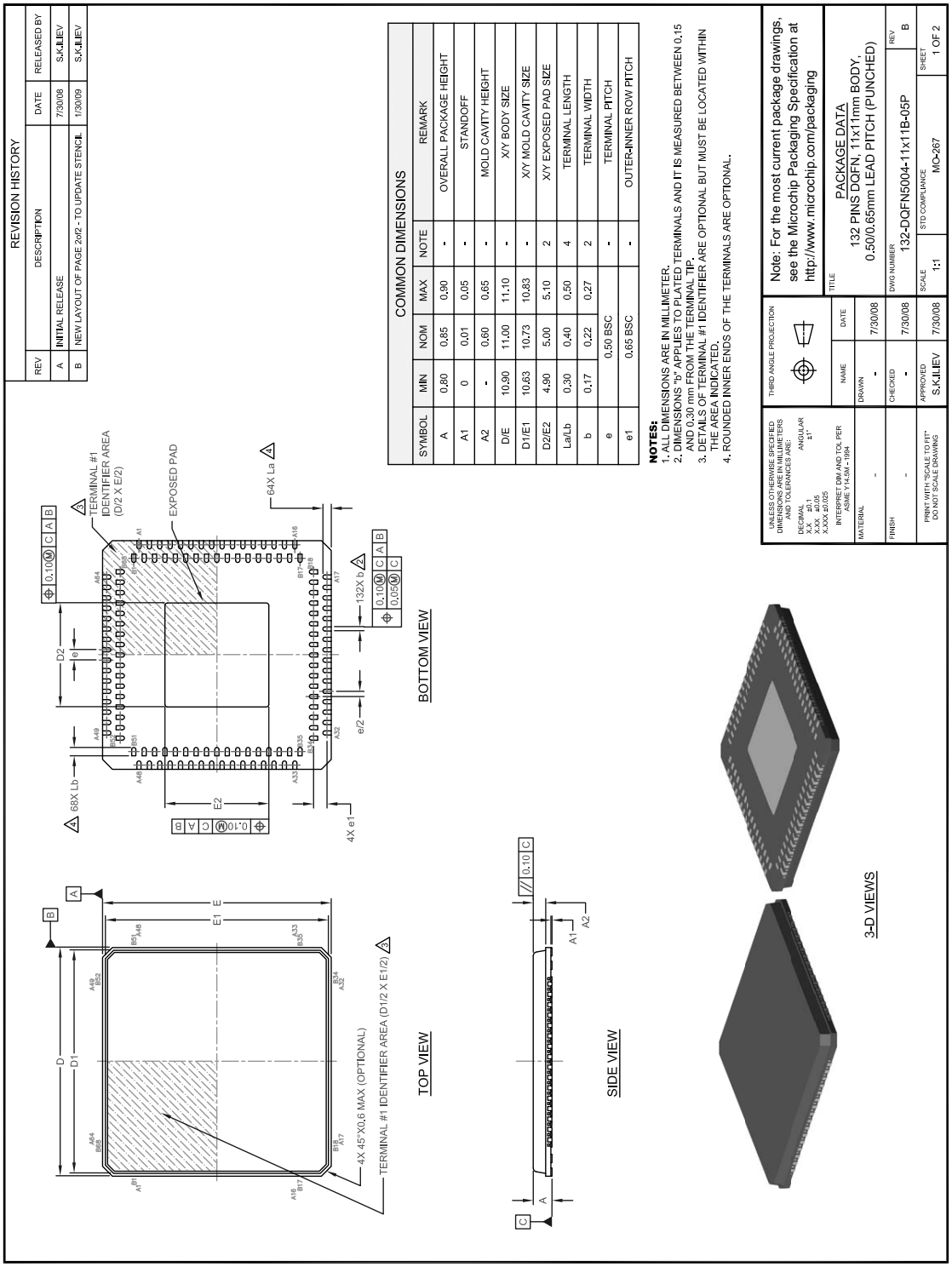
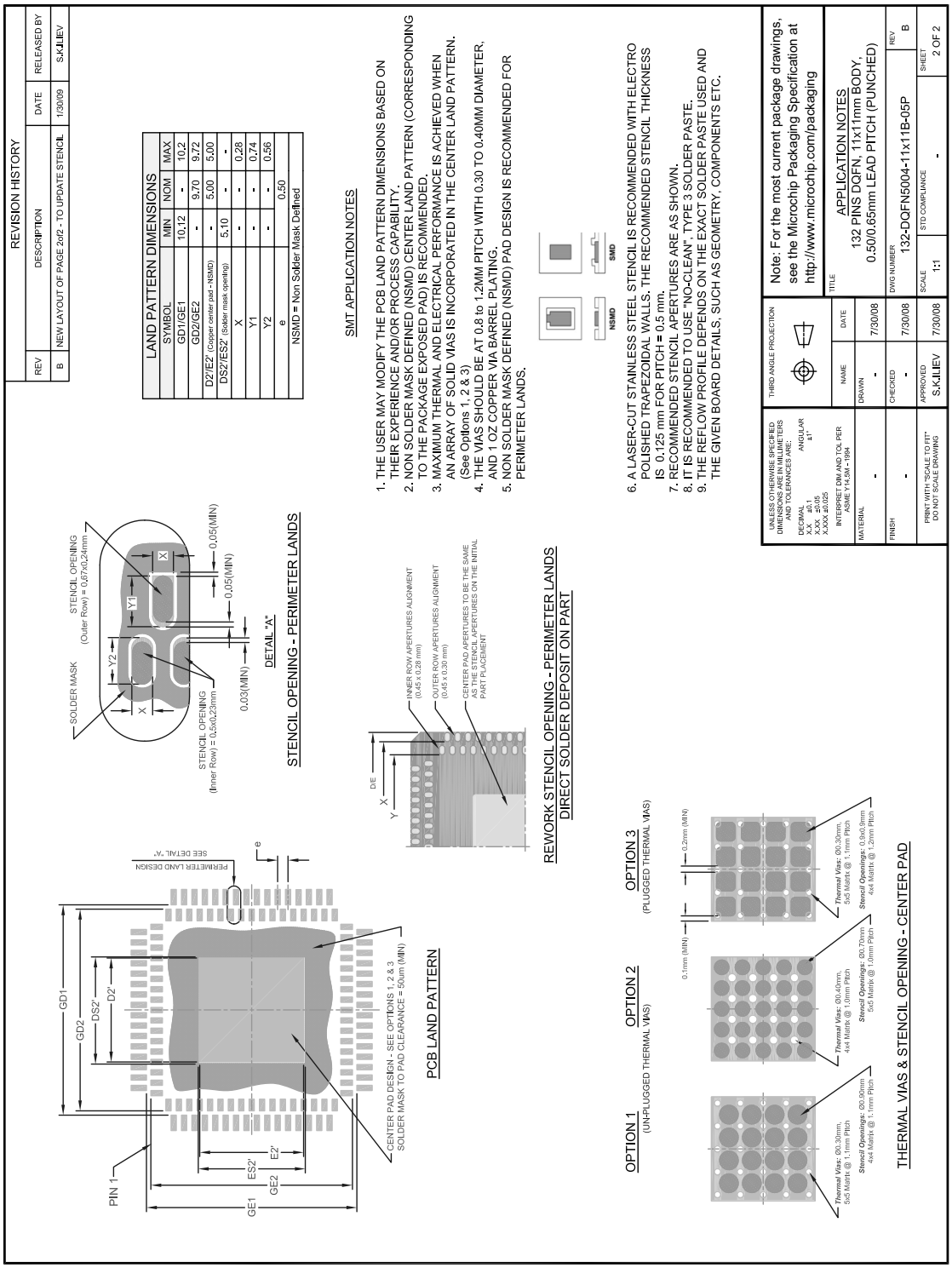


FIGURE 3: 132-PIN DQFN PACKAGE OUTLINE (2 OF 2)



APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001733A (05-05-14)	Document Release	

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PART NO.[1]	-	XXX[2]	-	XX	-	[X][3]
Device		Package		ROM Version		Tape and Reel Option

Device:	MEC1322[1]	
Package:	NU = 128 pin VTQFP[2] LZY = 132 pin DQFN[2]	
ROM Version:	C0 = Standard ROM	
Tape and Reel Option:	Blank = Tray packaging TR = Tape and Reel[3]	

Examples:

a) MEC1322-NU-C0 = 128-pin VTQFP
b) MEC1322-LZY-C0 = 132-pin DQFN

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

Note 2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html .

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